ANADIGICS

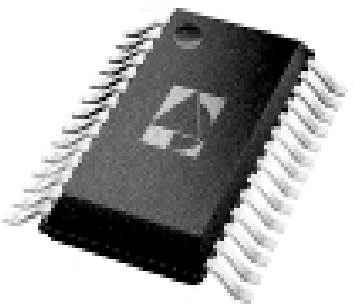
ARA2005

Reverse Amplifier with Step Attenuator

PRELIMINARY DATA SHEET - Rev 1.3

FEATURES

- Low cost integrated monolithic GaAs amplifier with step attenuator
- Attenuation Range: 0-58 dB, adjustable in 4dB increments via a 4 wire parallel control
- Meets DOCSIS distortion requirements at a +60dBmV output signal level
- Low distortion and low noise
- Frequency range: 5-100MHz
- 5 Volt operation
- -40 to +85 ^{0}C temperature range



S8 Package
28 Pin SSOP

APPLICATIONS

- MCNS/DOCSIS Compliant Cable Modems
- CATV Interactive Set-Top Box
- Telephony over Cable Systems
- OpenCable Set-Top Box
- Residential Gateway

PRODUCT DESCRIPTION

The ARA2005 is a monolithic GaAs device designed to provide the reverse path amplification and output level control functions in a Cable TV Set Top Box or Cable Modem. It incorporates a digitally controlled precision step attenuator, which is preceded by an ulta low noise amplifier stage and followed by an ulta-linear output driver amplifier. The ARA2005 uses a balanced circuit design that exceeds the MCNS/ DOCSIS requirement for harmonic performance at a +60 dBmV output level while requiring only a single +5V supply. Both the input and output of the device are matched to 75 Ohms with an appropriate transformer. The precision attenuator provides up to 58 dB of attenuation in 4 dB increments, programmable via a four-bit digital control interface. With external passive components, this device meets IEC 1000-4-12 and ANSI/IEEE C62.41-1991 100KHz ringwave tests, as well as IEC1000-4-5 1.2/50μS surge tests. The ARA2005 is offered in a 28-pin SSOP package.

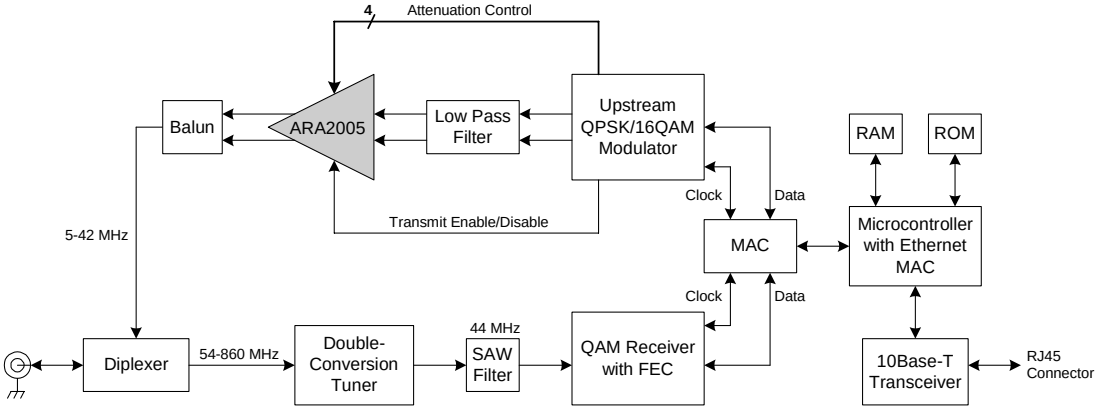


Figure 1: Cable Modem or Set Top Box Application Diagram

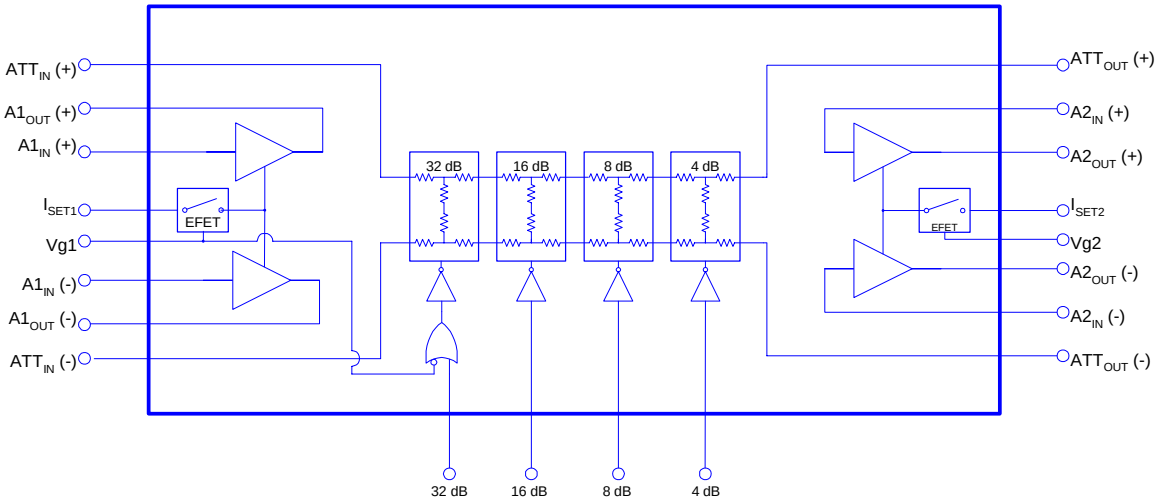


Figure 2: Functional Block Diagram

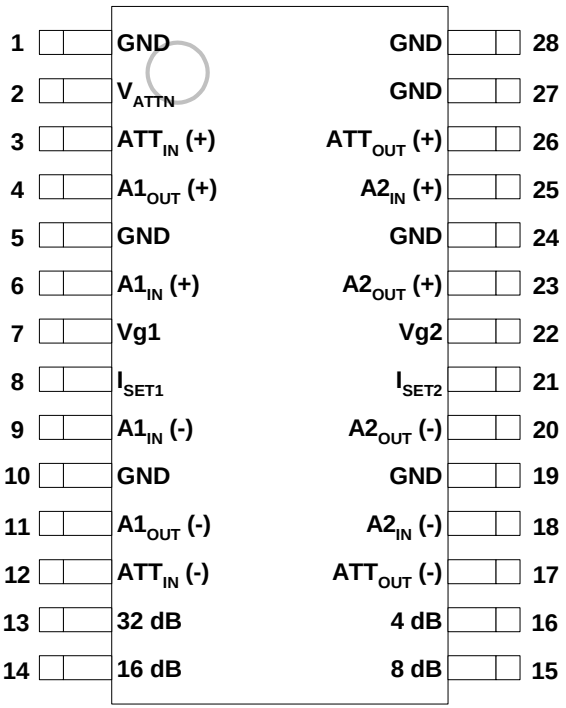


Figure 3: Pin Out

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	GND	Ground	15	8 dB	8 dB Attenuation Control Bit
2	V_{ATTN}	Supply for Attenuator	16	4 dB	4 dB Attenuation Control Bit
3	ATT_{IN} (+)	Attenuator Input (+) (1)	17	ATT_{OUT} (-)	Attenuator (-) Output (1)
4	$A1_{OUT}$ (+)	Amplifier A1 (+) Output	18	$A2_{IN}$ (-)	Amplifier A2 (-) Input (1)
5	GND	Ground	19	GND	Ground
6	$A1_{IN}$ (+)	Amplifier A1 (+) Input (1)	20	$A2_{OUT}$ (-)	Amplifier A2 (-) Output
7	Vg1	Amplifier A1 (+/-) Control	21	I_{SET2}	Amplifier A2 (+/-) Current Adjust
8	I_{SET1}	Amplifier A1 (+/-) Current Adjust	22	Vg2	Amplifier A2 (+/-) Control
9	$A1_{IN}$ (-)	Amplifier A1 (-) Input (1)	23	$A2_{OUT}$ (+)	Amplifier A2 (+) Output
10	GND	Ground	24	GND	Ground
11	$A1_{OUT}$ (-)	Amplifier A1 (-) Output	25	$A2_{IN}$ (+)	Amplifier A2 (+) Input (1)
12	ATT_{IN} (-)	Attenuator Input (-) (1)	26	ATT_{OUT} (+)	Attenuator (+) Output (1)
13	32 dB	32 dB Attenuation Control Bit	27	GND	Ground
14	16 dB	16 dB Attenuation Control Bit	28	GND	Ground

Notes:
(1) Pins should be AC-coupled. No external DC bias should be applied.

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Analog Supply (pins 2, 4, 11, 20, 23)	0	9	VDC
Amplifier Controls Vg1, Vg2 (pins 7, 22)	-5	2	V
RF Power at Inputs (pins 6, 9)	-	+60	dBmV
Attenuator Controls (pins 13, 14, 15, 16)	0	6	V
Storage Temperature	-55	+200	^{0}C
Soldering Temperature	-	260	^{0}C
Soldering Time	-	5	Sec

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Notes:

1. Pins 3, 6, 9, 12, 17, 18, 25 and 26 should be AC-coupled. No external DC bias should be applied.

2. Pins 8 and 21 should be grounded or pulled to ground through a resistor. No external DC bias should be applied.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT
Amplifier Supply: V_{DD} (pins 4, 11, 20, 23)	4.5	5	7	VDC
Attenuator Supply: V_{ATTN} (pin 2)	V_{DD}-0.5	5	7	VDC
Attenuator Controls (pins 13, 14, 15, 16)	0	-	V_{DD}+0.5	V
Amplifier Controls Vg1, Vg2 (pins 7, 22)	-5	1	2	V
Case Temperature	-40	25	85	^{0}C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: DC Electrical Specifications

T_A=25°C; V_{DD}, V_{ATTN} = +5.0 VDC; Vg1, Vg2 = +1.0 V (Tx enabled); Vg1, Vg2 = 0 V (Tx disabled)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Amplifier A1 Current (pins 4, 11)	- -	48 2.4	80 6	mA	Tx enabled Tx disabled
Amplifier A2 Current (pins 20, 23)	- -	70 3.7	110 9	mA	Tx enabled Tx disabled
Attenuator Current (pin 2)	-	2	5	mA	
Total Power Consumption	- -	600 40	900 100	mW	Tx enabled Tx disabled

Table 5: AC Electrical Specifications

T_A=25°C; V_{DD}, V_{ATTN} = +5.0 VDC; Vg1, Vg2 = +1.0 V (Tx enabled); Vg1, Vg2 = 0 V (Tx disabled)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Gain (10 MHz)	27.5	29.3	30.5	dB	0 dB attenuation setting
Gain Flatness	- -	0.75 1.5	- -	dB	5 to 42 MHz 5 to 65 MHz
Gain Variation over Temperature	-	-0.006	-	dB/°C	
Attenuation Steps 4 dB 8 dB 16 dB 32 dB	 3.6 7.5 15.0 30.2	 3.75 7.75 15.4 30.75	 4.0 8.0 15.8 31.3	dB	Monotonic
Maximum Attenuation	56.3	57.8	59.1	dB	
2nd Harmonic Distortion Level (10 MHz)	-	-75	-53	dBc	+60 dBmV into 75 Ohms
3rd Harmonic Distortion Level (10 MHz)	-	-60	-53	dBc	+60 dBmV into 75 Ohms
3rd Order Output Intercept	78	-	-	dBmV	
1 dB Gain Compression	-	68.5	-	dBmV	
Noise Figure	-	3.0	4.0	dB	Includes input balun loss

Note: As measured in ANADIGICS test fixture

continued: AC Electrical Specifications

T_A=25°C; V_{DD}, V_{ATTN} = +5.0 VDC; Vg1, Vg2 = +1.0 V (Tx enabled); Vg1, Vg2 = 0 V (Tx disabled)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Output Noise Power Active / No Signal / Min. Atten. Set. Active / No Signal / Max. Atten. Set.	 - -	 - -	 -38.5 -53.8	dBmV	Any 160 kHz bandwidth from 5 to 42 MHz
Isolation in Tx disable mode	-	52	-	dB	
Differential Input Impedance	-	300	-	Ohms	between pins 6 and 9 (Tx enabled)
Input Impedance	-	75	-	Ohms	with transformer (Tx enabled)
Input Return Loss (75 Ohm characteristic impedance)	- -	-20 -5	-12 -	dB	Tx enabled Tx disabled
Differential Output Impedance	-	300	-	Ohms	between pins 20 and 23
Output Impedance	-	75	-	Ohms	with transformer
Output Return Loss (75 Ohm characteristic impedance)	- -	-17 -15	-12 -10	dB	Tx enabled Tx disabled
Output Voltage Transient Tx enable / Tx disable	- -	- 4	100 7	mVp-p	0 dB attenuator setting 24 dB attenuator setting

Note: As measured in ANADIGICS test fixture

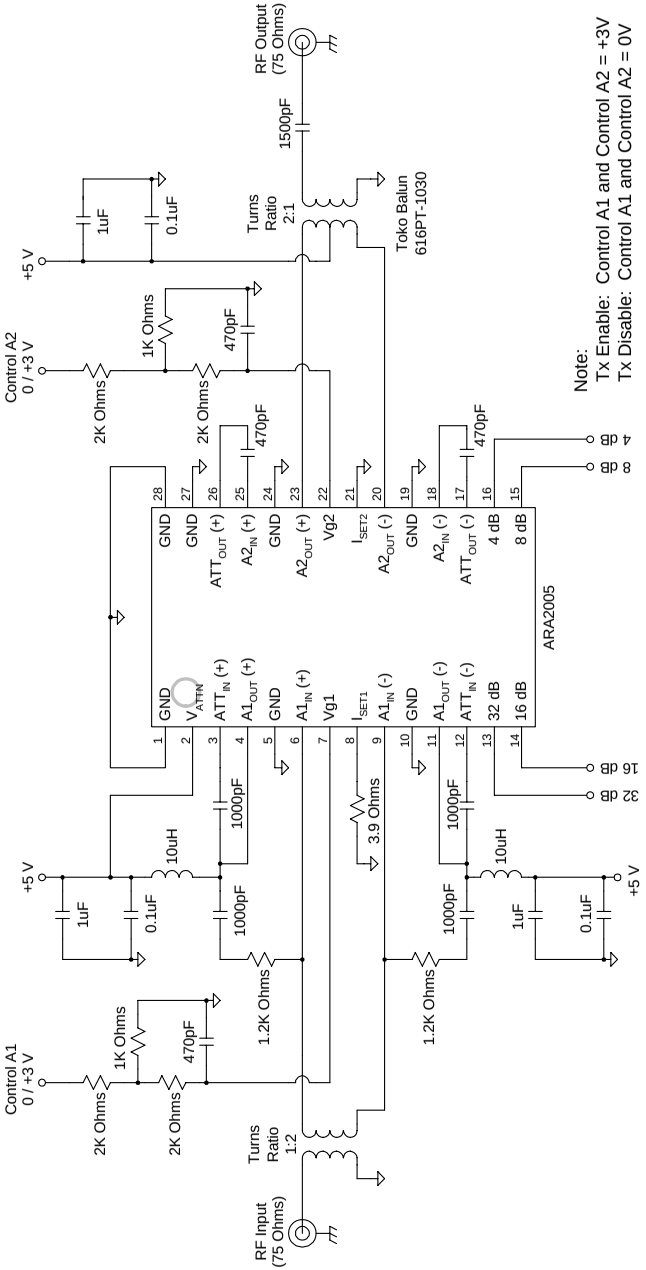


Figure 4: Test Circuit

PERFORMANCE DATA

Figure 5: Gain & Noise Figure vs Frequency

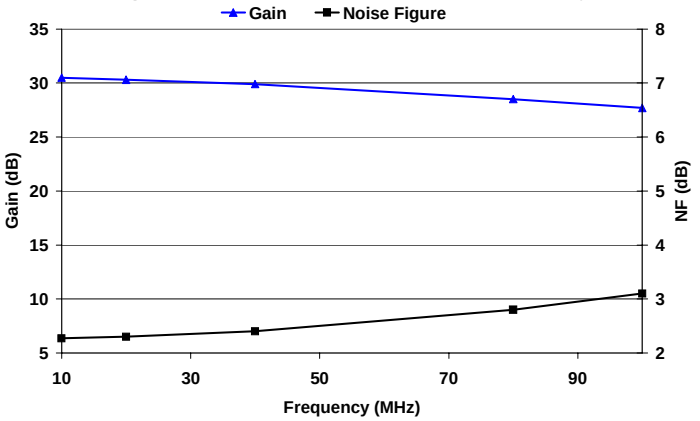


Figure 6: Gain & Noise Figure vs V_{DD}

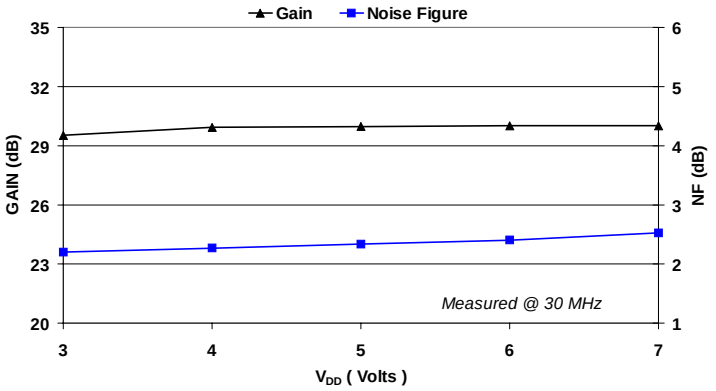


Figure 7: Gain & Noise Figure vs Temperature

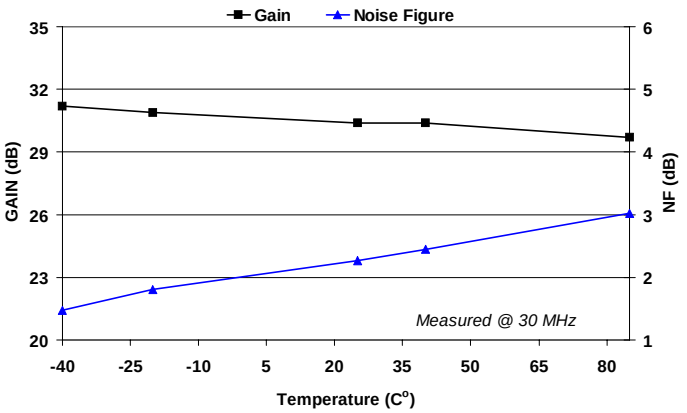


Figure 8: Harmonic Distortion vs V_{DD}
P_{OUT} = 58dBmV

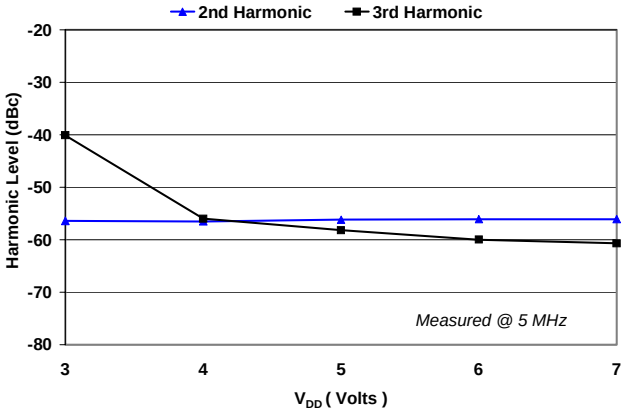


Figure 9: Harmonic Distortion vs V_{DD}
P_{OUT} = 58dBmV

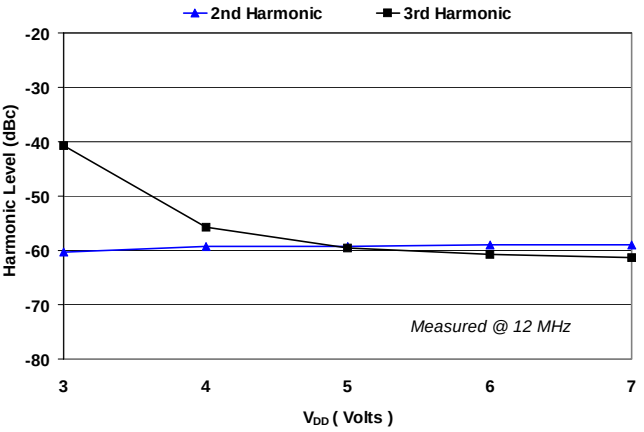


Figure 10: Harmonic Distortion vs Temperature
P_{OUT} = 58dBmV

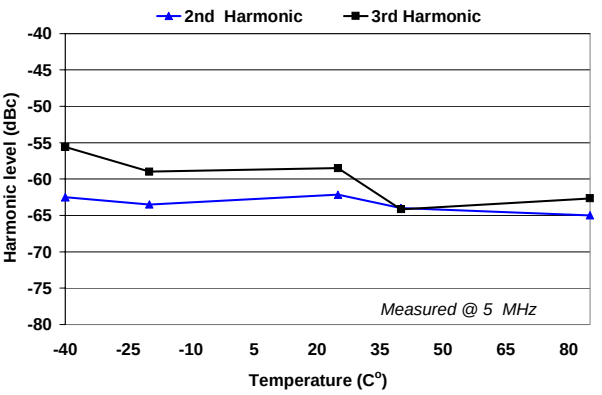


Figure 11: Harmonic Distortion vs Power Out

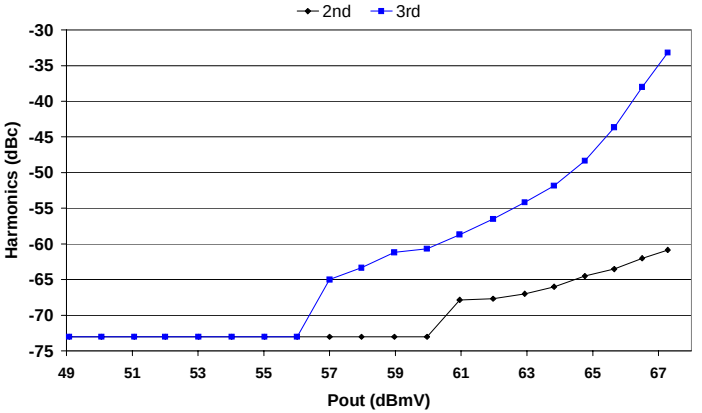


Figure 12: Transients vs Attenuation
POUT = 55dBmV at 0dB attenuation

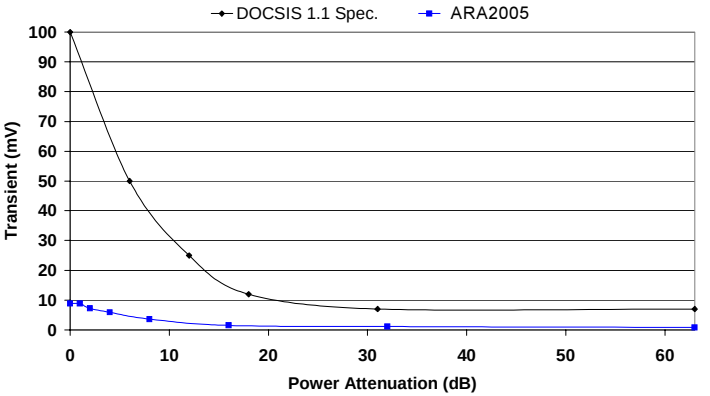


Figure 13: Harmonic Performance over Frequency POUT = +62dBmV

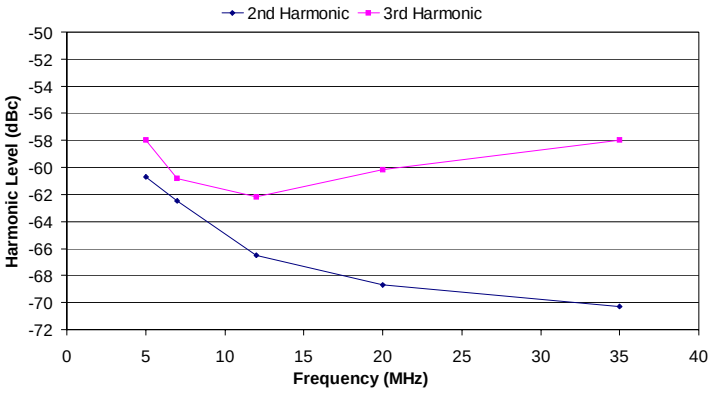


Figure 14: IIP_2 & IIP_3 vs Frequency

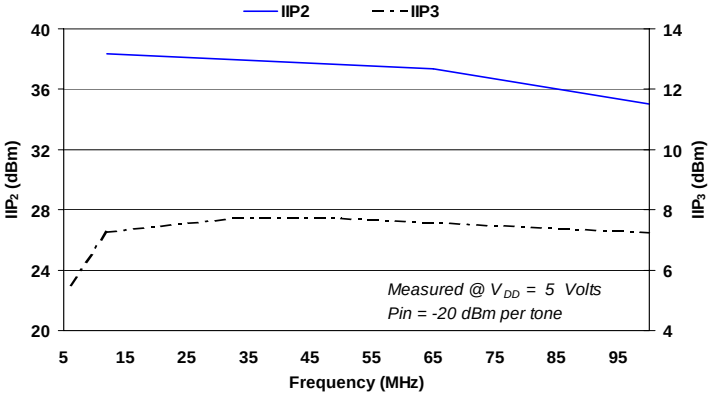
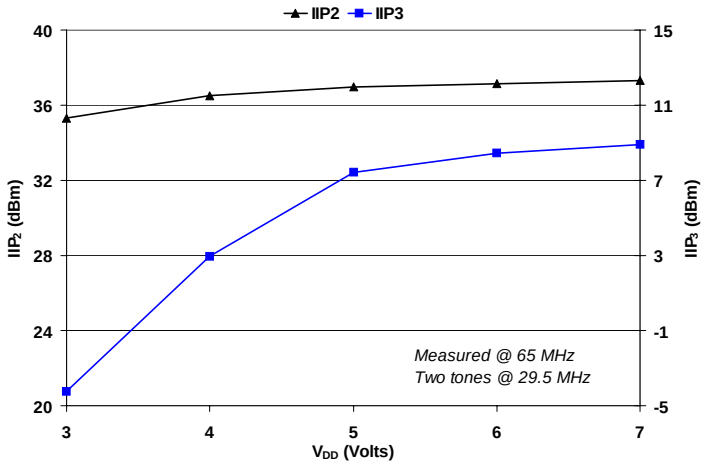


Figure 15: IIP_2 & IIP_3 vs V_{DD}



APPLICATION INFORMATION

Transmit Enable / Disable

The ARA2005 includes two amplification stages that each can be shut down through external control pins Vg1 and Vg2 (pins 7 and 22, respectively.) By applying a slightly positive bias of typically +1.0 Volts, the amplifier is enabled. In order to disable the amplifier, the control pin needs to be pulled to ground.

A practical way to implement the necessary control is to use bias resistor networks similar to those shown in the test circuit schematic (Figure 4.) Each network includes a resistor shunted to ground that serves as a pull-down to disable the amplifier when no control voltage is applied. When a positive voltage is applied, the network acts as a voltage divider that presents the required +1.0 Volts to enable the amplifier. By selecting different resistor values for the voltage divider, the network can accommodate different control voltage inputs.

The Vg1 and Vg2 pins may be connected together directly, and controlled through a single resistor network from a common control voltage.

Amplifier Bias Current

The ISET pins (8 and 21) set the bias current for the amplification stages. Grounding these pins results in the maximum possible current. By placing a resistor from the pin to ground, the current can be reduced. The recommended bias conditions use the configuration shown in the test circuit schematic in Figure 4.

Attenuator Control

Each of the four internal attenuation stages of the ARA2005 is controlled by a TTL-compatible logic input at one of the attenuator control pins (13 - 16). A logic high will enable a given attenuator stage, and a logic low will bypass it.

Output Transformer

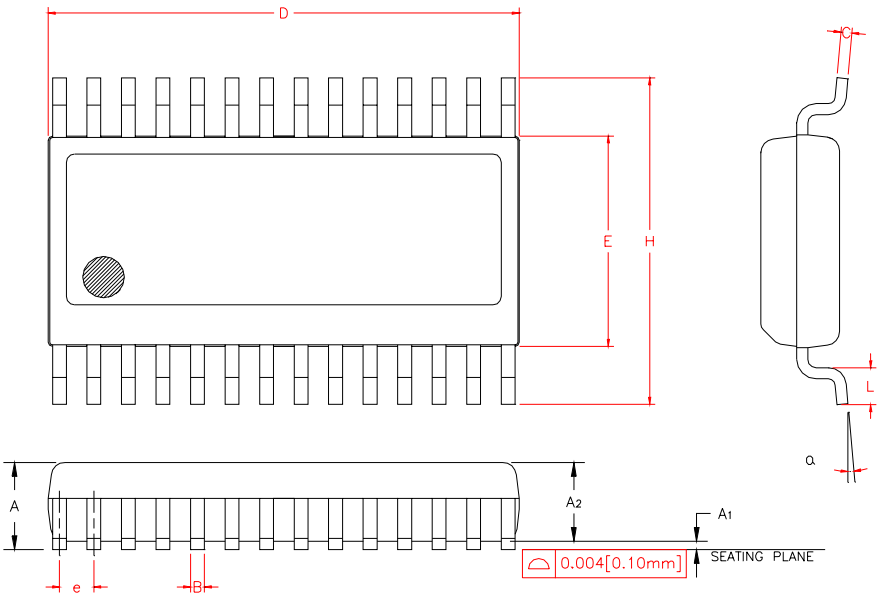
Matching the output of the ARA2005 to a 75 Ohm load is accomplished using a 2:1 turns ratio transformer. In addition to providing an impedance transformation, this transformer provides the bias to the output amplifier stage via the center tap.

The transformer also cancels even mode distortion products and common mode signals, such as the voltage transients that occur while enabling and disabling the amplifiers. As a result, care must be taken when selecting the transformer to be used at the output. It must be capable of handling the RF and DC power requirements without saturating the core, and it must have adequate isolation and good phase and amplitude balance. It also must operate over the desired frequency and temperature range for the intended application.

ESD Sensitivity

Electrostatic discharges can cause permanent damage to this device. Electrostatic charges accumulate on test equipment and the human body, and can discharge without detection. Although the ARA2005 has some built-in ESD protection, proper precautions and handling are strongly recommended. Refer to the ANADIGICS application note on ESD precautions.

PACKAGE OUTLINE



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.053	0.069	1.35	1.75	
A1	0.004	0.010	0.10	0.25	
A2	–	0.059	–	1.50	
B	0.008	0.012	0.20	0.30	
C	0.007	0.010	0.18	0.25	
D	0.386	0.394	9.80	10.00	2
E	0.150	0.157	3.81	3.98	3
e	0.025 BSC		0.64 BSC		4
H	0.228	0.244	5.79	6.19	
L	0.016	0.050	0.40	1.27	
α	0°	8°	0°	8°	

NOTES:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE ±0.0035 [0.089mm].
5. REFERENCE JEDEC MO-137 AF.

Figure 16: S8 Package Outline - 28 Pin SSOP

COMPONENT PACKAGING

Volume quantities of the ARA2005 are supplied on tape and reel. Each reel holds 3,500 pieces. Smaller quantities are available in plastic tubes of 50 pieces.

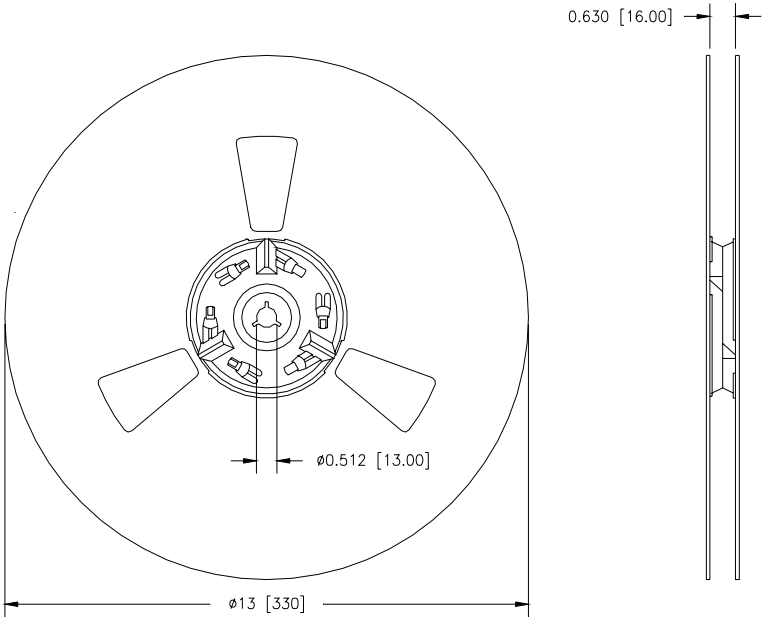


Figure 17: Reel Dimensions

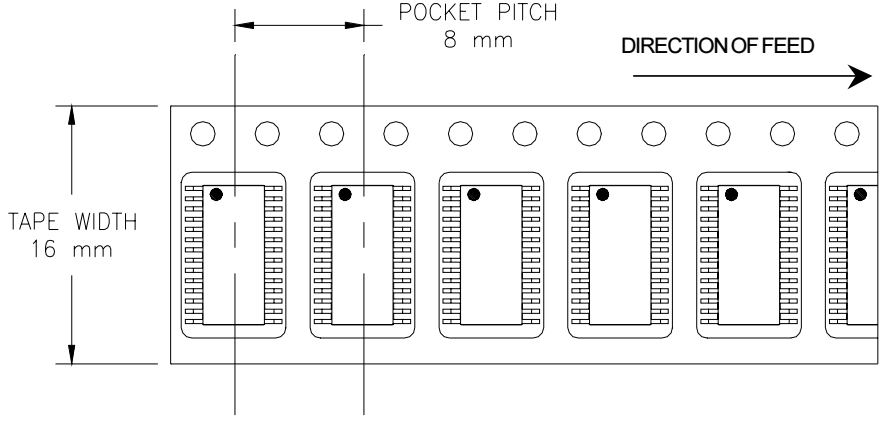


Figure 18: Tape Dimensions

NOTES

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ARA2005S8P1	-40 to 85 ^{0}C	28 Pin SSOP	3,500 piece tape and reel
ARA2005S8P0	-40 to 85 ^{0}C	28 Pin SSOP	Plastic tubes (50 pieces per tube)

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