

Features

- Full TCGA V1.1b Compatibility
- Single Chip Turnkey Solution
- Hardware Asymmetric Crypto Engine
- 2048 RSA Sign in 500 ms Using CRT
- AVR 8-bit RISC Microprocessor
- Internal EEPROM Storage for 10+ RSA Keys
- 33 MHz LPC (Low Pin Count) Bus for Easy PC Interface
- Tamper Detectors for Physical or Environmental Attacks
- Secure Hardware and Firmware Design and Chip Layout
- True Random Number Generator (RNG)
- Secure Real-time Clock Option
- 3.3V \pm 10% Supply Voltage
- 28-lead TSSOP Package
- 0–70°C Temperature Range

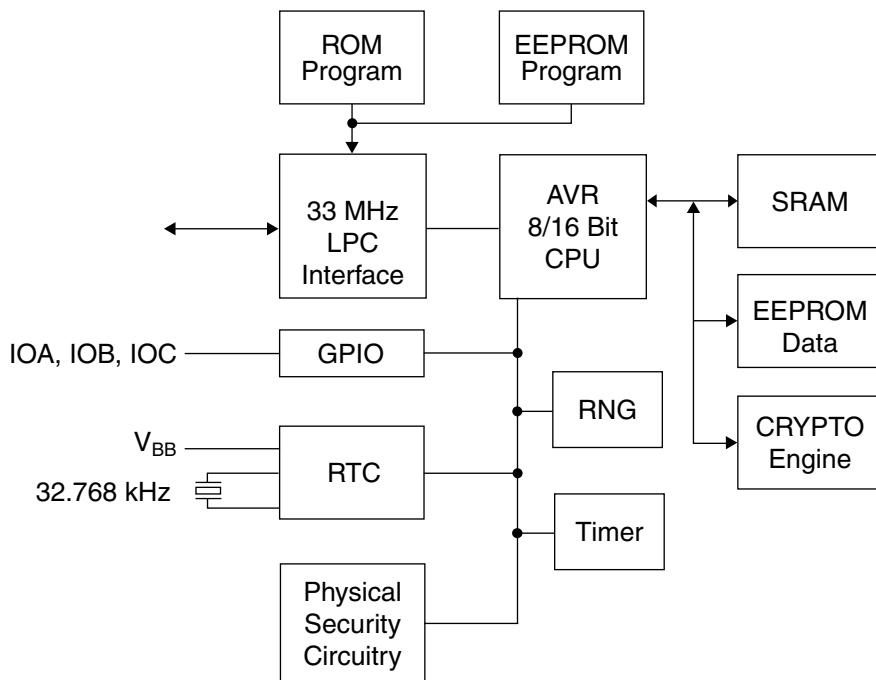
Description

The AT97SC3201 is a fully integrated security module designed to be integrated into personal computers and other embedded systems. It implements version 1.1b of the Trusted Computing Platform Alliance (TCGA) specification for Trusted Platform Modules (TPM).

The TPM includes a crypto accelerator capable of computing a 2048-bit RSA signature in 500 ms, and a 1024-bit RSA signature in 100 ms, both using CRT.

The chip communicates with the PC through the LPC interface, which runs at 33 MHz. In addition, it supports SIRQ (for interrupts) and CLKRUN (to permit clock stopping).

Figure 1. AT97SC3201 Block Diagram



The chip includes a full hardware random number generator that is used for the TCGA protocol and is also available to the system for any random numbers it may need during normal operation.



Trusted Platform Module

AT97SC3201

Summary

Rev. 2015AS–TCGA–07/02



Note: This is a summary document. A complete document is available under NDA. For more information, please contact your local Atmel sales office.



A real-time clock function is available using an external battery and crystal. The chip provides tamper detection if the battery or crystal is removed or tampered with, and the current time value can be signed by the appropriate internal keys to verify its accuracy. (Contact Atmel for current status of this option.)

The battery detector can be used without the crystal for lower cost. In this mode, the TPM can indicate to the system if it has been removed from the PC in any way and also take actions internally.

The chip uses a dynamic internal memory management scheme to store from 10 to 20 keys. Other than the standard TCGA commands (TPM_Evictkey, TPM_Loadkey), no system intervention is required to manage this internal key cache.

The TPM is offered to OEM manufacturers as a turnkey solution, including the firmware integrated on the chip. In addition, Atmel provides the necessary driver software for integration into certain operating systems, along with BIOS drivers. (Contact Atmel for a complete list of operating systems supported.)

Full documentation for TCGA primitives can be found on the TCGA web site, www.trustedcomputing.org. This specification includes only mechanical, electrical and LPC protocol information.

Absolute Maximum Ratings

Operating Temperature.....0°C to +70°C
 Storage Temperature (without Bias).....0°C to + 70°C
 Voltage on I/O Pins.....-0.1 to $V_{CC} + 0.3V$
 Voltage on VCC with Respect to Ground.....6.0V
 Maximum ESD Voltage.....2000V

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification may cause temporary or permanent failure. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1. DC Parameters

$V_{CC} = 3.0$ to $3.6V$; Temperature = 0 to $70^{\circ}C$

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	
I_{CC}	Operating Current at fclk = 33 MHz		25	50	mA	Note 1
I_{SB}	Standby Current, Chip Idle			100	μA	Note 1
I_{BB}	Battery Current		2	4	μA	Note 1. $V_{CC} = 0V$. fxtal = 0.
I_{LIO}	Input Leakage		0.1	3	μA	$V_{in} = V_{CC}$ or GND
V_{IH}	Input High Threshold	$0.5 \times V_{CC}$		$V_{CC} + 0.5$	V	
V_{IL}	Input Low Threshold	-0.5		$0.3 \times V_{CC}$	V	
V_{OH}	Output High Voltage	$0.9 \times V_{CC}$			V	At $I_{OUT} = -500 \mu A$
V_{OL}	Output Low Voltage			$0.1 \times V_{CC}$	V	At $I_{OUT} = 1.5 mA$
I_{OH}		-24			mA	$V_{OUT} = .3 V_{CC}$
I_{OH}		-0.5			mA	$V_{OUT} = .9 V_{CC}$
I_{OH}				116	mA	$V_{OUT} = .7 V_{CC}$
I_{OL}		30			mA	$V_{OUT} = .6 V_{CC}$
I_{OL}		1.9			mA	$V_{OUT} = .1 V_{CC}$
I_{OL}				113	mA	$V_{OUT} = .18 V_{CC}$
I_{OLCR}	Output Low Current, CLKRUN#	7			mA	At $V_{OUT} = .615 \times V_{CC}$
C_I	Input Pin Capacitance		6		pF	Note 2

- Notes: 1. Values listed are advance information and are likely to change as production silicon is characterized.
 2. These parameters guaranteed but not tested.

Table 2. AC Parameters

 Cl = 10 pf. V_{CC} = 3.0 to 3.7V; Temperature = 0 to 70°C

Symbol	Parameter	Min	Nom	Max	Units	Notes
T _{VAL}	CLK to Signal Valid Delay – LAD0-3	2		11	ns	Measured at V _{rise} = 0.285 * V _{CC} and V _{fall} = 0.615 * V _{CC} . Measured from clk at V _{test} = 0.4 * V _{CC} .
T _{ON}	Float to Active Delay	2			ns	
T _{OFF}	Active to Float Delay			28	ns	
T _{SU}	Input Setup Time to CLK	7			ns	
T _H	Input Hold Time from CLK	0			ns	
T _{RST}	Reset Active Time After Power Stable	1			ms	Note 2
T _{RST-CLK}	Reset Active After CLK Stable	100			m	Note 2
T _{RST-OFF}	Reset Active to Output Float Delay			40	ns	Note 2
T _{RHFF}	RST# High to First FRAME# Assertion			500	clocks	
T _{CLKIN}	CLK Period	29.5	30	31	ns	Note 3
T _{CLKLO}	CLK Low Duration	13.4		18	ns	Note 1, Note 3
T _{CLKHI}	CLK High Duration	13.4		18	ns	Note 1, Note 3

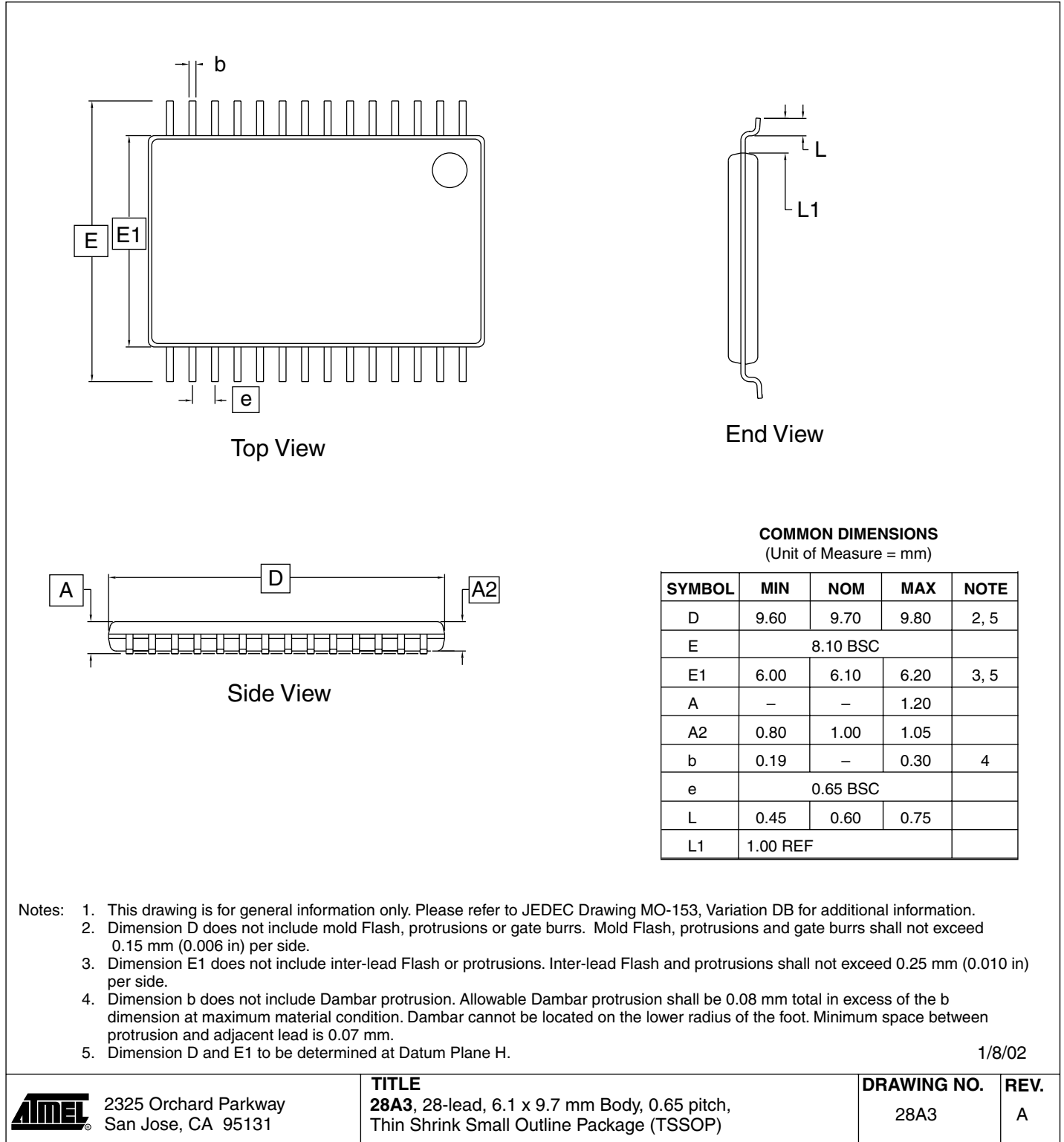
- Note:
1. All parameters measured with respect to signal crossing V_{test} = 0.4 * V_{CC} unless otherwise noted.
 2. These parameters guaranteed but not tested.
 3. The minimum parameter must never be violated under any circumstances unless I_{reset#} is asserted. If proper CLKRUN# signaling is observed, the maximum specification can be violated.

Table 3. Ordering Information

Ordering Code	Package	Operation Range
AT97SC3201-01AC	28A	Commercial (0° to 70° C)

Package Drawing

Figure 2. 28A3 – TSSOP





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