



CYPRESS

CY2277A

Pentium®/II, 6x86, K6 Clock Synthesizer/Driver for Desktop/ Mobile PCs with Intel 82430TX and 2 DIMMs or 3 SO-DIMMs

Features

- Mixed 2.5V and 3.3V operation
Complete clock solution to meet requirements of Pentium®, Pentium® II, 6x86, or K6 motherboards
Four CPU clocks at 2.5V or 3.3V
Up to eight 3.3V SDRAM clocks
Seven 3.3V synchronous PCI clocks, one free running
Two 3.3V USB/IO clocks at 48 or 24 MHz, selectable by serial interface
One 2.5V IOAPIC clock at 14.318 MHz
Two 3.3V Ref. clocks at 14.318 MHz
Factory-EPROM programmable CPU, PCI, and USB/IO clock frequencies for custom configuration
Factory-EPROM programmable output drive and slew rate for EMI customization
MODE Enable pin for CPU\_STOP and PCI\_STOP
I²C™ serial configuration interface
Available in space-saving 48-pin SSOP and TSSOP packages.

Functional Description

The CY2277A is a Clock Synthesizer/Driver for Pentium, Pentium II, 6X86, and K6 portable PCs designed with the Intel® 82430TX or similar chipsets. There are three available options as shown in the selector guide

The CY2277A outputs four CPU clocks at 2.5V or 3.3V with up to nine selectable frequencies. There are up to eight 3.3V SDRAM clocks and seven PCI clocks, running at one half the CPU clock frequency. One of the PCI clocks is free-running. Additionally, the part outputs two 3.3V USB/IO clocks at 48 MHz or 24 MHz, one 2.5V IOAPIC clock at 14.318 MHz, and two 3.3V reference clocks at 14.318 MHz. The CPU, PCI, USB,

and IO clock frequencies are factory-EPROM programmable for easy customization with fast turnaround times.

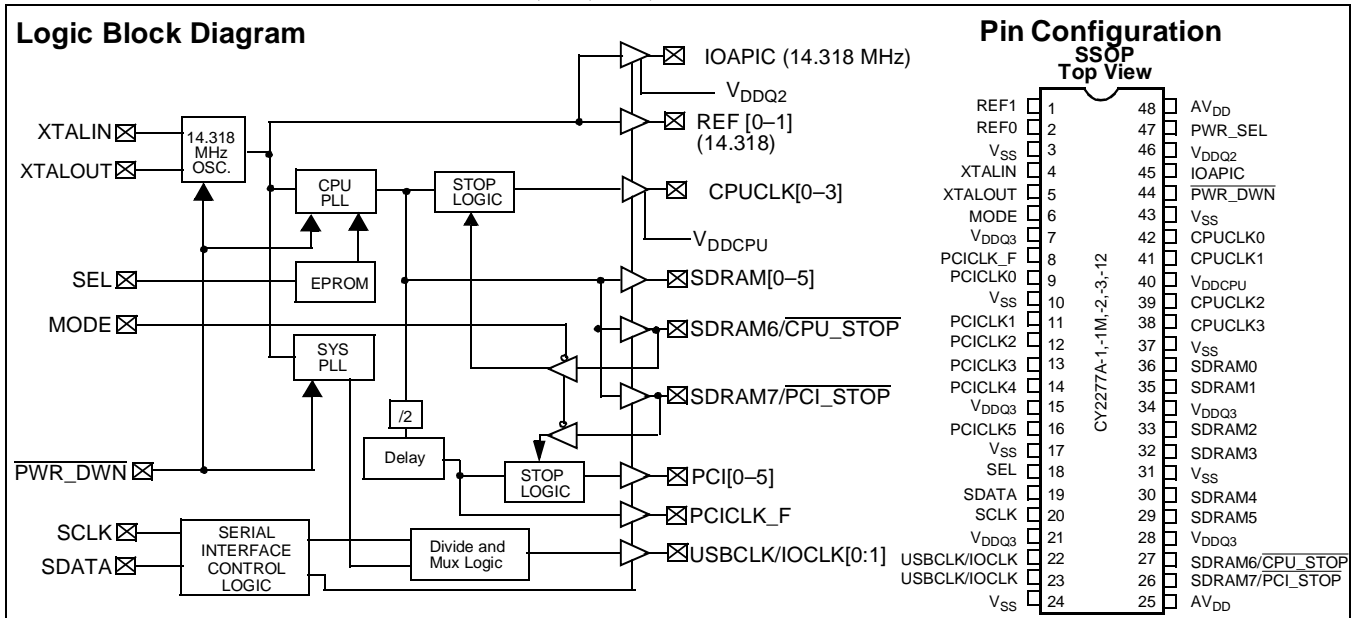
The CY2277A has power-down, CPU stop and PCI stop pins for power management control. The CPU stop and PCI stop are controlled by the MODE pin. They are multiplexed with SDRAM clock outputs, and are selected when the MODE pin is driven LOW. Additionally, these inputs are synchronized on-chip, enabling glitch-free transitions. When the CPU\_STOP input is asserted, the CPU outputs are driven LOW. When the PCI\_STOP input is asserted, the PCI outputs (except the free-running PCI clock) are driven LOW. Finally, when the PWR\_DWN pin is asserted, the reference oscillator and PLLs are shut down, and all outputs are driven LOW.

The CY2277A outputs are designed for low EMI emission. Controlled rise and fall times, unique output driver circuits and factory-EPROM programmable output drive and slew-rate enable optimal configurations for EMI control.

CY2277A Selector Guide

Table with 5 columns: Clock Outputs, -1/-1M, -2, -3, -12. Rows include CPU (60, 66.6MHz), CPU (33.3, 66.6MHz), CPU (I²C selectable), PCI (CPU/2), SDRAM, USB/IO (48 or 24MHz), IOAPIC (14.318 MHz), Ref (14.318MHz), and CPU-PCI delay.

Note: 1. One free-running PCI clock.



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**Pin Summary**

Name	Pins	Description
V <sub>DDQ3</sub>	7, 15, 21, 28, 34	3.3V Digital voltage supply
V <sub>DDQ2</sub>	46	IOAPIC Digital voltage supply, 2.5V
V <sub>DDCPU</sub>	40	CPU Digital voltage supply, 2.5V or 3.3V
A <sub>V</sub> <sub>DD</sub>	25, 48	3.3V Analog voltage supply
V <sub>SS</sub>	3, 10, 17, 24, 31, 37, 43	Ground
XTALIN <sup>[2]</sup>	4	Reference crystal input
XTALOUT <sup>[2]</sup>	5	Reference crystal feedback
MODE	6	Mode select input, enables power management features
SEL	18	Select input to enable 66.66 MHz or 60 MHz CPU clock (See Function tables.)
SDATA	19	I <sup>2</sup> C serial data input for serial configuration port
SCLK	20	I <sup>2</sup> C serial clock input for serial configuration port
PWR_DWN	44	Active low control input to put osc., PLLs, and outputs in power down state
PWR_SEL	47	Power select input, indicates whether V <sub>DDCPU</sub> is at 2.5V or 3.3V HIGH = 3.3V, LOW=2.5V (internal pull-up to V <sub>DD</sub> )
SDRAM7/PCI_STOP	26	SDRAM clock output. Also, active LOW control input to stop PCI clocks, enabled when MODE is LOW
SDRAM6/CPU_STOP	27	SDRAM clock output. Also, active LOW control input to stop CPU clocks, enabled when MODE is LOW
SDRAM[0:5]	36, 35, 33, 32, 30, 29	SDRAM clock outputs, have same frequency as CPU clocks
CPUCLK[0:3]	42, 41, 39, 38	CPU clock outputs
PCICLK[0:5]	9, 11, 12, 13, 14, 16	PCI clock outputs
PCICLK_F	8	PCI clock output, free-running
IOAPIC	45	IOAPIC clock output
REF[0:1]	1, 2	Reference clock outputs, 14.318 MHz. REF0 drives 45 pF load
USBCLK/IOCLK	22, 23	USB or IO clock outputs, frequency selected by serial word

**Note:**

- For best accuracy, use a parallel-resonant crystal, C<sub>LOAD</sub> = 18 pF.

**Function Table (-1, -1M, -12)**

SEL	XTALIN	CPUCLK[0:3] SDRAM[0:7]	PCICLK[0:5] PCICLK_F	REF[0:1] IOAPIC	USBCLK / IOCLK <sup>[3]</sup>
0	14.318 MHz	60.0 MHz	30.0 MHz	14.318 MHz	48.0 MHz / 24.0 MHz
1	14.318 MHz	66.67 MHz	33.33 MHz	14.318 MHz	48.0 MHz / 24.0 MHz

**Function Table (-3)**

SEL	XTALIN	CPUCLK[0:3] SDRAM[0:7]	PCICLK[0:5] PCICLK_F	REF[0:1] IOAPIC	USBCLK / IOCLK <sup>[3]</sup>
0	14.318 MHz	33.33 MHz	16.67 MHz	14.318 MHz	48.0 MHz / 24.0 MHz
1	14.318 MHz	66.67 MHz	33.33 MHz	14.318 MHz	48.0 MHz / 24.0 MHz

**Function Table (-2)<sup>[4, 5]</sup>**

Pin 18	I <sup>2</sup> C Control - Byte 0 <sup>[7]</sup>			Outputs (MHz)			
SEL <sup>[6]</sup>	Bit 6	Bit 5	Bit 4	CPU Freq (Target)	PCI Freq (CPU/2)	CPU Freq (Actual)	PPM
0	0	0	0	66.8	33.4	66.818	272
0	0	0	1	75.0	37.5	75.000	0
0	0	1	0	60.0	30.0	60.000	0
0	0	1	1	55.0	27.5	55.012	217
0	1	0	0	68.4	34.2	68.409	133
0	1	0	1	50.0	25.0	49.947	1057
0	1	1	0	83.3	41.65	83.306	69
0	1	1	1	33.3	16.67	33.298	1107
1	0	0	0	68.4	34.2	68.409	133
1	0	0	1	50.0	25.0	49.947	1057
1	0	1	0	83.3	41.65	83.306	69
1	0	1	1	33.3	16.67	33.298	1107
1	1	0	0	66.8	33.4	66.818	272
1	1	0	1	75.0	37.5	75.000	0
1	1	1	0	60.0	30.0	60.000	0
1	1	1	1	55.0	27.5	55.012	217

**Actual Clock Frequency Values (-1, -1M, -3, -12)**

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK, SDRAM	66.67	66.654	-195
CPUCLK, SDRAM	60.0	60.0	0
USBCLK <sup>[8]</sup>	48.0	48.008	167
IOCLK	24.0	24.004	167

**CPU and PCI Clock Driver Strengths**

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V

**Notes:**

3. On power-up, the default frequency on these outputs is 48 MHz.
4. All AC specs for duty cycle, skew, jitter, and rise/fall time remain the same.
5. The above frequencies support Intel Pentium and Pentium II, AMD K6, and Cyrix processors.
6. SEL = 0 OR SEL = 1 gives all the same CPU frequencies on the outputs. In this case, the CPU and PCI frequencies are I<sup>2</sup>C controllable. Therefore, the user can have jumperless frequency changes.
7. The above I<sup>2</sup>C bits will NOT affect the other clocks in the system.
8. Meets Intel USB clock requirements.

**Power Management Logic**

CPU_STOP	PCI_STOP	PWR_DWN	CPUCLK	PCICLK	PCICLK_F	Other Clocks	Osc.	PLLs
X	X	0	Low	Low	Stopped	Stopped	Off	Off
0	0	1	Low	Low	Running	Running	Running	Running
0	1	1	Low	33/30 MHz	Running	Running	Running	Running
1	0	1	66/60 MHz	Low	Running	Running	Running	Running
1	1	1	66/60 MHz	33/30 MHz	Running	Running	Running	Running

**Serial Configuration Map**

- The Serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

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Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to "0".
- I<sup>2</sup>C Address for the CY2277A is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

**Byte 0: Functional and Frequency Select Clock Register (1 = Enable, 0 = Disable)**

Bit	Pin #	Description
Bit 7	--	(Reserved) drive to '0'
Bit 6	--	(Reserved) drive to '0' on -1, -1M, -3, -12
Bit 6	--	Freq. Sel. Bit on -2
Bit 5	--	(Reserved) drive to '0' on -1, -1M, -3, -12
Bit 5	--	Freq. Sel. Bit on -2
Bit 4	--	(Reserved) drive to '0' on -1, -1M, -3, -12
Bit 4	--	Freq. Sel. Bit on -2
Bit 3	23	48/24 MHz (Frequency Select) 1 = 48 MHz (default), 0 = 24 MHz
Bit 2	22	48/24 MHz (Frequency Select) 1 = 48 MHz (default), 0 = 24 MHz
Bit 1	--	Bit 1
Bit 0	--	Bit 0
		1 - Three-State (see table below)
		0 - N/A
		1 - Test Mode (see table below)
		0 - Normal Operation

**Select Functions**

Functional Description	Outputs						
	CPU	PCI, PCI_F	SDRAM	Ref	IOAPIC	IOCLK	USBCLK
Three-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	TCLK/2 <sup>[9]</sup>	TCLK/4	TCLK/2	TCLK	TCLK	TCLK/4	TCLK/2

**Note:**

9. TCLK supplied on the XTALIN, PIN 4.

**Byte 1: CPU, 24/48 MHz Active/Inactive**  
**Register(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	23	48/24 MHz (Active/Inactive)
Bit 6	22	48/24 MHz (Active/Inactive)
Bit 5	--	(Reserved) drive to '0'
Bit 4	N/A	Not Used, drive 0
Bit 3	38	CPUCLK3 (Active/Inactive)
Bit 2	39	CPUCLK2 (Active/Inactive)
Bit 1	41	CPUCLK1 (Active/Inactive)
Bit 0	42	CPUCLK0 (Active/Inactive)

**Byte 2: PCI Active/Inactive**  
**Register(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	--	(Reserved) drive to '0'
Bit 6	8	PCICLK_F (Active/Inactive)
Bit 5	16	PCICLK5 (Active/Inactive)
Bit 4	14	PCICLK4 (Active/Inactive)
Bit 3	13	PCICLK3 (Active/Inactive)
Bit 2	12	PCICLK2 (Active/Inactive)
Bit 1	11	PCICLK1 (Active/Inactive)
Bit 0	9	PCICLK0 (Active/Inactive)

**Byte 3: SDRAM Active/Inactive**  
**Register(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	26	SDRAM7 (Active/Inactive)
Bit 6	27	SDRAM6 (Active/Inactive)
Bit 5	29	SDRAM5 (Active/Inactive)
Bit 4	30	SDRAM4 (Active/Inactive)
Bit 3	32	SDRAM3 (Active/Inactive)
Bit 2	33	SDRAM2 (Active/Inactive)
Bit 1	35	SDRAM1 (Active/Inactive)
Bit 0	36	SDRAM0 (Active/Inactive)

**Byte 4: SDRAM Active/Inactive**  
**Register(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	N/A	Not used, drive to '0'
Bit 6	N/A	Not used, drive to '0'
Bit 5	N/A	Not used, drive to '0'
Bit 4	N/A	Not used, drive to '0'
Bit 3	N/A	Not used, drive to '0'
Bit 2	N/A	Not used, drive to '0'
Bit 1	N/A	Not used, drive to '0'
Bit 0	N/A	Not used, drive to '0'

**Byte 5: Peripheral Active/Inactive**  
**Register(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	--	(Reserved) drive to '0'
Bit 6	--	(Reserved) drive to '0'
Bit 5	--	(Reserved) drive to '0'
Bit 4	45	IOAPIC (Active/Inactive)
Bit 3	--	(Reserved) drive to '0'
Bit 2	--	(Reserved) drive to '0'
Bit 1	1	REF1 (Active/Inactive)
Bit 0	2	REF0 (Active/Inactive)

**Byte 6: Reserved, for future use**
**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... -0.5 to +7.0V  
 Input Voltage ..... -0.5V to  $V_{DD}+0.5$   
 Storage Temperature (Non-Condensing).... -65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C  
 Junction Temperature ..... +150°C  
 Package Power Dissipation ..... 1W  
 Static Discharge Voltage ..... >2000V  
 (per MIL-STD-883, Method 3015, like  $V_{DD}$  pins tied together)

**Operating Conditions<sup>[10]</sup>**

Parameter	Description	Min.	Max.	Unit
AV <sub>DD</sub> , V <sub>DDQ3</sub>	Analog and Digital Supply Voltage	3.135	3.465	V
V <sub>DDCPU</sub>	2.5V CPU Supply Voltage (-1, -1M, -2, -3) 2.5V CPU Supply Voltage (-12) 3.3V CPU Supply Voltage	2.375 2.375 3.135	2.9 2.625 3.465	V
V <sub>DDQ2</sub>	2.5V IOAPIC Supply Voltage (-1, -1M, -2, -3) 2.5V IOAPIC Supply Voltage (-12) 3.3V IOAPIC Supply Voltage	2.375 2.375 3.135	2.9 2.625 3.465	V
T <sub>A</sub>	Operating Temperature, Ambient	0	70	°C
C <sub>L</sub>	Max. Capacitive Load on CPUCLK, USBCLK/IOCLK, REF1, IOAPIC PCICLK, SDRAM REF0	10 30, 20 20	20 30 45	pF
f <sub>(REF)</sub>	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

**Electrical Characteristics (-1, -2, -3, -12)**

Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>IH</sub>	High-level Input Voltage	Except Crystal Inputs	2.0		V
V <sub>IL</sub>	Low-level Input Voltage	Except Crystal Inputs		0.8	V
V <sub>ILiic</sub>	Low-level Input Voltage	I <sup>2</sup> C inputs only		0.7	V
V <sub>OH</sub>	High-level Output Voltage <sup>[11]</sup>	V <sub>DDQ2</sub> = V <sub>DDCPU</sub> = 2.375V I <sub>OH</sub> = 18 mA CPUCLK I <sub>OH</sub> = 18 mA IOAPIC	2.0		V
V <sub>OL</sub>	Low-level Output Voltage <sup>[11]</sup>	V <sub>DDQ2</sub> = V <sub>DDCPU</sub> = 2.375V I <sub>OL</sub> = 29 mA CPUCLK I <sub>OL</sub> = 29 mA IOAPIC		0.4	V
V <sub>OH</sub>	High-level Output Voltage <sup>[11]</sup>	V <sub>DDQ3</sub> , AV <sub>DD</sub> , V <sub>DDCPU</sub> = 3.135V I <sub>OH</sub> = 32 mA CPUCLK I <sub>OH</sub> = 36 mA SDRAM I <sub>OH</sub> = 32 mA PCICLK I <sub>OH</sub> = 26 mA USBCLK I <sub>OH</sub> = 26 mA IOCLK I <sub>OH</sub> = 36 mA REF0 I <sub>OH</sub> = 26 mA REF1	2.4		V
V <sub>OL</sub>	Low-level Output Voltage <sup>[11]</sup>	V <sub>DDQ3</sub> , AV <sub>DD</sub> , V <sub>DDCPU</sub> = 3.135V I <sub>OL</sub> = 24 mA CPUCLK I <sub>OL</sub> = 29 mA SDRAM I <sub>OL</sub> = 26 mA PCICLK I <sub>OL</sub> = 21 mA USBCLK I <sub>OL</sub> = 21 mA IOCLK I <sub>OL</sub> = 29 mA REF0 I <sub>OL</sub> = 21 mA REF1		0.4V	V
I <sub>IH</sub>	Input High Current	V <sub>IH</sub> = V <sub>DD</sub>	-10	+10	μA
I <sub>IL</sub>	Input Low Current	V <sub>IL</sub> = 0V, except PWR_SEL		10	μA
I <sub>IL</sub>	Input Low Current	V <sub>IL</sub> = 0V, PWR_SEL only		100	μA
I <sub>OZ</sub>	Output Leakage Current	Three-state	-10	+10	μA
I <sub>DD</sub>	Power Supply Current <sup>[11, 12]</sup>	V <sub>DD</sub> = 3.465V, V <sub>IN</sub> = 0 or V <sub>DD</sub> , Loaded Outputs, CPU = 66.67 MHz		250	mA
I <sub>DD</sub>	Power Supply Current <sup>[11, 12]</sup>	V <sub>DD</sub> = 3.465V, V <sub>IN</sub> = 0 or V <sub>DD</sub> , Unloaded Outputs		120	mA
I <sub>DDS</sub>	Power-down Current	Current draw in power-down state, PWR_SEL = V <sub>DD</sub>		150	μA

**Notes:**

10. Electrical parameters are guaranteed with these operating conditions.
11. Guaranteed by design and characterization. Not 100% tested in production.
12. Power supply current will vary with number of outputs which are running.

**Electrical Characteristics (-1M)**

Parameter	Description	Test Conditions	Min.	Max.	Unit	
V <sub>IH</sub>	High-level Input Voltage	Except Crystal Inputs	2.0		V	
V <sub>IL</sub>	Low-level Input Voltage	Except Crystal Inputs		0.8	V	
V <sub>ILiic</sub>	Low-level Input Voltage	I <sup>2</sup> C inputs only		0.7	V	
V <sub>OH</sub>	High-level Output Voltage <sup>[11]</sup>	V <sub>DDQ2</sub> = V <sub>DDCPU</sub> = 2.375V	I <sub>OH</sub> = 12.6 mA	CPUCLK	2.0	V
			I <sub>OH</sub> = 16.7 mA	IOAPIC		
V <sub>OL</sub>	Low-level Output Voltage <sup>[11]</sup>	V <sub>DDQ2</sub> = V <sub>DDCPU</sub> = 2.375V	I <sub>OL</sub> = 18.2 mA	CPUCLK		0.4
			I <sub>OL</sub> = 23.1 mA	IOAPIC		
V <sub>OH</sub>	High-level Output Voltage <sup>[11]</sup>	V <sub>DDQ3</sub> , AV <sub>DD</sub> , V <sub>DDCPU</sub> = 3.135V	I <sub>OH</sub> = 32.2 mA	SDRAM	2.4	V
			I <sub>OH</sub> = 32.2 mA	PCICLK		
			I <sub>OH</sub> = 32.2 mA	USBCLK		
			I <sub>OH</sub> = 32.2 mA	IOCLK		
			I <sub>OH</sub> = 32.2 mA	REF0		
			I <sub>OH</sub> = 32.2 mA	REF1		
V <sub>OL</sub>	Low-level Output Voltage <sup>[11]</sup>	V <sub>DDQ3</sub> , AV <sub>DD</sub> , V <sub>DDCPU</sub> = 3.135V	I <sub>OL</sub> = 23.8 mA	SDRAM		0.4V
			I <sub>OL</sub> = 23.8 mA	PCICLK		
			I <sub>OL</sub> = 23.8 mA	USBCLK		
			I <sub>OL</sub> = 23.8 mA	IOCLK		
			I <sub>OL</sub> = 23.8 mA	REF0		
			I <sub>OL</sub> = 23.8 mA	REF1		
I <sub>IH</sub>	Input High Current	V <sub>IH</sub> = V <sub>DD</sub>	-10	+10	μA	
I <sub>IL</sub>	Input Low Current	V <sub>IL</sub> = 0V, except PWR_SEL		10	μA	
I <sub>IL</sub>	Input Low Current	V <sub>IL</sub> = 0V, PWR_SEL only		100	μA	
I <sub>OZ</sub>	Output Leakage Current	Three-state	-10	+10	μA	
I <sub>DD</sub>	Power Supply Current <sup>[11, 12]</sup>	V <sub>DD</sub> = 3.465V, V <sub>IN</sub> = 0 or V <sub>DD</sub> , Loaded Outputs, CPU = 66.67 MHz		250	mA	
I <sub>DD</sub>	Power Supply Current <sup>[11, 12]</sup>	V <sub>DD</sub> = 3.465V, V <sub>IN</sub> = 0 or V <sub>DD</sub> , Unloaded Outputs		120	mA	
I <sub>DDs</sub>	Power-down Current	Current draw in power-down state, PWR_SEL = V <sub>DD</sub>		150	μA	

**Switching Characteristics (-1, -3)** [11, 13, 15]

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>1</sub>	CPUCLK SDRAM USBCLK IOCLK REF [0,1] IOAPIC	Output Duty Cycle <sup>[14]</sup>	t <sub>1</sub> = t <sub>1A</sub> ÷ t <sub>1B</sub>	45	50	55	%
t <sub>1</sub>	PCI	Output Duty Cycle <sup>[14]</sup>	t <sub>1</sub> = t <sub>1A</sub> ÷ t <sub>1B</sub>	40	50	55	%
t <sub>2</sub>	CPUCLK, IOAPIC	CPU and IOAPIC Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V CPU clocks at 66.66 MHz	0.75 0.75		4.0 4.0	V/ns
t <sub>2</sub>	PCI	PCI Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V	0.75		4.0	V/ns
t <sub>2</sub>	USBCLK, IOCLK, REF0	USB, I/O, REF0 Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.8		4.0	V/ns
t <sub>2</sub>	SDRAM	SDRAM Rising and Fall- ing Edge Rate	Between 0.4V and 2.4V SDRAM clocks at 66.66 MHz	1.0		4.0	V/ns
t <sub>2</sub>	REF1	REF1 Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.5		2.0	V/ns
t <sub>3</sub>	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V	0.4 0.5		2.13 2.0	ns
t <sub>3</sub>	USBCLK, IOCLK	USB Clock and I/O Clock Rise Time	Between 0.4V and 2.4V			2.5	ns
t <sub>4</sub>	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V, V <sub>DDCPU</sub> = 2.5V Between 2.4V and 0.4V, V <sub>DDCPU</sub> = 3.3V	0.4 0.5		2.13 2.0	ns
t <sub>4</sub>	USBCLK, IOCLK	USB Clock and I/O Clock Fall Time	Between 2.4V and 0.4V			2.5	ns
t <sub>5</sub>	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V, V <sub>DDCPU</sub> = 2.5V		100	400	ps
t <sub>6</sub>	CPUCLK, PCICLK	CPU-PCI Clock Skew (-1, -3)	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.0	2.0	6.0	ns
t <sub>7</sub>	CPUCLK, SDRAM	CPU-SDRAM Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks, V <sub>DDCPU</sub> = 2.5V			775	ps
t <sub>8</sub>	CPUCLK	Cycle-Cycle Clock Jitter	Measured at 1.25V for 2.5V clocks and at 1.5V for 3.3V clocks			450	ps
t <sub>8</sub>	SDRAM	Cycle-Cycle Clock Jitter	Measured at 1.5V for 3.3V clocks			650	ps
t <sub>8</sub>	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			500	ps
t <sub>8</sub>	USBCLK, IOCLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			1.3	ns
t <sub>9</sub>	CPUCLK, PCICLK, SDRAM	Power-up Time	CPU, PCI, and SDRAM clock stabiliza- tion from power-up			3	ms
t <sub>10</sub>	CPU, PCI, SDRAM	Frequency Slew Rate	Rate of change of frequency		2		MHz/ ms

**Notes:**

13. All parameters specified with loaded outputs.
14. Duty cycle is measured at 1.5V when V<sub>DD</sub> = 3.3V. When V<sub>DDCPU</sub> = 2.5V, CPUCLK duty cycle is measured at 1.25V.
15. Over the operating range unless otherwise specified.



**Switching Characteristics (-1M)** [11, 13, 15]

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>1</sub>	CPUCLK SDRAM USBCLK REF [0,1] IOAPIC	Output Duty Cycle <sup>[14]</sup>	t <sub>1</sub> = t <sub>1A</sub> ÷ t <sub>1B</sub>	45	50	55	%
t <sub>1</sub>	PCI	Output Duty Cycle <sup>[14]</sup>	t <sub>1</sub> = t <sub>1A</sub> ÷ t <sub>1B</sub>	45	50	55	%
t <sub>2</sub>	CPUCLK, IOAPIC	CPU and IOAPIC Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V CPU clocks at 66.66 MHz	0.60		4.0	V/ns
t <sub>2</sub>	PCI	PCI Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V	0.65		4.0	V/ns
t <sub>2</sub>	USBCLK, REF0	USB, REF0 Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.65		4.0	V/ns
t <sub>2</sub>	SDRAM	SDRAM Rising and Fall- ing Edge Rate	Between 0.4V and 2.4V SDRAM clocks at 66.66 MHz	0.70		4.0	V/ns
t <sub>2</sub>	REF1	REF1 Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.5		2.0	V/ns
t <sub>3</sub>	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V	0.4		2.4	ns
t <sub>3</sub>	USBCLK	USB Clock Rise Time	Between 0.4V and 2.0V			2.5	ns
t <sub>4</sub>	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V, V <sub>DDCPU</sub> = 2.5V	0.4		2.4	ns
t <sub>4</sub>	USBCLK	USB Clock Fall Time	Between 2.0V and 0.4V			2.5	ns
t <sub>5</sub>	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V, V <sub>DDCPU</sub> = 2.5V		100	250	ps
t <sub>5</sub>	PCICLK	PCI-PCI Clock Skew	Measured at 1.5V			400	ps
t <sub>5</sub>	SDRAM	SDRAM-SDRAM Clock Skew	Measured at 1.5V			300	ps
t <sub>6</sub>	CPUCLK, PCICLK	CPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.0	2.0	6.0	ns
t <sub>7</sub>	CPUCLK, SDRAM	CPU-SDRAM Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks, V <sub>DDCPU</sub> = 2.5V			600	ps
t <sub>8</sub>	CPUCLK	Cycle-Cycle Clock Jitter	Measured at 1.25V for 2.5V clocks			525	ps
t <sub>8</sub>	SDRAM	Cycle-Cycle Clock Jitter	Measured at 1.5V			600	ps
t <sub>8</sub>	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			400	ps
t <sub>8</sub>	USBCLK, IOCLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			900	ps
t <sub>9</sub>	CPUCLK, PCICLK, SDRAM	Power-up Time	CPU, PCI, and SDRAM clock stabiliza- tion from power-up			3	ms
t <sub>10</sub>	CPU, PCI, SDRAM	Frequency Slew Rate	Rate of change of frequency		2		MHz/ ms

**Switching Characteristics (-2)** [11, 13, 15]

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>1</sub>	CPUCLK SDRAM USBCLK IOCLK REF [0,1] IOAPIC PCI	Output Duty Cycle <sup>[14]</sup>	$t_1 = t_{1A} \div t_{1B}$	40	50	55	%
t <sub>2</sub>	CPUCLK, IOAPIC	CPU and IOAPIC Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V CPU clocks at 66.8 MHz	0.75 0.75		4.0 4.0	V/ns
t <sub>2</sub>	PCI	PCI Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V	0.7		4.0	V/ns
t <sub>2</sub>	USBCLK, IOCLK, REF0	USB, I/O, REF0 Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.8		4.0	V/ns
t <sub>2</sub>	SDRAM	SDRAM Rising and Fall- ing Edge Rate	Between 0.4V and 2.4V SDRAM clocks at 66.8 MHz	1.0		4.0	V/ns
t <sub>2</sub>	REF1	REF1 Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.5		2.0	V/ns
t <sub>3</sub>	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V	0.4 0.5		2.13 2.0	ns
t <sub>3</sub>	USBCLK, IOCLK	USB Clock and I/O Clock Rise Time	Between 0.4V and 2.4V			2.5	ns
t <sub>4</sub>	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V, V <sub>DDCPU</sub> = 2.5V Between 2.4V and 0.4V, V <sub>DDCPU</sub> = 3.3V	0.4 0.5		2.13 2.0	ns
t <sub>4</sub>	USBCLK, IOCLK	USB Clock and I/O Clock Fall Time	Between 2.4V and 0.4V			2.5	ns
t <sub>5</sub>	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V, V <sub>DDCPU</sub> = 2.5V		100	400	ps
t <sub>6</sub>	CPUCLK, PCICLK	CPU-PCI Clock Skew (-2)	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.0	2.0	6.0	ns
t <sub>7</sub>	CPUCLK, SDRAM	CPU-SDRAM Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks, V <sub>DDCPU</sub> = 2.5V			1.3	ns
t <sub>8</sub>	CPUCLK SDRAM	Cycle-Cycle Clock Jitter	Measured at 1.25V for 2.5V clocks and at 1.5V for 3.3V clocks			650	ps
t <sub>8</sub>	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			600	ps
t <sub>8</sub>	USBCLK, IOCLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			1.3	ns
t <sub>9</sub>	CPUCLK, PCICLK, SDRAM	Power-up Time	CPU, PCI, and SDRAM clock stabiliza- tion from power-up			3	ms
t <sub>10</sub>	CPU, PCI, SDRAM	Frequency Slew Rate	Rate of change of frequency		2		MHz/ ms

**Switching Characteristics (-12)** [11, 13, 15, 16]

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>1</sub>	All Clocks	Output Duty Cycle <sup>[14]</sup>	t <sub>1</sub> = t <sub>1A</sub> ÷ t <sub>1B</sub>	45	50	55	%
t <sub>2</sub>	CPUCLK, IOAPIC	CPU and IOAPIC Clock Rising and Falling Edge Rate	Between 0.6V and 1.8V, V <sub>DDCPU</sub> = 2.5V Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V CPU clocks at 66.6 MHz	1.0 1.0		4.0 4.0	V/ns
t <sub>2</sub>	PCI	PCI Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V	1.0		4.0	V/ns
t <sub>2</sub>	REF0	REF0 Clock Rising and Falling Edge Rate	Between 0.8V and 2.4V, V <sub>DDCPU</sub> = 3.3V	1.0		4.0	V/ns
t <sub>2</sub>	SDRAM	SDRAM Rising and Falling Edge Rate	Between 0.5V and 2.0V SDRAM clocks at 66.6 MHz	1.5		4.0	V/ns
t <sub>2</sub>	REF1 USBCLK IOCLK	REF1, USB and IO Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.5		2.0	V/ns
t <sub>3</sub>	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V	0.4 0.4		2.0 2.0	ns
t <sub>3</sub>	USBCLK, IOCLK	USB Clock and I/O Clock Rise Time	Between 0.4V and 2.4V	1.0		4.0	ns
t <sub>4</sub>	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V, V <sub>DDCPU</sub> = 2.5V Between 2.4V and 0.4V, V <sub>DDCPU</sub> = 3.3V	0.4 0.4		2.0 2.0	ns
t <sub>4</sub>	USBCLK, IOCLK	USB Clock and I/O Clock Fall Time	Between 2.4V and 0.4V	1.0		4.0	ns
t <sub>5</sub>	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V, V <sub>DDCPU</sub> = 2.5V		100	250	ps
t <sub>6</sub>	CPUCLK, PCICLK	CPU-PCI Clock Skew (-12)	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.0		4.0	ns
t <sub>7</sub>	CPUCLK, SDRAM	CPU-SDRAM Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks, V <sub>DDCPU</sub> = 2.5V			500	ps
t <sub>8</sub>	CPUCLK	Cycle-Cycle Clock Jitter	Measured at 1.25V for 2.5V clocks and at 1.5V for 3.3V clocks			250	ps
t <sub>8</sub>	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			500	ps
t <sub>9</sub>	CPUCLK, PCICLK, SDRAM	Power-up Time	CPU, PCI, and SDRAM clock stabilization from power-up			3	ms
t <sub>10</sub>	CPU, PCI, SDRAM	Frequency Slew Rate	Rate of change of frequency		2		MHz/ ms

**Note:**

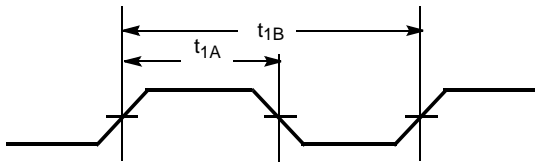
 16. Parameters specified with: V<sub>DDCPU</sub>=2.5V, V<sub>DDQ2</sub>=2.5V, V<sub>DDQ3</sub>=3.3V.

### Timing Requirement for the I<sup>2</sup>C Bus

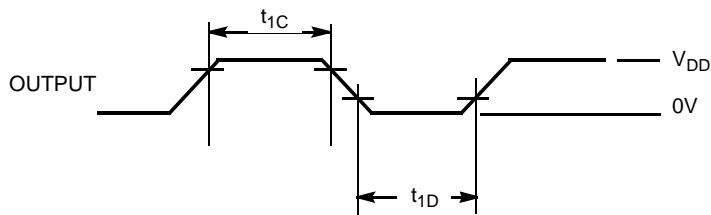
Parameter	Description	Min.	Max.	Unit
t <sub>10</sub>	SCLK Clock Frequency	0	100	kHz
t <sub>11</sub>	Time the bus must be free before a new transmission can start	4.7		μs
t <sub>12</sub>	Hold time start condition. After this period the first clock pulse is generated.	4		μs
t <sub>13</sub>	The LOW period of the clock.	4.7		μs
t <sub>14</sub>	The HIGH period of the clock.	4		μs
t <sub>15</sub>	Setup time for start condition. (Only relevant for a repeated start condition.)	4.7		μs
t <sub>16</sub>	Hold time DATA for CBUS compatible masters. for I <sup>2</sup> C devices	50		μs
t <sub>17</sub>	DATA input set-up time	250		ns
t <sub>18</sub>	Rise time of both SDATA and SCLK inputs		1	μs
t <sub>19</sub>	Fall time of both SDATA and SCLK inputs		300	ns
t <sub>20</sub>	Set-up time for stop condition	4.0		μs

### Switching Waveforms

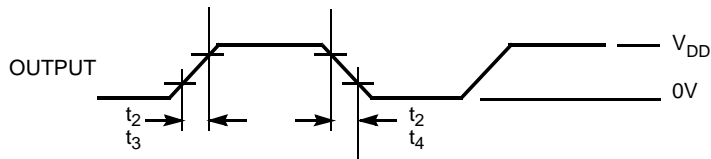
#### Duty Cycle Timing

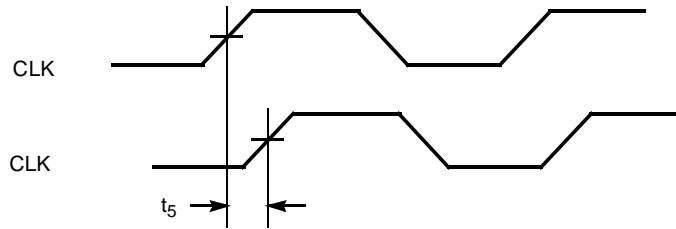
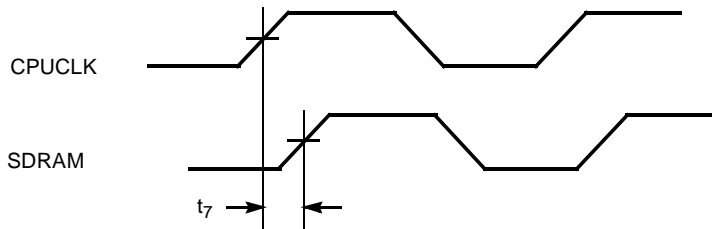
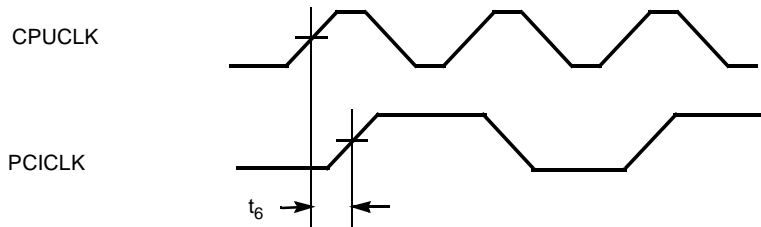
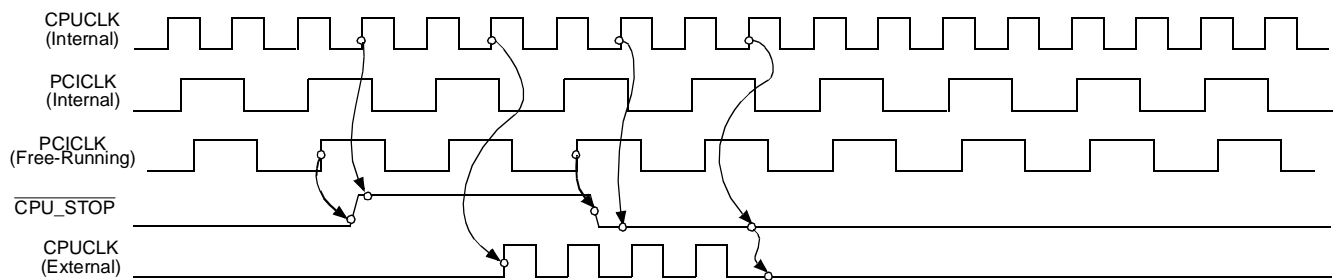


#### CPUCLK Outputs HIGH/LOW Time

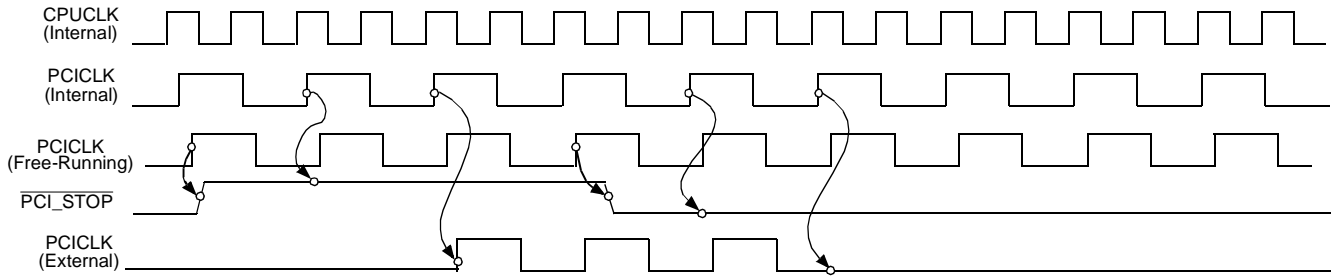
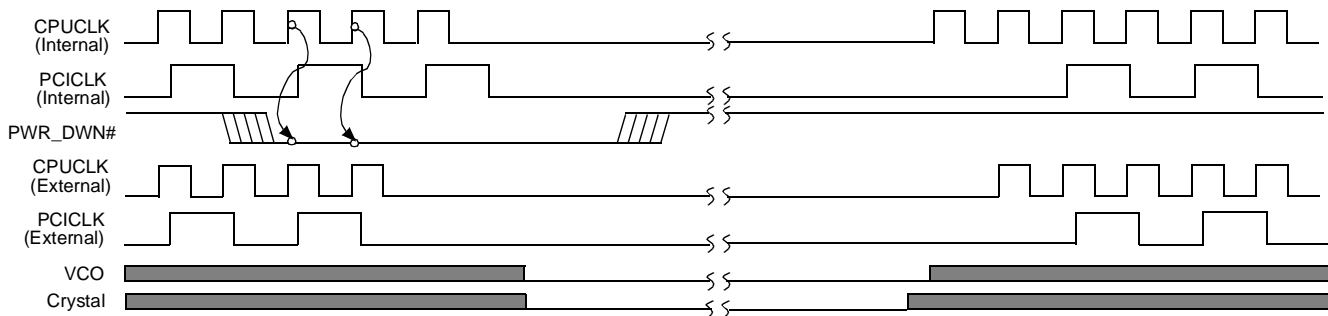


#### All Outputs Rise/Fall Time

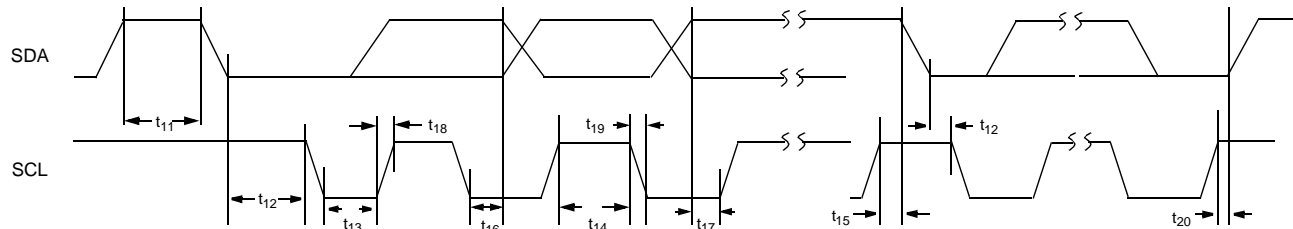


**Switching Waveforms (continued)**
**CPU-CPU Clock Skew**

**CPU-SDRAM Clock Skew**

**CPU-PCI Clock Skew**

**CPU\_STOP<sup>[17, 18]</sup>**

**Notes:**

17. CPUCLK on and CPUCLK off latency is 2 or 3 CPUCLK cycles.
18. CPU\_STOP may be applied asynchronously. It is synchronized internally.

**Switching Waveforms (continued)**
**PCI\_STOP [19, 20]**

**PWR\_DOWN**


Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

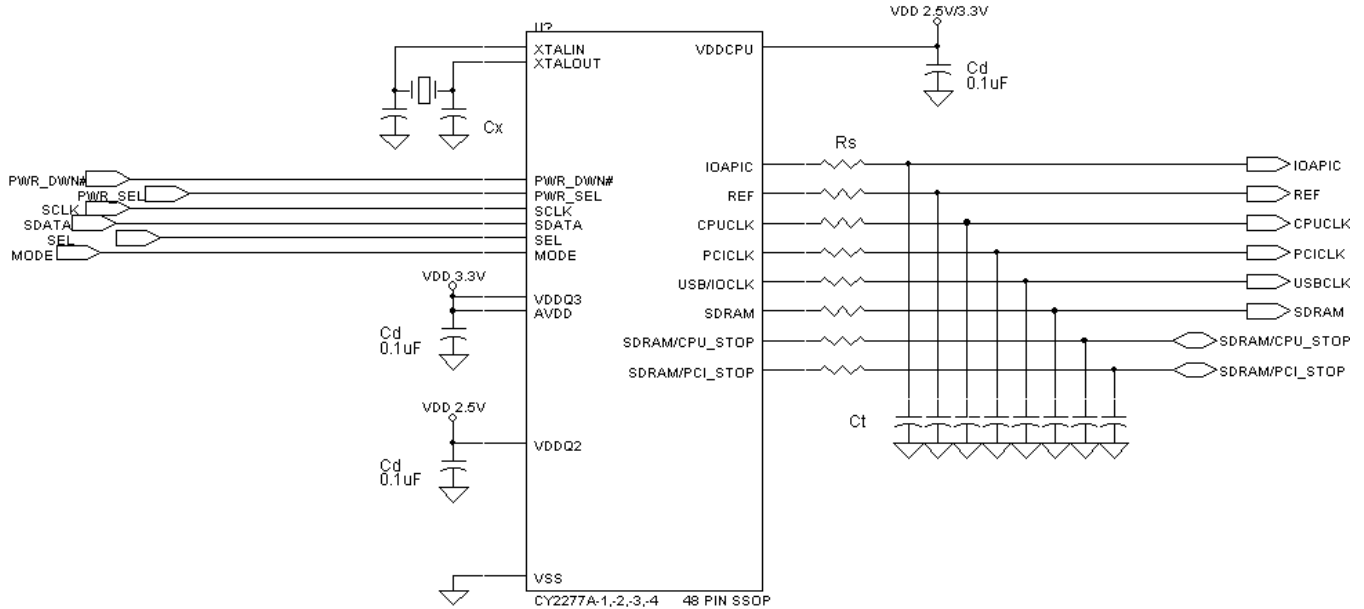
**Timing Requirements for the I<sup>2</sup>C Bus**

**Notes:**

19. PCICLK on and PCICLK off latency is 1 rising edge of the external PCICLK.
20. PCI\_STOP may be applied asynchronously. It is synchronized internally.

## Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

## Application Circuit



Cd = DECOUPLING CAPACITORS

Ct = OPTIONAL EMI-REDUCING CAPACITORS

Cx = OPTIONAL LOAD MATCHING CAPACITOR

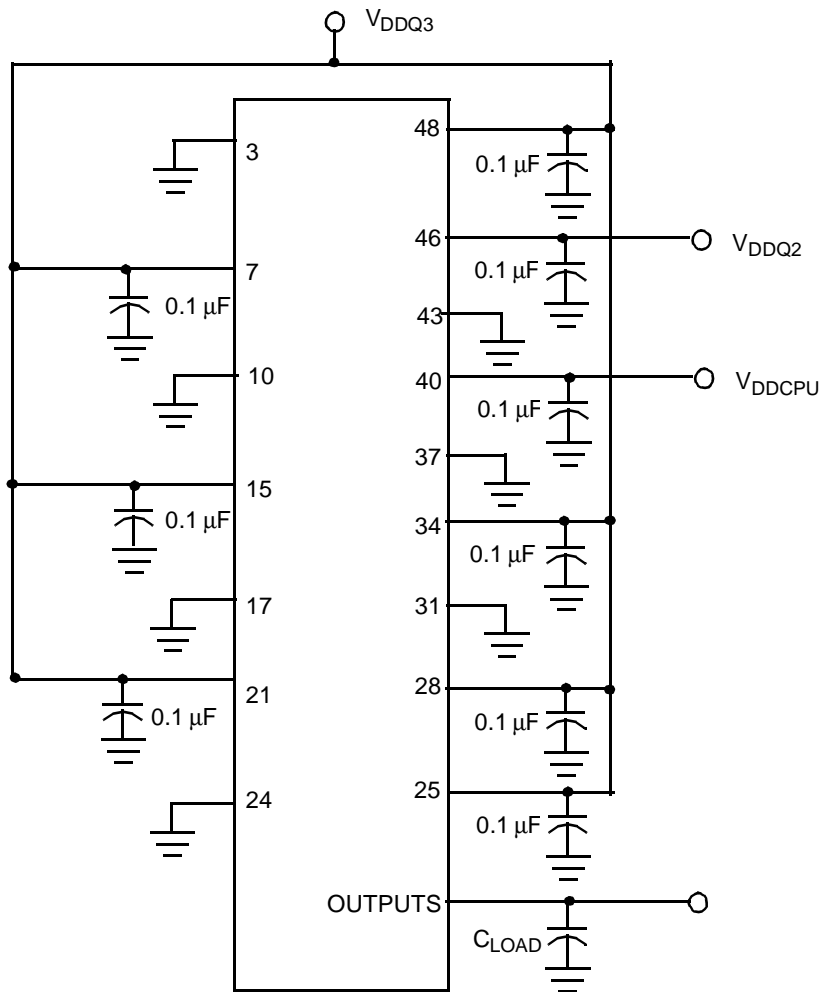
Rs = SERIES TERMINATING RESISTORS

## Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and  $C_{LOAD}$  of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different  $C_{LOAD}$  is used. Footprints can be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1  $\mu$ F. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where  $R_{trace}$  is the loaded characteristic impedance of the trace,  $R_{out}$  is the output impedance of the clock generator (specified in the data sheet), and  $R_{series}$  is the series terminating resistor.

$$R_{series} \geq R_{trace} - R_{out}$$

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board  $V_{DD}$  from the clock generator  $V_{DD}$  island. Ensure that the Ferrite Bead offers greater than 50 $\Omega$  impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10  $\mu$ F– 22  $\mu$ F tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

**Test Circuit**


Note: All capacitors should be placed as close to each pin as possible.

**Ordering Information**

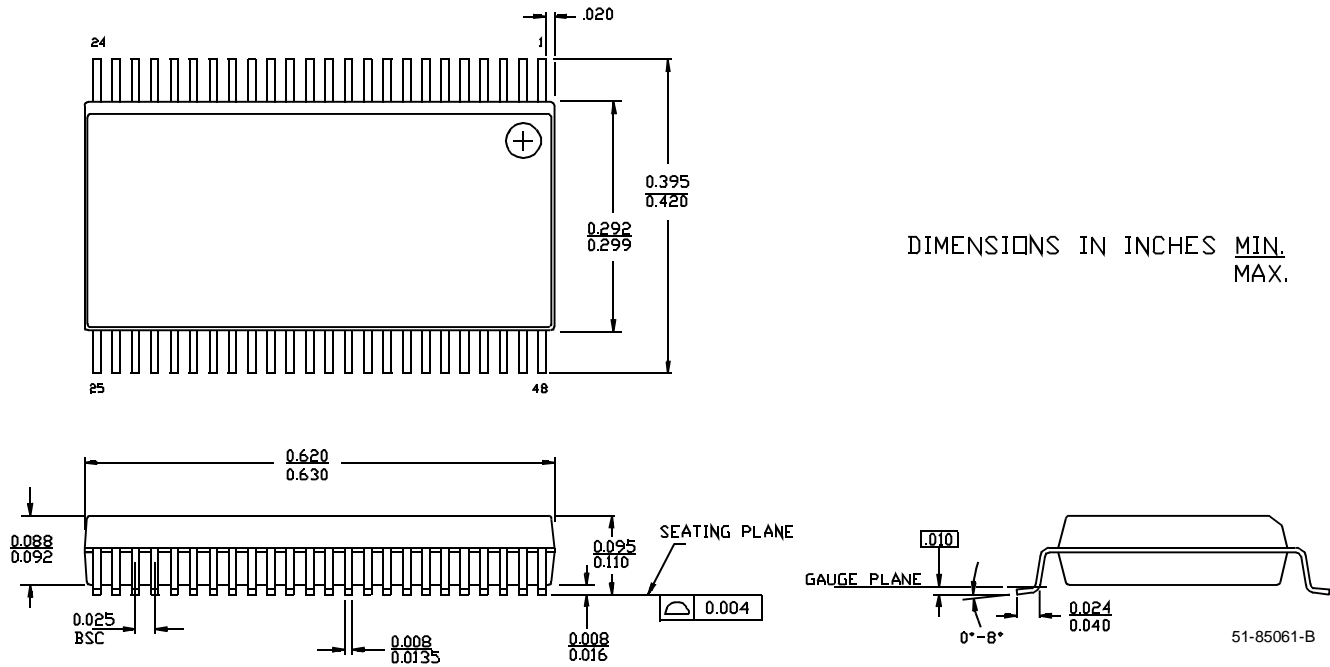
Ordering Code	Package Name	Package Type	Operating Range
CY2277APAC-1	Z48	48-Pin TSSOP	Commercial
CY2277APVC-1	O48	48-Pin SSOP	Commercial
CY2277APAC-1M	Z48	49-Pin TSSOP	Commercial
CY2277APVC-2	O48	48-Pin SSOP	Commercial
CY2277APVC-3	O48	48-Pin SSOP	Commercial
CY2277APAC-12	Z48	48-Pin TSSOP	Commercial
CY2277APVC-12	O48	48-Pin SSOP	Commercial

Document #: 38-00612-D



Package Diagrams

48-Lead Shrunken Small Outline Package O48



48-Lead Thin Shrunken Small Outline Package Z48

