

Output Limiting, Ultra High Speed Programmable Gain, Buffer Amplifier

July 1994

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- User Programmable Output Voltage Limiting
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Low Differential Gain and Phase 0.02%/0.04 Deg.
- Low Distortion (HD3, 30MHz) -73dBc (Typ)
- Wide -3dB Bandwidth 850MHz (Typ)
- Very High Slew Rate 2400V/ μ s (Typ)
- Fast Settling (0.1%) 13ns (Typ)
- Excellent Gain Flatness (to 100MHz) 0.07dB (Typ)
- Excellent Gain Accuracy 0.99V/V (Typ)
- High Output Current 60mA (Typ)
- Fast Overdrive Recovery <1ns (Typ)

Applications

- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems

Description

The HFA1113/883 is a closed loop buffer featuring a high degree of gain accuracy, wide bandwidth, low distortion, and programmable output limiting. This buffer is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overdrive recovery times. The output limiting function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The sub-nanosecond overdrive recovery time quickly returns the amplifier to linear operation following an overdrive condition.

Component and composite video systems will also benefit from this buffer's performance, as indicated by the excellent gain flatness, and 0.02%/0.04 Deg. Differential Gain/Phase specifications ($R_L = 150\Omega$).

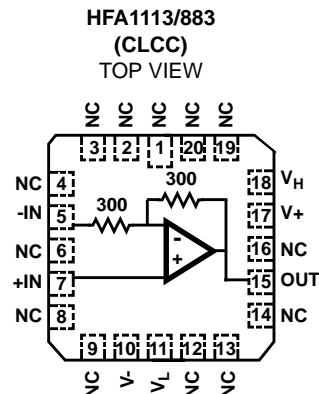
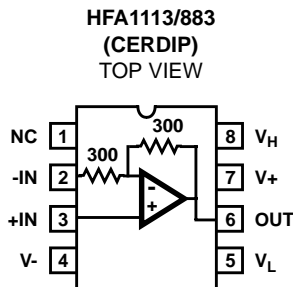
A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components, as described in the "Design Information" section. Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

This amplifier is available without output limiting as the HFA1112/883. For applications requiring a standard buffer pinout, please refer to the HFA1110/883 datasheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1113MJ/883	-55°C to +125°C	8 Lead CerDIP
HFA1113ML/883	-55°C to +125°C	20 Lead Ceramic LCC

Pinouts



Specifications HFA1113/883

Absolute Maximum Ratings

Voltage Between V+ and V-	12V
Differential Input Voltage	5V
Voltage at Either Input Terminal	V+ to V-
Voltage at V _H or V _L Terminal	(V+) + 2V to (V-) - 2V
Output Current (50% Duty Cycle)	±55mA
Junction Temperature	+175°C
ESD Rating	< 2000V
Storage Temperature Range	-65°C ≤ T _A ≤ +150°C
Lead Temperature (Soldering 10s)	+300°C

Thermal Information

Thermal Resistance	θ _{JA}	θ _{JC}
CerDIP Package	115°C/W	30°C/W
Ceramic LCC Package	75°C/W	23°C/W
Maximum Package Power Dissipation at +75°C		
CerDIP Package	0.87W	
Ceramic LCC Package	1.33W	
Package Power Dissipation Derating Factor above +75°C		
CerDIP Package	8.7mW/°C	
Ceramic LCC Package	13.3mW/°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (±V _S)	±5V	R _L ≥ 50Ω
Operating Temperature Range	-55°C ≤ T _A ≤ +125°C	

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{SUPPLY} = ±5V, R_{SOURCE} = 0Ω, R_L = 100Ω, V_{OUT} = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS	
					MIN	MAX		
Output Offset Voltage	V _{OS}	V _{CM} = 0V	1	+25°C	-25	25	mV	
			2, 3	+125°C, -55°C	-40	40	mV	
Power Supply Rejection Ratio	PSRRP	ΔV _{SUPPLY} = ±1.25V, V+ = 6.25V, V- = -5V, V+ = 3.75V, V- = -5V	1	+25°C	39	-	dB	
			2, 3	+125°C, -55°C	35	-	dB	
	PSRRN	ΔV _{SUPPLY} = ±1.25V, V+ = 5V, V- = -6.25V, V+ = 5V, V- = -3.75V	1	+25°C	39	-	dB	
			2, 3	+125°C, -55°C	35	-	dB	
Non-Inverting Input (+IN) Current	I _{BSP}	V _{CM} = 0V	1	+25°C	-40	40	μA	
			2, 3	+125°C, -55°C	-65	65	μA	
+IN Common Mode Rejection	CMS _{IBP}	ΔV _{CM} = ±2V, V+ = 3V, V- = -7V, V+ = 7V, V- = -3V	1	+25°C	-	40	μA/V	
			2, 3	+125°C, -55°C	-	50	μA/V	
+IN Resistance	+R _{IN}	Note 1	1	+25°C	25	-	kΩ	
			2, 3	+125°C, -55°C	20	-	kΩ	
Gain (V _{OUT} = 2V _{P-P})	A _{VP1}	A _V = +1, V _{IN} = -1V to +1V	1	+25°C	0.980	1.020	V/V	
			2, 3	+125°C, -55°C	0.975	1.025	V/V	
Gain (V _{OUT} = 2V _{P-P})	A _{VM1}	A _V = -1, V _{IN} = -1V to +1V	1	+25°C	0.980	1.020	V/V	
			2, 3	+125°C, -55°C	0.975	1.025	V/V	
Gain (V _{OUT} = 4V _{P-P})	A _{VP2}	A _V = +2, V _{IN} = -1V to +1V	1	+25°C	1.960	2.040	V/V	
			2, 3	+125°C, -55°C	1.950	2.050	V/V	
Output Voltage Swing	V _{OP100}	A _V = -1 R _L = 100Ω	V _{IN} = -3.2V	1	+25°C	3	-	V
			V _{IN} = -2.7V	2, 3	+125°C, -55°C	2.5	-	V
	V _{ON100}	A _V = -1 R _L = 100Ω	V _{IN} = +3.2V	1	+25°C	-	-3	V
			V _{IN} = +2.7V	2, 3	+125°C, -55°C	-	-2.5	V
Output Voltage Swing	V _{OP50}	A _V = -1 R _L = 50Ω	V _{IN} = -2.7V	1, 2	+25°C, +125°C	2.5	-	V
			V _{IN} = -2.25V	3	-55°C	1.5	-	V
	V _{ON50}	A _V = -1 R _L = 50Ω	V _{IN} = +2.7V	1, 2	+25°C, +125°C	-	-2.5	V
			V _{IN} = +2.25V	3	-55°C	-	-1.5	V
Output Current	+I _{OUT}	Note 2	1, 2	+25°C, +125°C	50	-	mA	
			3	-55°C	30	-	mA	
	-I _{OUT}	Note 2	1, 2	+25°C, +125°C	-	-50	mA	
			3	-55°C	-	-30	mA	

Specifications HFA1113/883

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $V_{SUPPLY} = \pm 5V$, $R_{SOURCE} = 0\Omega$, $R_L = 100\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Quiescent Power Supply Current	I_{CC}	$R_L = 100\Omega$	1	+25°C	14	26	mA
			2, 3	+125°C, -55°C	-	33	mA
	I_{EE}	$R_L = 100\Omega$	1	+25°C	-26	-14	mA
			2, 3	+125°C, -55°C	-33	-	mA
Limiting Accuracy	$V_H CLMP$	$A_V = -1$, $V_{IN} = -1.6V$, $V_H = 1V$	1	+25°C	-150	150	mV
			2, 3	+125°C, -55°C	-200	200	mV
	$V_L CLMP$	$A_V = -1$, $V_{IN} = +1.6V$, $V_L = -1V$	1	+25°C	-150	150	mV
			2, 3	+125°C, -55°C	-200	200	mV
V_H or V_L Input Current	$V_H BIAS$	$V_H = 1V$	1	+25°C	-	200	μA
			2, 3	+125°C, -55°C	-	300	μA
	$V_L BIAS$	$V_L = -1V$	1	+25°C	-200	-	μA
			2, 3	+125°C, -55°C	-300	-	μA

NOTES:

1. Guaranteed from +IN Common Mode Rejection Test, by: $+R_{IN} = 1/CMS_{IBP}$.
2. Guaranteed from V_{OUT} Test with $R_L = 50\Omega$, by: $I_{OUT} = V_{OUT}/50\Omega$.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: $V_{SUPPLY} = \pm 5V$, $R_L = 100\Omega$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
-3dB Bandwidth	$BW(-1)$	$A_V = -1$, $V_{OUT} = 200mV_{P-P}$	1	+25°C	450	-	MHz
	$BW(+1)$	$A_V = +1$, $V_{OUT} = 200mV_{P-P}$	1	+25°C	500	-	MHz
	$BW(+2)$	$A_V = +2$, $V_{OUT} = 200mV_{P-P}$	1	+25°C	350	-	MHz
Gain Flatness	$GF30$	$A_V = +2$, $f \leq 30MHz$, $V_{OUT} = 200mV_{P-P}$	1	+25°C	-	± 0.04	dB
	$GF50$	$A_V = +2$, $f \leq 50MHz$, $V_{OUT} = 200mV_{P-P}$	1	+25°C	-	± 0.08	dB
	$GF100$	$A_V = +2$, $f \leq 100MHz$, $V_{OUT} = 200mV_{P-P}$	1	+25°C	-	± 0.22	dB
Slew Rate	+SR(-1)	$A_V = -1$, $V_{OUT} = 5V_{P-P}$	1, 2	+25°C	1500	-	V/ μs
	-SR(-1)	$A_V = -1$, $V_{OUT} = 5V_{P-P}$	1, 2	+25°C	1800	-	V/ μs
	+SR(+1)	$A_V = +1$, $V_{OUT} = 5V_{P-P}$	1, 2	+25°C	900	-	V/ μs
	-SR(+1)	$A_V = +1$, $V_{OUT} = 5V_{P-P}$	1, 2	+25°C	800	-	V/ μs
	+SR(+2)	$A_V = +2$, $V_{OUT} = 5V_{P-P}$	1, 2	+25°C	1200	-	V/ μs
	-SR(+2)	$A_V = +2$, $V_{OUT} = 5V_{P-P}$	1, 2	+25°C	1100	-	V/ μs

Specifications HFA1113/883

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: $V_{SUPPLY} = \pm 5V$, $R_L = 100\Omega$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Rise and Fall Time	$T_{R(-1)}$	$A_V = -1, V_{OUT} = 0.5V_{P-P}$	1, 2	+25°C	-	750	ps
	$T_{F(-1)}$	$A_V = -1, V_{OUT} = 0.5V_{P-P}$	1, 2	+25°C	-	800	ps
	$T_{R(+1)}$	$A_V = +1, V_{OUT} = 0.5V_{P-P}$	1, 2	+25°C	-	750	ps
	$T_{F(+1)}$	$A_V = +1, V_{OUT} = 0.5V_{P-P}$	1, 2	+25°C	-	750	ps
	$T_{R(+2)}$	$A_V = +2, V_{OUT} = 0.5V_{P-P}$	1, 2	+25°C	-	1000	ps
	$T_{F(+2)}$	$A_V = +2, V_{OUT} = 0.5V_{P-P}$	1, 2	+25°C	-	1000	ps
Overshoot	+OS(-1)	$A_V = -1, V_{OUT} = 0.5V_{P-P}$	1, 3	+25°C	-	30	%
	-OS(-1)	$A_V = -1, V_{OUT} = 0.5V_{P-P}$	1, 3	+25°C	-	25	%
	+OS(+1)	$A_V = +1, V_{OUT} = 0.5V_{P-P}$	1, 3	+25°C	-	65	%
	-OS(+1)	$A_V = +1, V_{OUT} = 0.5V_{P-P}$	1, 3	+25°C	-	60	%
	+OS(+2)	$A_V = +2, V_{OUT} = 0.5V_{P-P}$	1, 3	+25°C	-	20	%
	-OS(+2)	$A_V = +2, V_{OUT} = 0.5V_{P-P}$	1, 3	+25°C	-	20	%
Settling Time	TS(0.1)	$A_V = +2, \text{to } 0.1\%, V_{OUT} = 2V \text{ to } 0V$	1	+25°C	-	20	ns
	TS(0.05)	$A_V = +2, \text{to } 0.05\%, V_{OUT} = 2V \text{ to } 0V$	1	+25°C	-	33	ns
2nd Harmonic Distortion	HD2(30)	$A_V = +2, f = 30\text{MHz}, V_{OUT} = 2V_{P-P}$	1	+25°C	-	-45	dBc
	HD2(50)	$A_V = +2, f = 50\text{MHz}, V_{OUT} = 2V_{P-P}$	1	+25°C	-	-40	dBc
	HD2(100)	$A_V = +2, f = 100\text{MHz}, V_{OUT} = 2V_{P-P}$	1	+25°C	-	-35	dBc
3rd Harmonic Distortion	HD3(30)	$A_V = +2, f = 30\text{MHz}, V_{OUT} = 2V_{P-P}$	1	+25°C	-	-65	dBc
	HD3(50)	$A_V = +2, f = 50\text{MHz}, V_{OUT} = 2V_{P-P}$	1	+25°C	-	-55	dBc
	HD3(100)	$A_V = +2, f = 100\text{MHz}, V_{OUT} = 2V_{P-P}$	1	+25°C	-	-45	dBc

NOTES:

- Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot-to-lot and within lot variation.
- Measured between 10% and 90% points.
- For 200ps input transition times. Overshoot decreases as input transition times increase, especially for $A_V = +1$. Please refer to Performance Curves.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3
Group A Test Requirements	1, 2, 3
Groups C and D Endpoints	1

NOTE:

- PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:

63 x 44 x 19 mils ± 1 mils
 1600 x 1130 x 483µm ± 25.4µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW Type: Metal 2: AlCu(2%)
 Thickness: Metal 1: 8kÅ ± 0.4kÅ Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:

Type: Nitride
 Thickness: 4kÅ ± 0.5kÅ

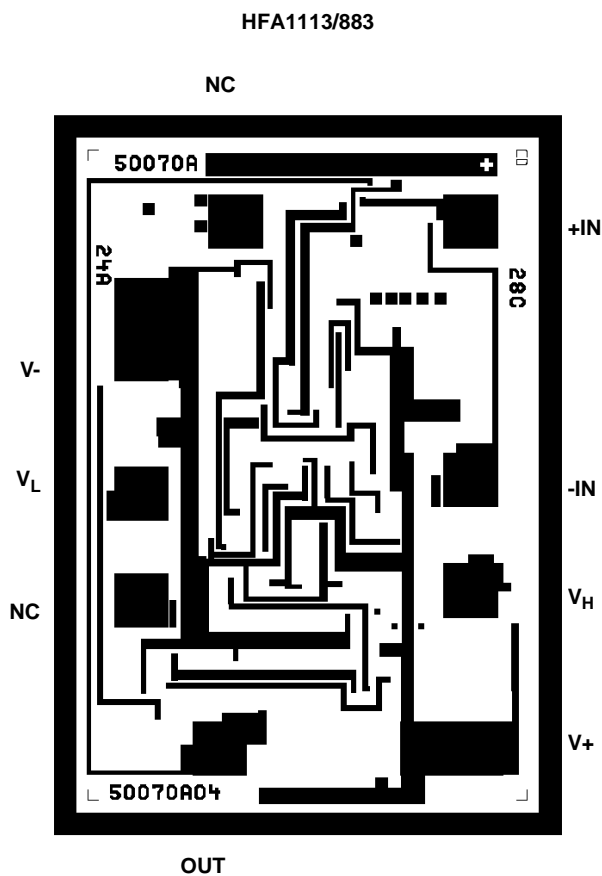
WORST CASE CURRENT DENSITY:

2.0 x 10⁵ A/cm² at 47.5mA

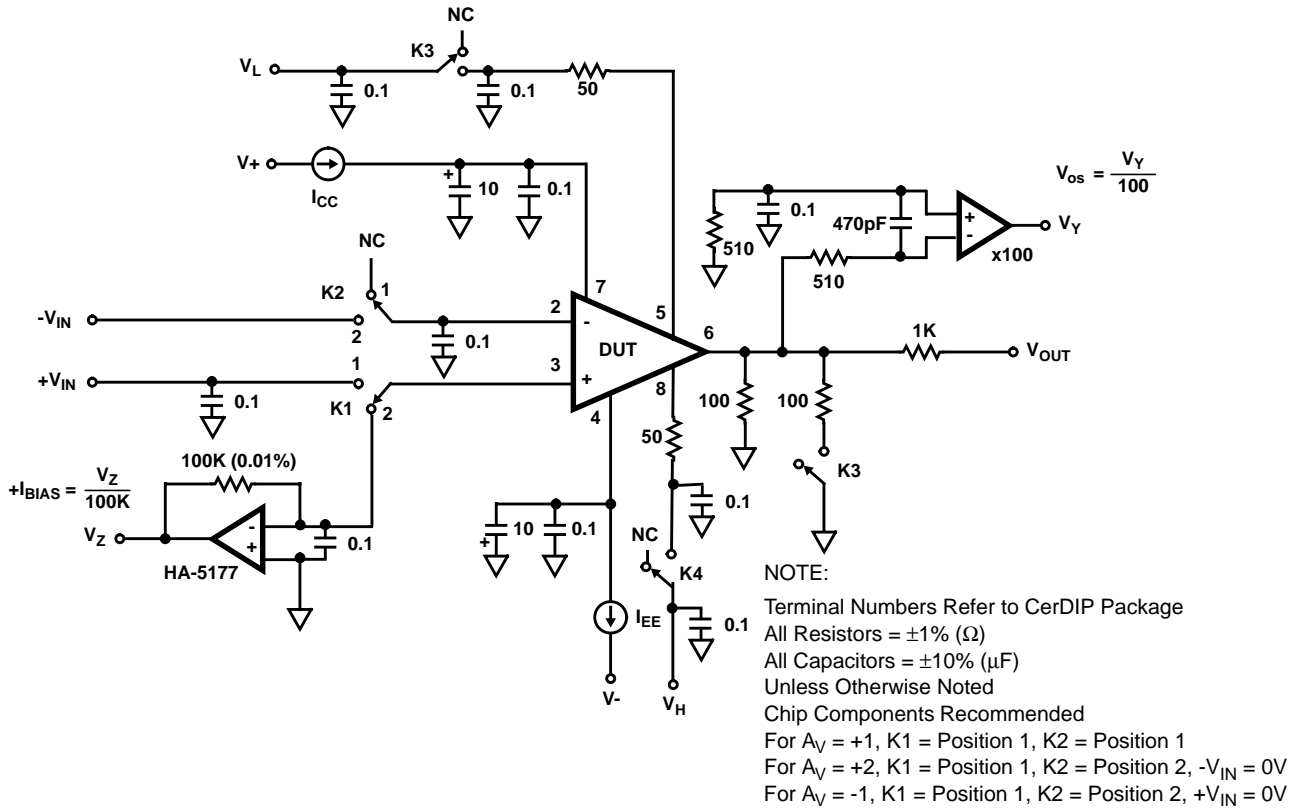
TRANSISTOR COUNT: 52

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout



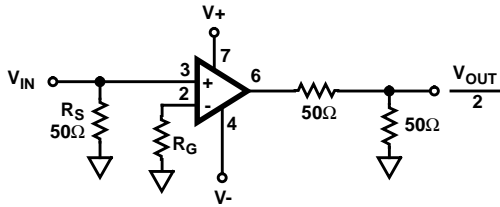
Test Circuit (Applies to Table 1)



Test Waveforms

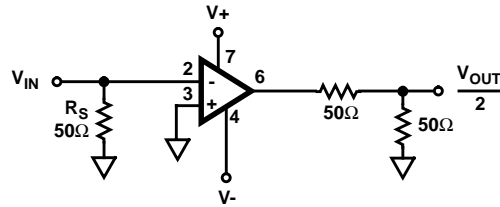
SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL PULSE RESPONSE (Applies to Table 3)

$A_V = +1$ or $+2$ TEST CIRCUIT



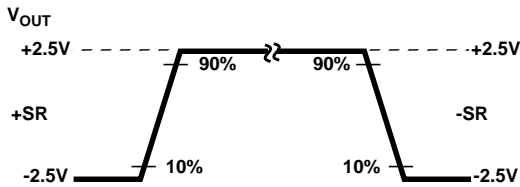
NOTE:
 $V_S = \pm 5V$, $R_G = 0\Omega$ for $A_V = +2$, $R_G = \infty$ for $A_V = +1$
 $R_F = \text{Internal}$, $R_S = 50\Omega$
 $R_L = 100\Omega$ For Small and Large Signals
 Terminal Numbers Refer to CerDIP Package

$A_V = -1$ TEST CIRCUIT

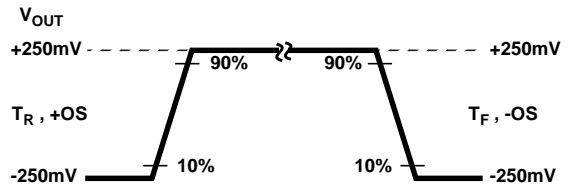


NOTE:
 $V_S = \pm 5V$, $A_V = -1$
 $R_F = \text{Internal}$
 $R_S = 50\Omega$, $R_L = 100\Omega$ For Small and Large Signals
 Terminal Numbers Refer to CerDIP Package

LARGE SIGNAL WAVEFORM



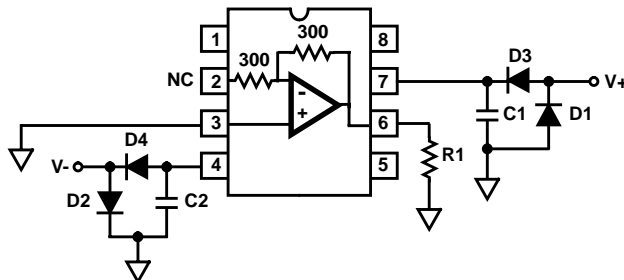
SMALL SIGNAL WAVEFORM



HFA1113/883

Burn-In Circuits

HFA1113MJ/883 CERAMIC DIP



NOTES:

R1 = 100Ω, ±5% (Per Socket)

C1 = C2 = 0.01μF (Per Socket) or 0.1μF (Per Row) Minimum

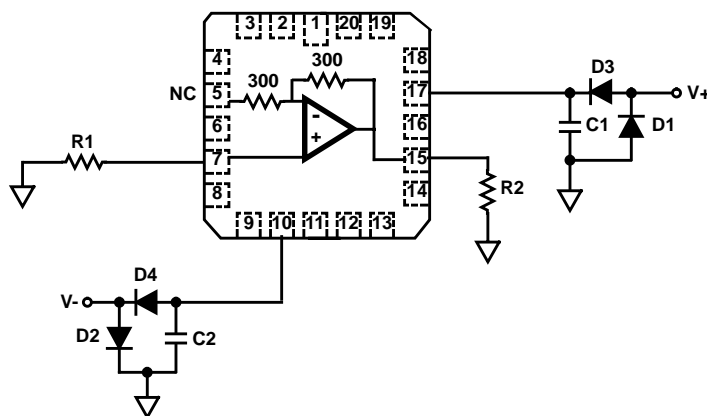
D1 = D2 = 1N4002 or Equivalent (Per Board)

D3 = D4 = 1N4002 or Equivalent (Per Socket)

V+ = +5.5V ±0.5V

V- = -5.5V ±0.5V

HFA1113ML/883 CERAMIC LCC



NOTES:

R1 = 1kΩ, ±5% (Per Socket)

R2 = 100Ω, ±5% (Per Socket)

C1 = C2 = 0.01μF (Per Socket) or 0.1μF (Per Row) Minimum

D1 = D2 = 1N4002 or Equivalent (Per Board)

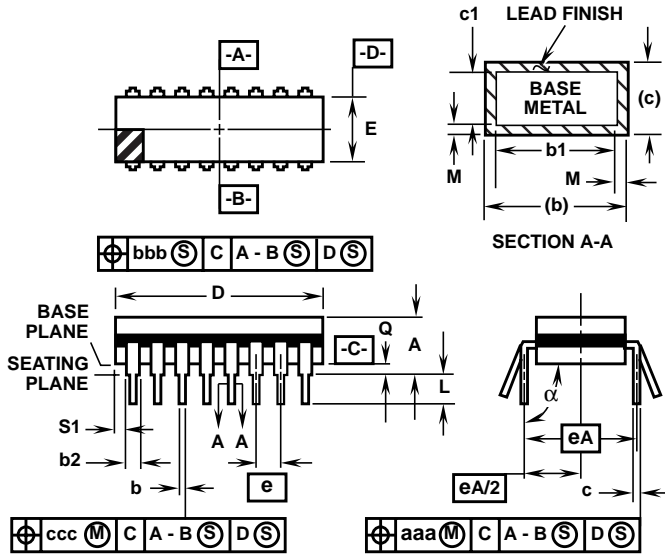
D3 = D4 = 1N4002 or Equivalent (Per Socket)

V+ = +5.5V ±0.5V

V- = -5.5V ±0.5V

Ceramic Dual-In-Line Frit Seal Packages (CerDIP)

**F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**



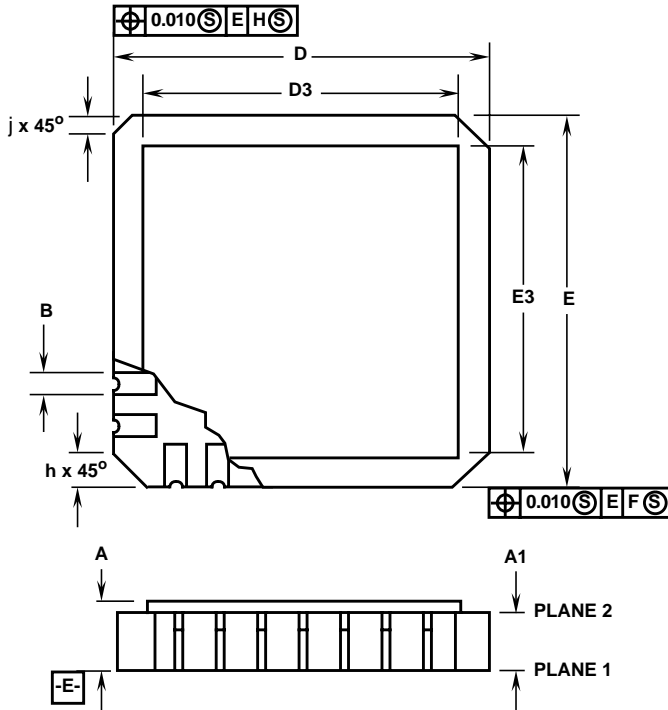
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
alpha	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.
11. Materials: Compliant to MIL-I-38535.

Rev. 0 4/94

Ceramic Leadless Chip Carrier Packages (CLCC)



J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

Rev. 0 4/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.
10. Materials: Compliant to MIL-I-38535.

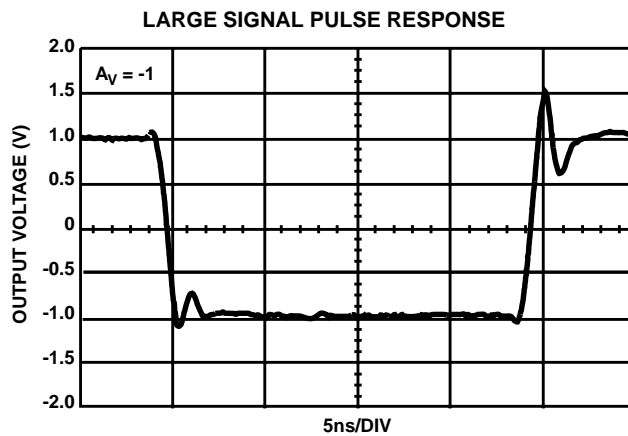
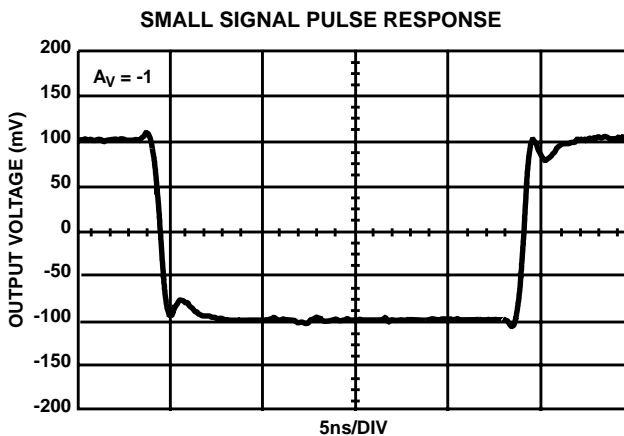
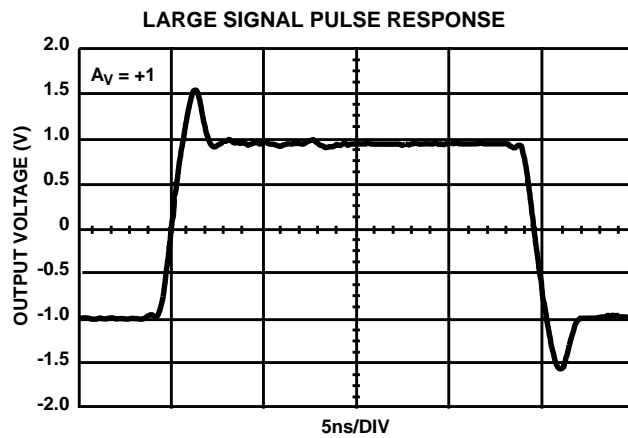
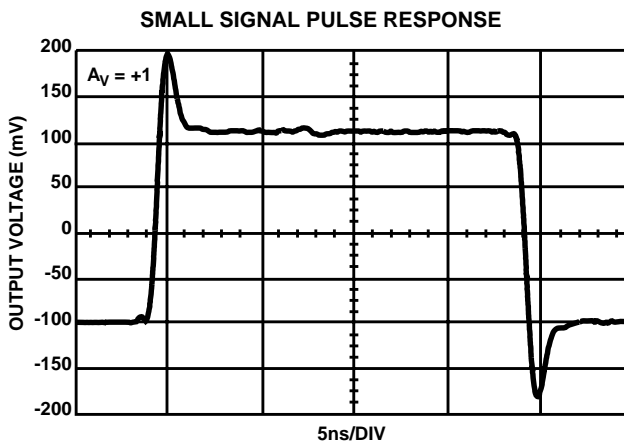
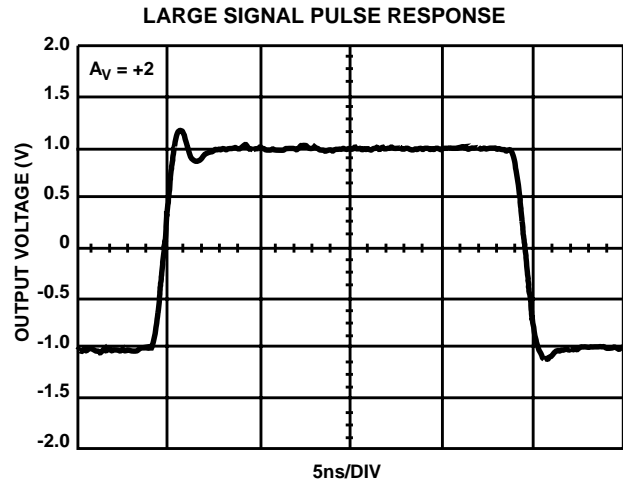
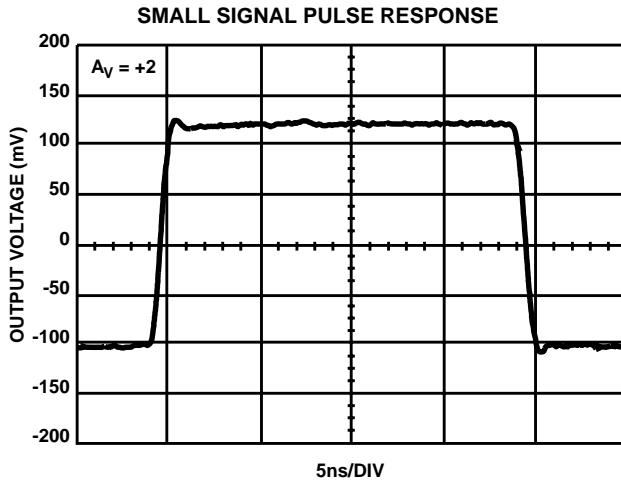
DESIGN INFORMATION

August 1999

Output Limiting, Ultra High Speed Programmable Gain Buffer Amplifier

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Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $R_L = 100\Omega$, $T_A = +25^\circ C$, Unless Otherwise Specified

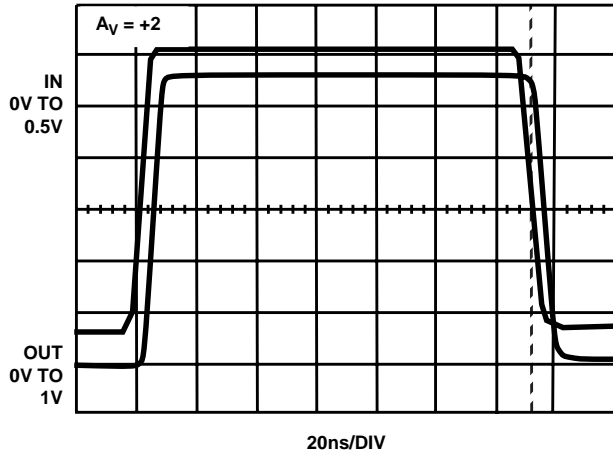


DESIGN INFORMATION (Continued)

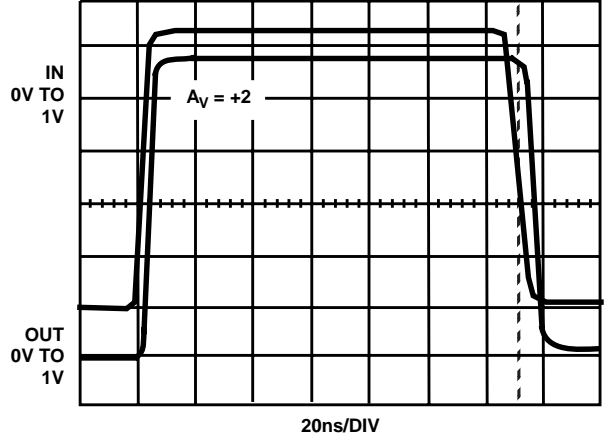
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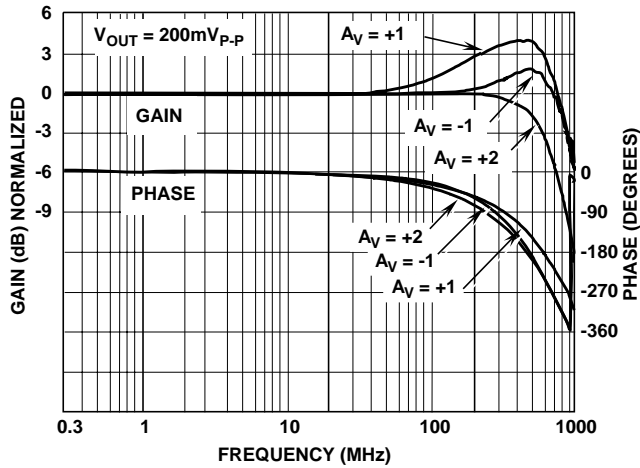
UNCLAMPED PERFORMANCE
($A_V = +2$, $V_H = 2V$, $V_L = -2V$)



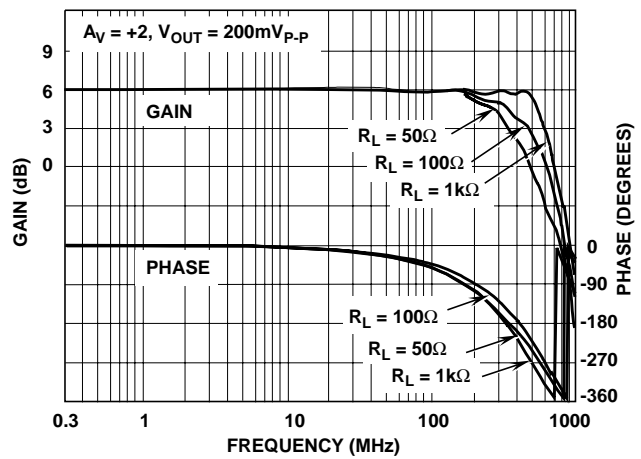
CLAMPED PERFORMANCE
($A_V = +2$, $V_H = 1V$, $V_L = -1V$, 2X Overdrive)



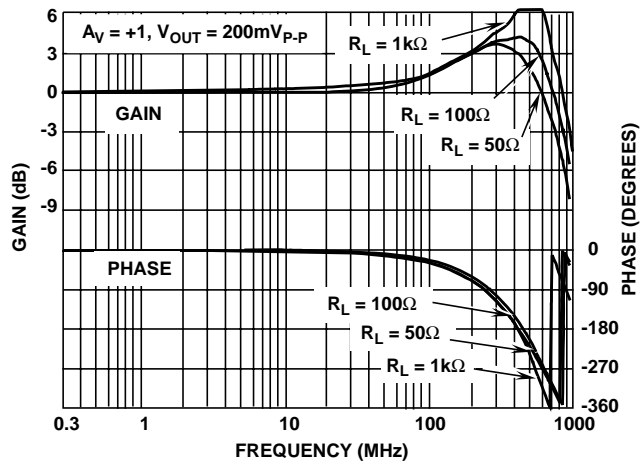
FREQUENCY RESPONSE



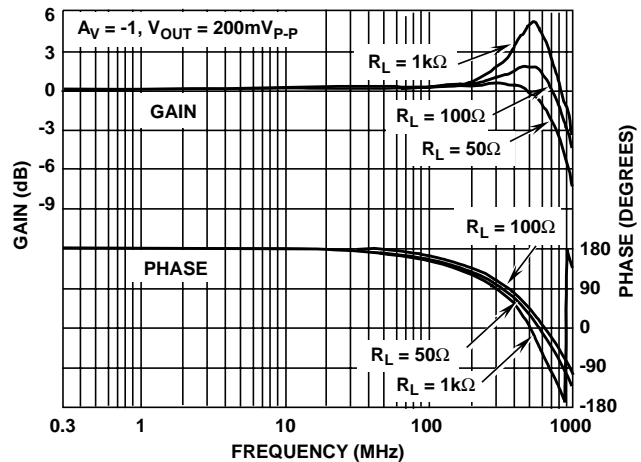
FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS



FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS



FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

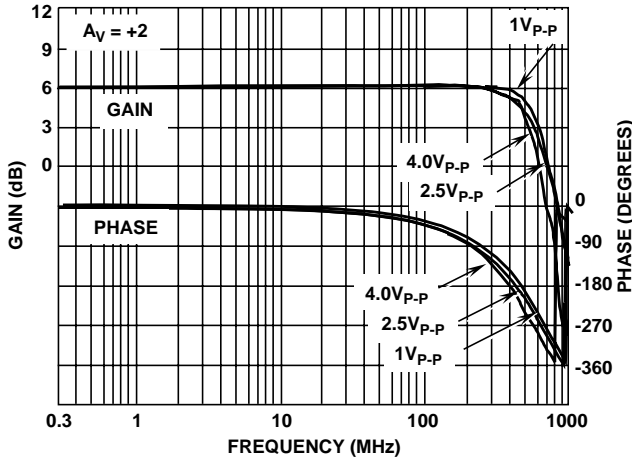


DESIGN INFORMATION (Continued)

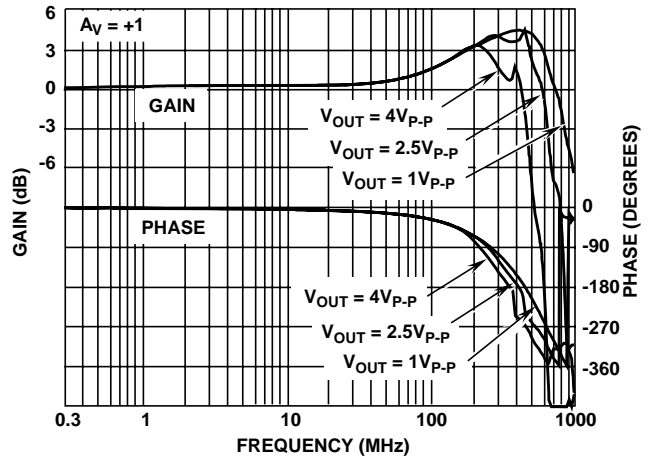
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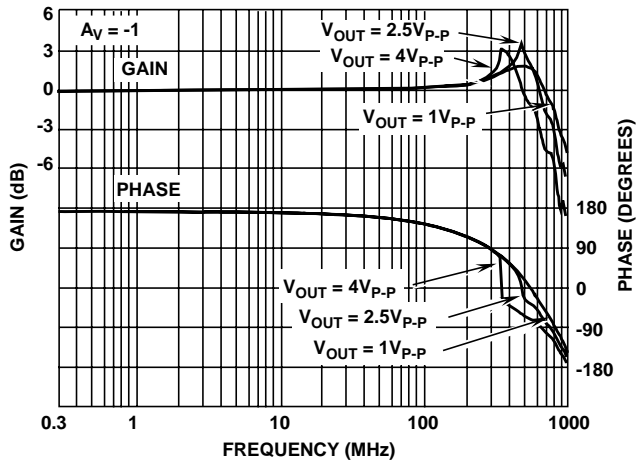
FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES



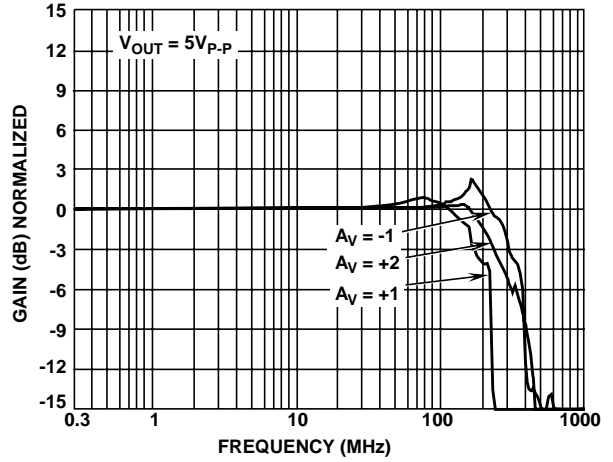
FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES



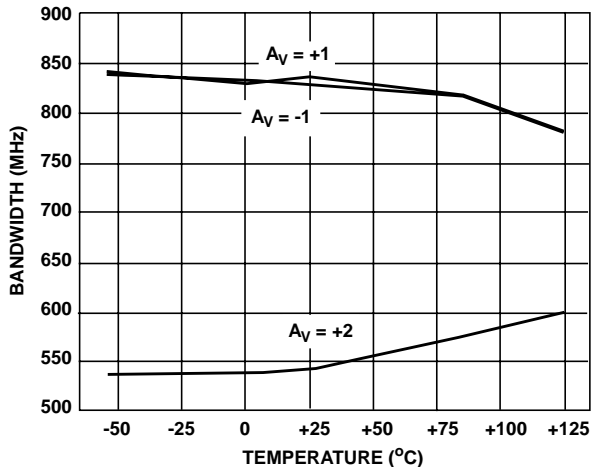
FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES



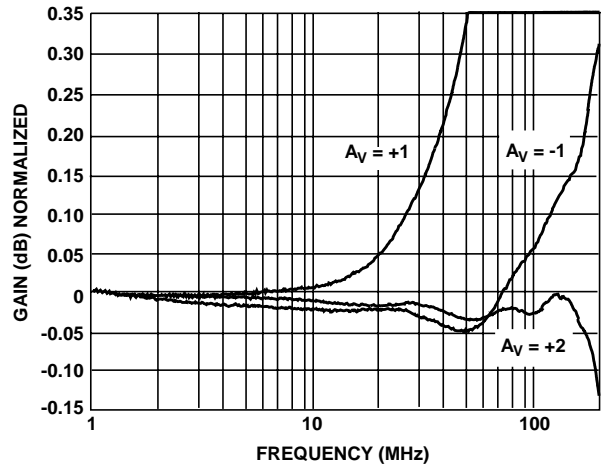
FULL POWER BANDWIDTH



-3dB BANDWIDTH vs TEMPERATURE



GAIN FLATNESS

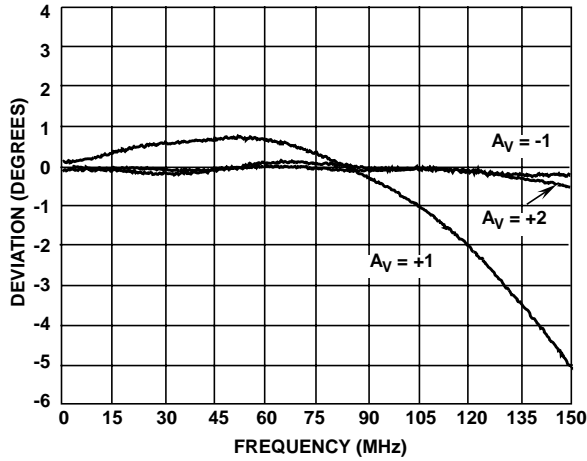


DESIGN INFORMATION (Continued)

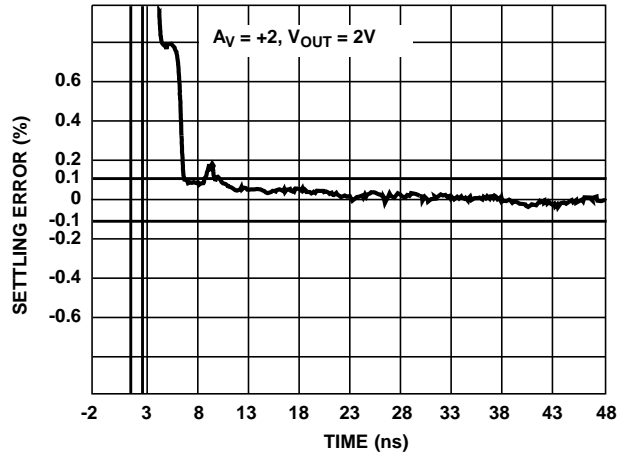
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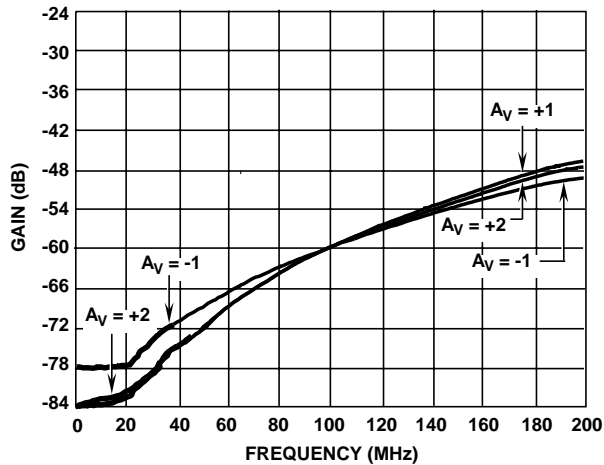
DEVIATION FROM LINEAR PHASE



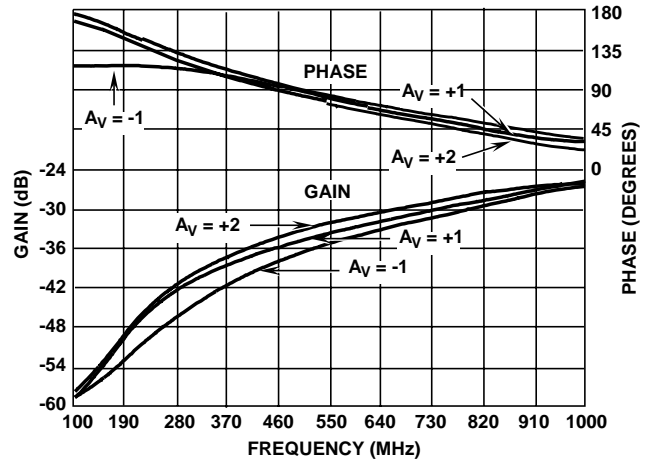
SETTLING RESPONSE



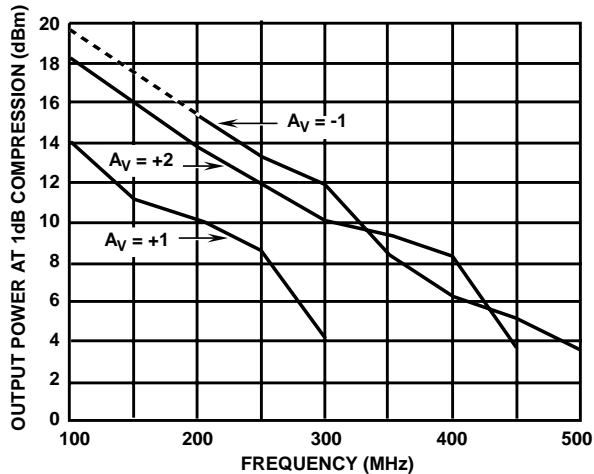
LOW FREQUENCY REVERSE ISOLATION (S_{12})



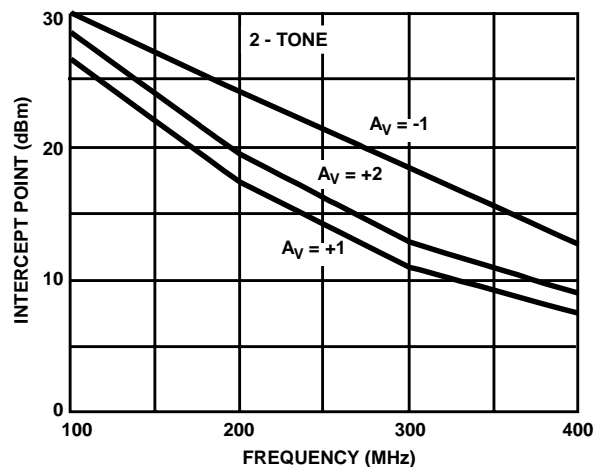
HIGH FREQUENCY REVERSE ISOLATION (S_{12})



1dB GAIN COMPRESSION vs FREQUENCY



3rd ORDER INTERMODULATION INTERCEPT vs FREQUENCY

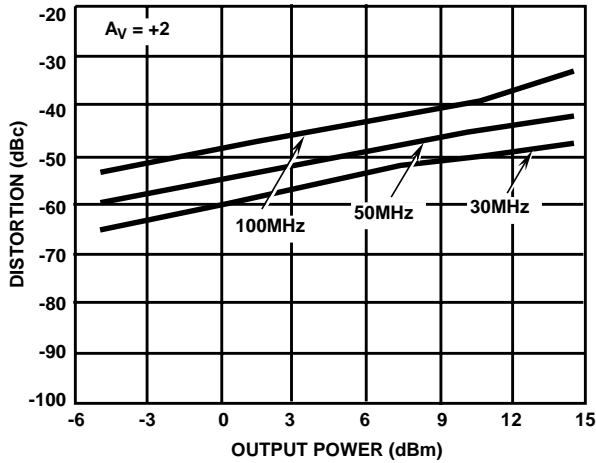


DESIGN INFORMATION (Continued)

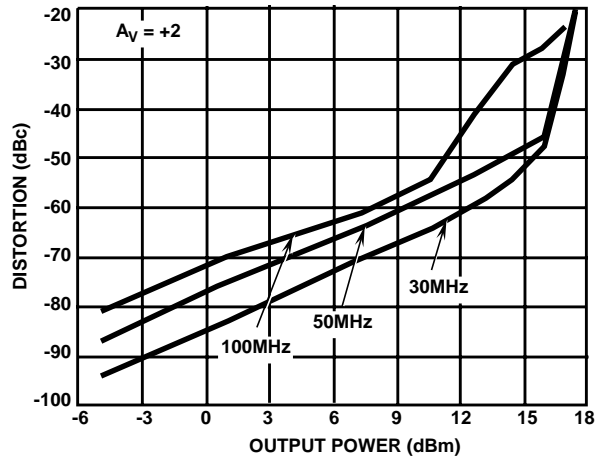
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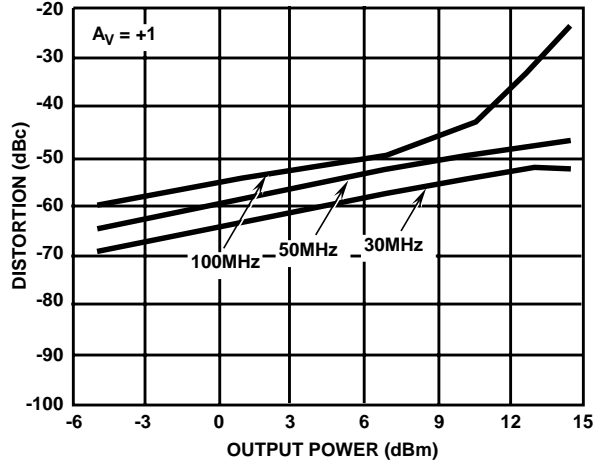
2nd HARMONIC DISTORTION vs P_{OUT}



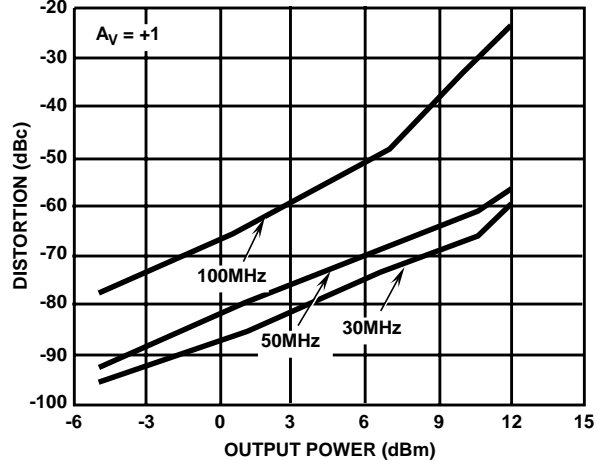
3rd HARMONIC DISTORTION vs P_{OUT}



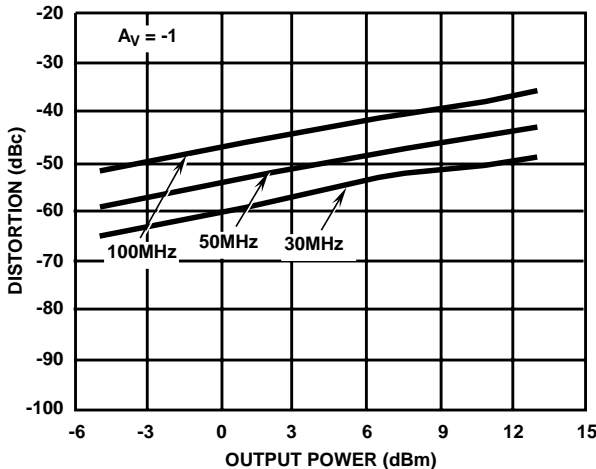
2nd HARMONIC DISTORTION vs P_{OUT}



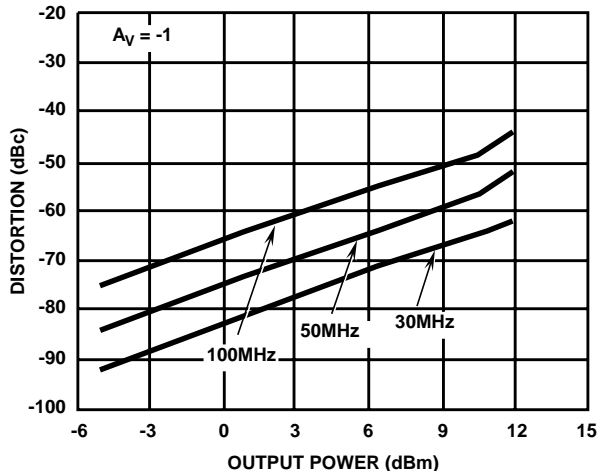
3rd HARMONIC DISTORTION vs P_{OUT}



2nd HARMONIC DISTORTION vs P_{OUT}



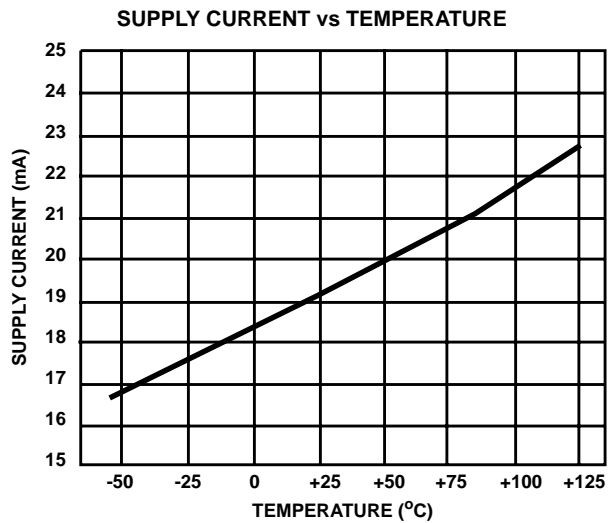
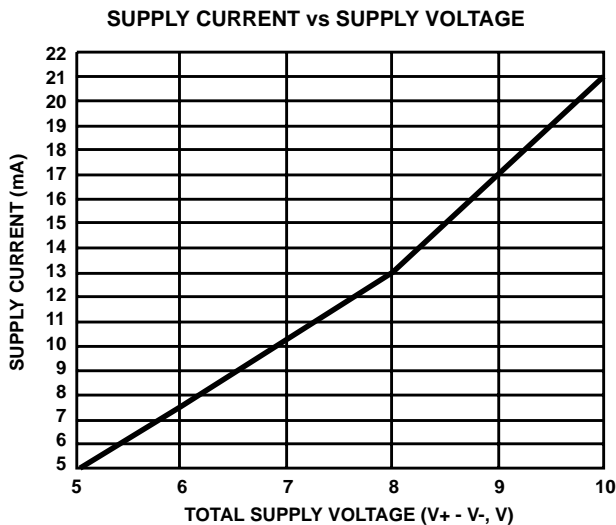
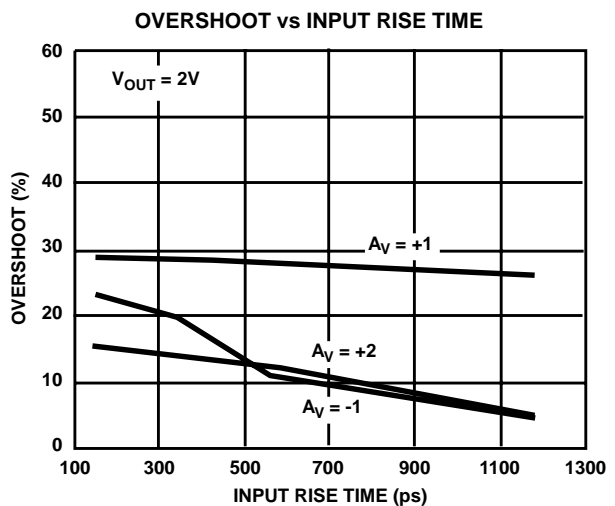
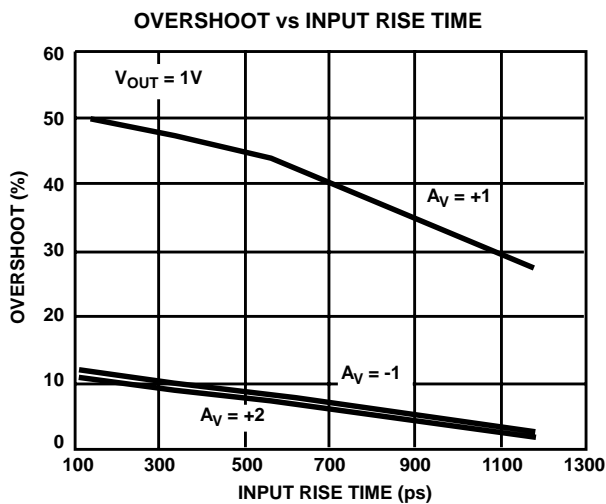
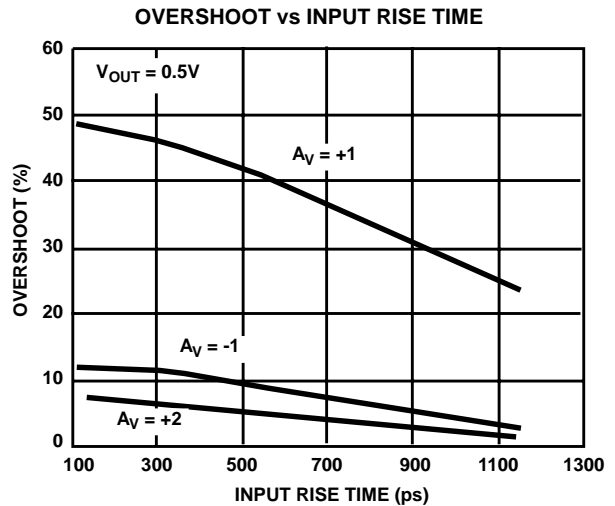
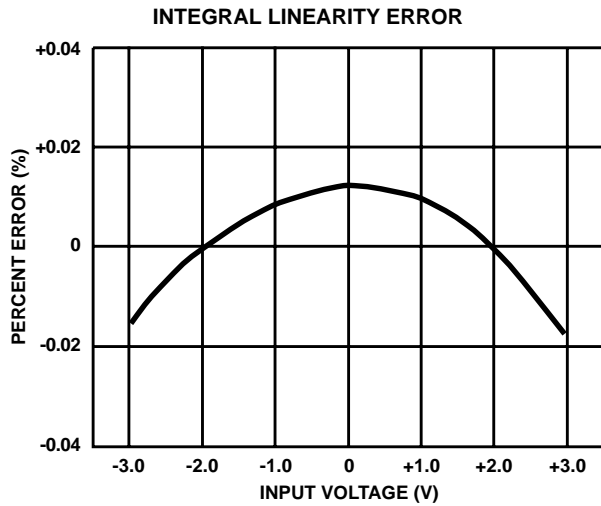
3rd HARMONIC DISTORTION vs P_{OUT}



DESIGN INFORMATION (Continued)

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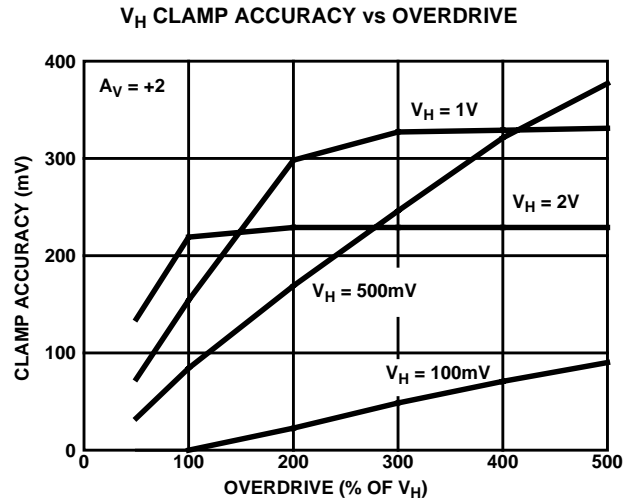
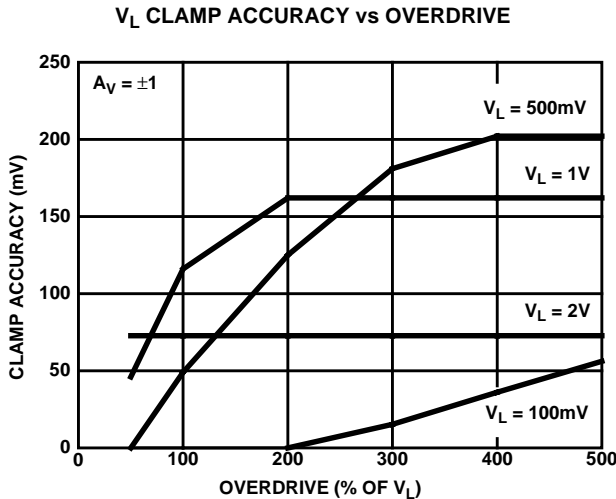
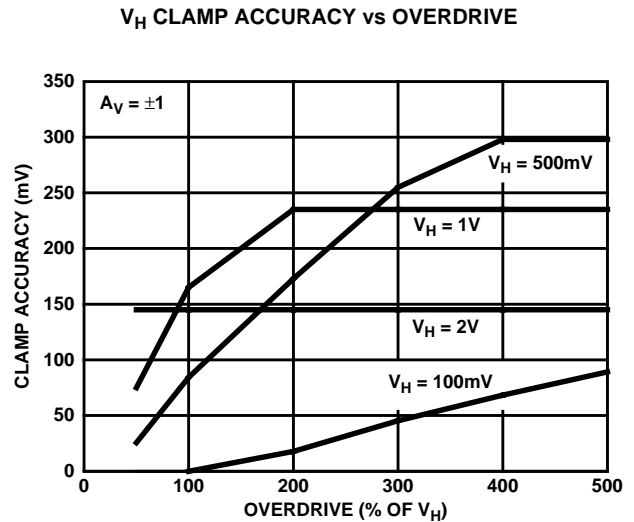
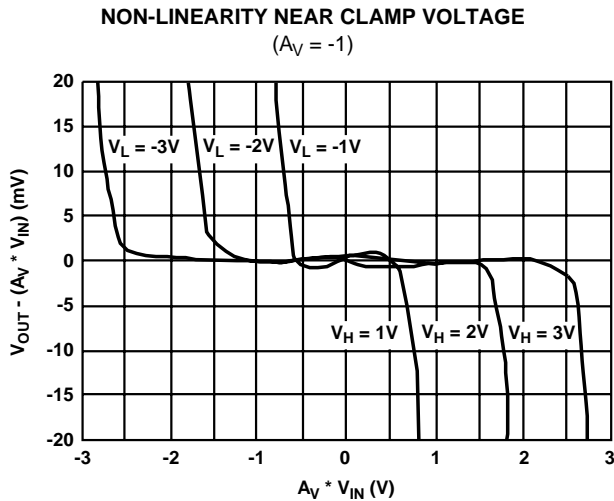
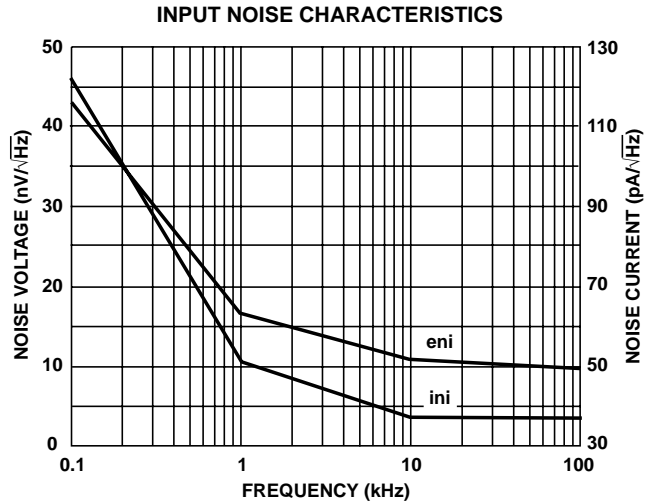
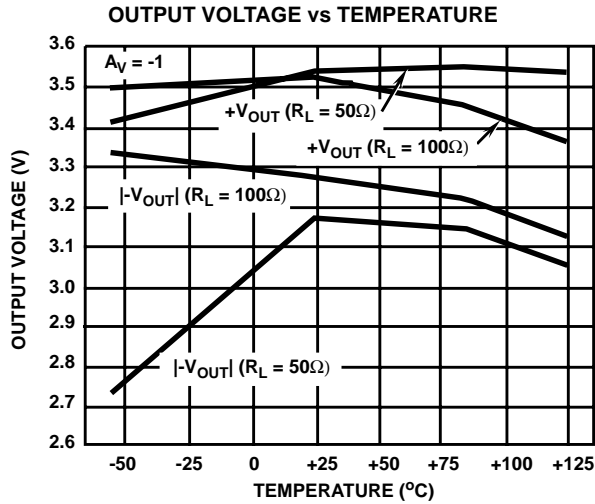
Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $R_L = 100\Omega$, $T_A = +25^\circ C$, Unless Otherwise Specified (Continued)



DESIGN INFORMATION (Continued)

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Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $R_L = 100\Omega$, $T_A = +25^\circ C$, Unless Otherwise Specified (Continued)

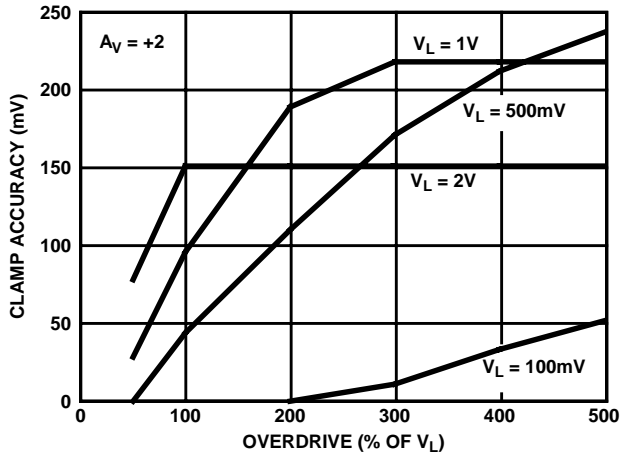


DESIGN INFORMATION (Continued)

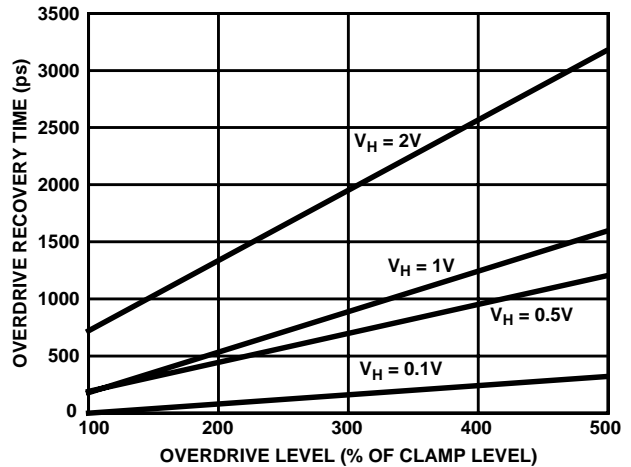
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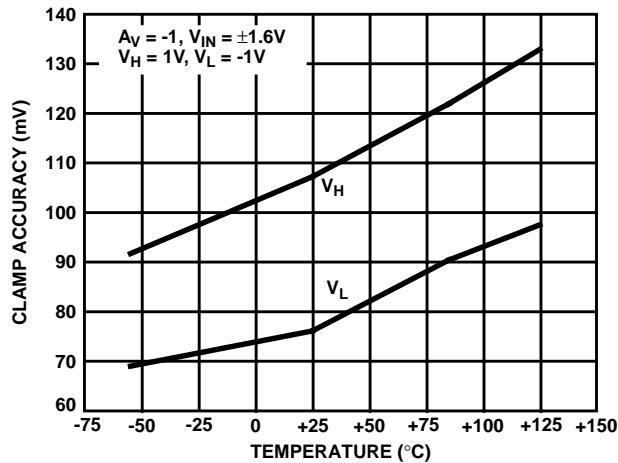
V_L CLAMP ACCURACY vs OVERDRIVE



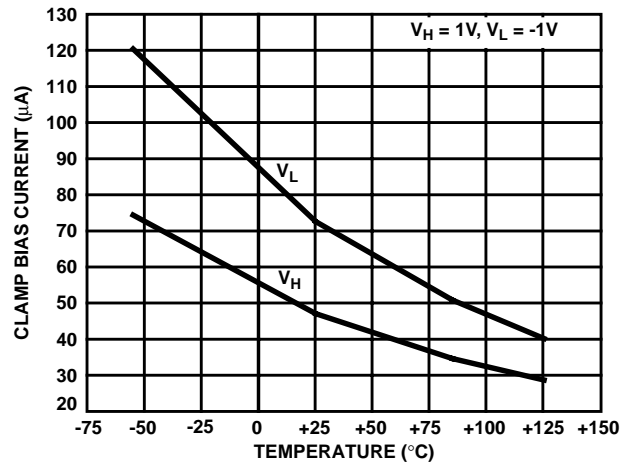
OVERDRIVE RECOVERY vs OVERDRIVE



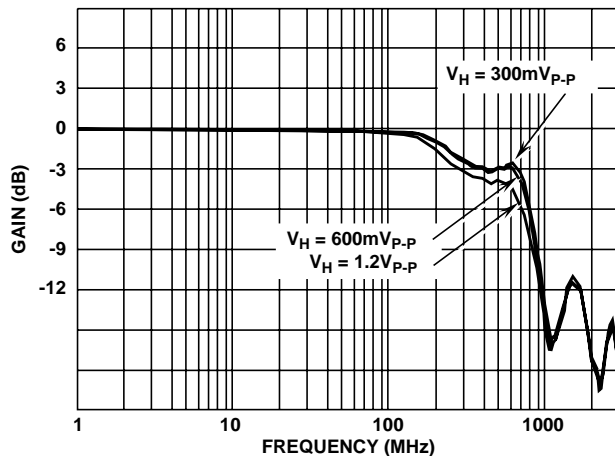
CLAMP ACCURACY vs TEMPERATURE



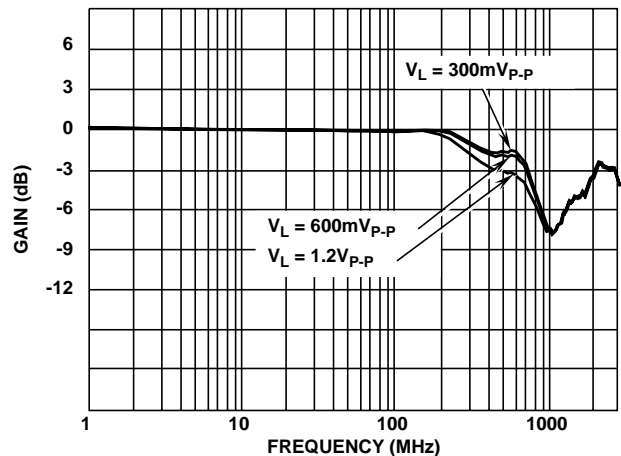
CLAMP BIAS CURRENT vs TEMPERATURE



V_H CLAMP INPUT BANDWIDTH



V_L CLAMP INPUT BANDWIDTH



DESIGN INFORMATION (Continued)

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Application Information

Closed Loop Gain Selection

The HFA1113 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the \pm Inputs. Applying the input signal to +IN and floating -IN selects a gain of +1, while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1	Input	NC (Floating)
+2	Input	GND

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10 μ F) tantalum in parallel with a small value (0.1 μ F) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at $A_V = +1$, $R_S = 50\Omega$, $C_L = 30\text{pF}$, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at $A_V = +1$, $R_S = 5\Omega$, $C_L = 340\text{pF}$.

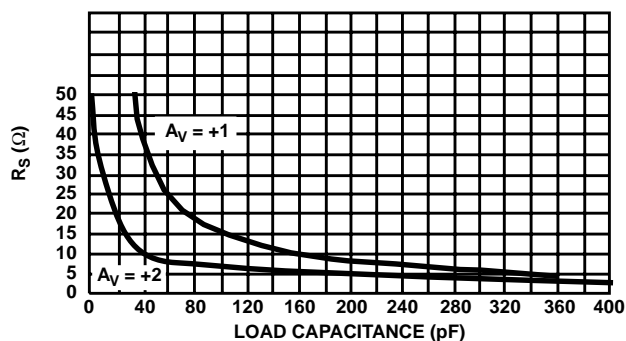


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs. LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1113 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

1. Remove the 500 Ω feedback resistor (R2), and leave the connection open.
2. A. For $A_V = +1$ evaluation, remove the 500 Ω gain setting resistor (R1), and leave pin 2 floating.
B. For $A_V = +2$, replace the 500 Ω gain setting resistor with a 0 Ω resistor to GND.

The layout and modified schematic of the board are shown in Figure 2.

To order evaluation boards, please contact your local sales office.

DESIGN INFORMATION (Continued)

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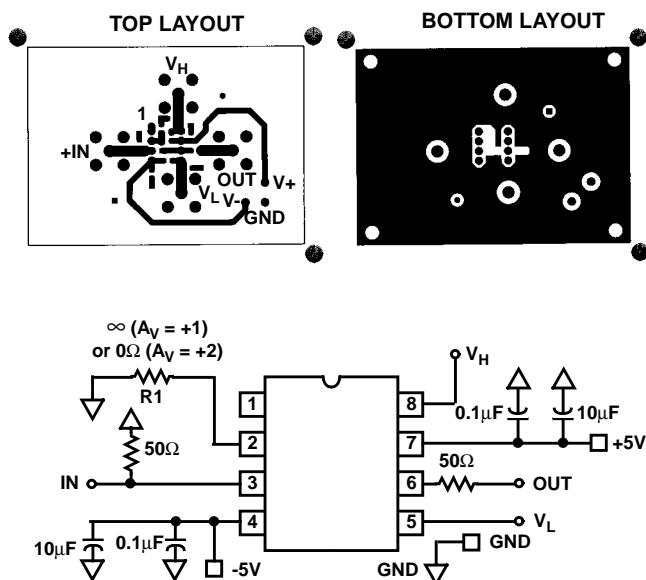


FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

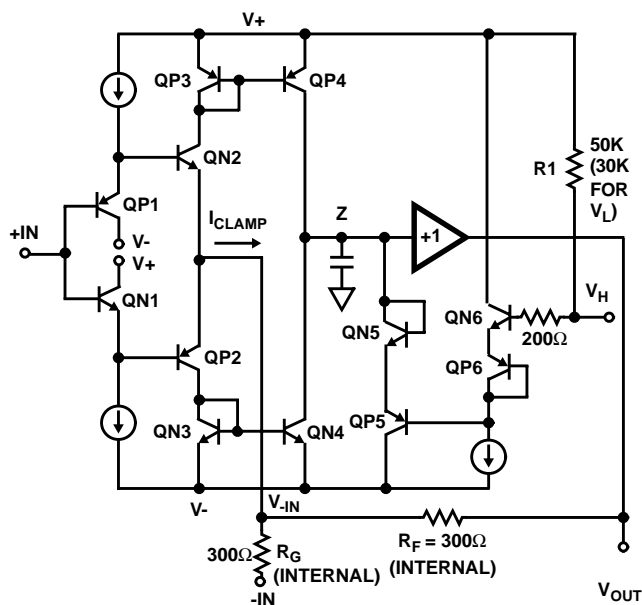


FIGURE 3. HFA1113 SIMPLIFIED V_H CLAMP CIRCUITRY

Clamp Operation

General

The HFA1113 features user programmable output clamps to limit output voltage excursions. Clamping action is obtained by applying voltages to the V_H and V_L terminals (DIP pins 8 & 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H , or below V_L , the clamp circuitry limits the output voltage at V_H or V_L (\pm the clamp accuracy), respectively. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

Clamp Circuitry

Figure 3 shows a simplified schematic of the HFA1113 input stage, and the high clamp (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (QX1 - QX2) between the positive and negative inputs. This buffer forces $-IN$ to track $+IN$, and sets up a slewing current of:

$$(V_{-IN} - V_{OUT})/R_F + V_{-IN}/R_G.$$

This current is mirrored onto the high impedance node (Z) by QX3-QX4, where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by QP4 and QN4. Note that when the output reaches its quiescent value, the current flowing through $-IN$ is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.

Tracing the path from V_H to Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (QN6 and QP6) to set up the base voltage on QP5.

QP5 begins to conduct whenever the high impedance node reaches a voltage equal to QP5's base voltage + $2V_{BE}$ (QP5 and QN5). Thus, QP5 clamps node Z whenever Z reaches V_H . R1 provides a pull-up network to ensure functionality with the clamp inputs floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L .

When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. QP5 must sink this current while clamping, because the $-IN$ current is always mirrored onto the high impedance node. The clamping current is calculated as:

$$I_{CLAMP} = (V_{-IN} - V_{OUT\ CLAMPED}) / 300\Omega + V_{-IN} / R_G.$$

As an example, a unity gain circuit with $V_{-IN} = 2V$, and $V_H = 1V$, would have $I_{CLAMP} = (2V-1V) / 300\Omega + 2V / \infty = 3.33mA$ ($R_G = \infty$ because $-IN$ is floated for unity gain applications). Note that I_{CC} will increase by I_{CLAMP} when the output is clamp limited.

Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L . Offset errors, mostly due to V_{BE} mismatches, necessitate a clamp accuracy parameter which is found in the device specifications. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 3, it can be seen that one component of clamp accuracy is the V_{BE} mismatch between the QX6 transistors, and the QX5 transistors. If the transistors always ran at the same current level there would be no V_{BE} mismatch, and no contribution to the inaccuracy. The QX6 transistors are biased at a constant current, but as described earlier, the current through QX5 is equivalent to I_{CLAMP} . V_{BE} increases as I_{CLAMP} increases,

DESIGN INFORMATION (Continued)

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causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level ($A_{VCL} \times V_{IN} - V_{OUT\ CLAMPED}$), so clamp accuracy degrades as the overdrive increases. As an example, the specified accuracy of $\pm 100\text{mV}$ for a 1.6X overdrive degrades to $\pm 240\text{mV}$ for a 3X overdrive.

Consideration must also be given to the fact that the clamp voltages have an affect on amplifier linearity. The "Nonlinearity Near Clamp Voltage" curve in the data sheet illustrates the impact of several clamp levels on linearity.

Clamp Range

Unlike some competitor devices, both V_H and V_L have usable ranges that cross 0V. While V_H must be more positive than V_L , both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1113 could be limited to ECL output levels by setting $V_H = -0.8\text{V}$ and $V_L = -1.8\text{V}$. V_H and V_L may be connected to the same voltage (GND for instance) but the result won't be a DC output voltage from an AC input signal. A 150 - 200mV AC signal will still be present at the output.

Recovery from Overdrive

The output voltage remains at the clamp level as long as the overdrive condition remains. When the input voltage drops below the overdrive level (V_{CLAMP} / A_{VCL}) the amplifier will return to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The plots of "Unclamped Performance" and "Clamped Performance" highlight the HFA1113's subnanosecond recovery time. The difference between the unclamped and clamped propagation delays is the overdrive recovery time. The appropriate propagation delays are 8.0ns for the unclamped pulse, and 8.8ns for the clamped (2X overdrive) pulse yielding an overdrive recovery time of 800ps. The measurement uses the 90% point of the output transition to ensure that linear operation has resumed. Note: The propagation delay illustrated is dominated by the fixturing. The delta shown is accurate, but the true HFA1113 propagation delay is 500ps.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: $V_{SUPPLY} = \pm 5\text{V}$, $A_V = +2\text{V/V}$, $R_L = 100\Omega$, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	UNITS
Output Offset Voltage	$A_V = +1$, $V_{CM} = 0\text{V}$	+25°C	8	mV
Average Offset Voltage Drift	Versus Temperature	Full	10	$\mu\text{V}/^\circ\text{C}$
+Input Current	$A_V = +1$, $V_{CM} = 0\text{V}$	+25°C	25	μA
+Input Resistance	$A_V = +1$, $\Delta V_{CM} = 2\text{V}$	+25°C	50	k Ω
-Input Resistance		+25°C	300	Ω
+Input Noise Voltage *	$f = 100\text{kHz}$	+25°C	9	$\text{nV}/\sqrt{\text{Hz}}$
+Input Noise Current *	$f = 100\text{kHz}$	+25°C	37	$\text{pA}/\sqrt{\text{Hz}}$
Input Common Mode Range		Full	± 2.8	V
Input Capacitance		+25°C	2.2	pF
Gain	$A_V = +1$, $V_{IN} = 2\text{V}$	+25°C	0.99	V/V
Gain	$A_V = +2$, $V_{IN} = 1\text{V}$	+25°C	1.98	V/V
DC Non-Linearity *	$V_{OUT} = \pm 2\text{V}$ Full Scale	+25°C	0.02	%
Output Voltage *	$A_V = -1$, $R_L = 100\Omega$	+25°C	± 3.3	V
	$A_V = -1$, $R_L = 100\Omega$	Full	± 3.0	V
Output Current *	$A_V = -1$, $R_L = 50\Omega$	+25°C to +125°C	± 60	mA
	$A_V = -1$, $R_L = 50\Omega$	-55°C to 0°C	± 50	mA
DC Closed Loop Output Resistance		+25°C	0.3	Ω
Quiescent Supply Current *	$R_L = \text{Open}$	Full	24	mA
-3dB Bandwidth *	$A_V = -1$, $V_{OUT} = 200\text{mV}_{P-P}$	+25°C	800	MHz
	$A_V = +1$, $V_{OUT} = 200\text{mV}_{P-P}$	+25°C	850	MHz
	$A_V = +2$, $V_{OUT} = 200\text{mV}_{P-P}$	+25°C	550	MHz

DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: $V_{\text{SUPPLY}} = \pm 5\text{V}$, $A_V = +2\text{V/V}$, $R_L = 100\Omega$, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	UNITS
Slew Rate	$A_V = -1$, $V_{\text{OUT}} = 5V_{\text{P-P}}$	+25°C	2400	V/ μs
	$A_V = +1$, $V_{\text{OUT}} = 5V_{\text{P-P}}$	+25°C	1500	V/ μs
	$A_V = +2$, $V_{\text{OUT}} = 5V_{\text{P-P}}$	+25°C	1900	V/ μs
Full Power Bandwidth (Note 1)	$A_V = -1$, $V_{\text{OUT}} = 5V_{\text{P-P}}$	+25°C	300	MHz
	$A_V = +1$, $V_{\text{OUT}} = 5V_{\text{P-P}}$	+25°C	150	MHz
	$A_V = +2$, $V_{\text{OUT}} = 5V_{\text{P-P}}$	+25°C	220	MHz
Gain Flatness (Note 1)	To 30MHz, $A_V = -1$	+25°C	± 0.02	dB
	To 30MHz, $A_V = +1$	+25°C	± 0.10	dB
	To 30MHz, $A_V = +2$	+25°C	± 0.015	dB
Gain Flatness (Note 1)	To 50MHz, $A_V = -1$	+25°C	± 0.05	dB
	To 50MHz, $A_V = +1$	+25°C	± 0.20	dB
	To 50MHz, $A_V = +2$	+25°C	± 0.036	dB
Gain Flatness (Note 1)	To 100MHz, $A_V = -1$	+25°C	± 0.10	dB
	To 100MHz, $A_V = +2$	+25°C	± 0.07	dB
Linear Phase Deviation (Note 1)	To 100MHz, $A_V = -1$	+25°C	± 0.13	Degrees
	To 100MHz, $A_V = +1$	+25°C	± 0.83	Degrees
	To 100MHz, $A_V = +2$	+25°C	± 0.05	Degrees
2nd Harmonic Distortion (Note 1)	30MHz, $A_V = -1$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-52	dBc
	30MHz, $A_V = +1$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-57	dBc
	30MHz, $A_V = +2$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-52	dBc
3rd Harmonic Distortion (Note 1)	30MHz, $A_V = -1$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-71	dBc
	30MHz, $A_V = +1$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-73	dBc
	30MHz, $A_V = +2$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-72	dBc
2nd Harmonic Distortion (Note 1)	50MHz, $A_V = -1$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-47	dBc
	50MHz, $A_V = +1$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-53	dBc
	50MHz, $A_V = +2$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-47	dBc
3rd Harmonic Distortion (Note 1)	50MHz, $A_V = -1$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-63	dBc
	50MHz, $A_V = +1$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-68	dBc
	50MHz, $A_V = +2$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-65	dBc
2nd Harmonic Distortion (Note 1)	100MHz, $A_V = -1$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-41	dBc
	100MHz, $A_V = +1$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-50	dBc
	100MHz, $A_V = +2$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-42	dBc
3rd Harmonic Distortion (Note 1)	100MHz, $A_V = -1$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-55	dBc
	100MHz, $A_V = +1$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-49	dBc
	100MHz, $A_V = +2$, $V_{\text{OUT}} = 2V_{\text{P-P}}$	+25°C	-62	dBc

DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: $V_{SUPPLY} = \pm 5V$, $A_V = +2V/V$, $R_L = 100\Omega$, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	UNITS
3rd Order Intercept (Note 1)	100MHz	+25°C	28	dBm
	300MHz	+25°C	13	dBm
1dB Compression (Note 1)	100MHz	+25°C	19	dBm
	300MHz	+25°C	12	dBm
Reverse Isolation (S_{12}) (Note 1)	40MHz	+25°C	-70	dB
	100MHz	+25°C	-60	dB
	600MHz	+25°C	-32	dB
Rise and Fall Time	$A_V = -1$, $V_{OUT} = 0.5V_{P-P}$	+25°C	500	ps
	$A_V = +1$, $V_{OUT} = 0.5V_{P-P}$	+25°C	480	ps
	$A_V = +2$, $V_{OUT} = 0.5V_{P-P}$	+25°C	700	ps
Overshoot (Note 1)	$A_V = -1$, $V_{OUT} = 0.5V_{P-P}$	+25°C	12	%
	$A_V = +1$, $V_{OUT} = 0.5V_{P-P}$	+25°C	45	%
	$A_V = +2$, $V_{OUT} = 0.5V_{P-P}$	+25°C	6	%
Settling Time (Note 1)	$A_V = +2$, to 0.1%, $V_{OUT} = 2V$ to 0V	+25°C	13	ns
	$A_V = +2$, to 0.05%, $V_{OUT} = 2V$ to 0V	+25°C	20	ns
	$A_V = +2$, to 0.02%, $V_{OUT} = 2V$ to 0V	+25°C	36	ns
Differential Gain	$A_V = +2$, $R_L = 150\Omega$, NTSC	+25°C	0.02	%
Differential Phase	$A_V = +2$, $R_L = 150\Omega$, NTSC	+25°C	0.04	Degrees
Overdrive Recovery Time, (2X Overdrive)	$V_{IN} = \pm 1V$, $V_H = +1V$, $V_L = -1V$	+25°C	0.75	ns
Clamp Accuracy	$A_V = -1$, $V_{IN} = \pm 1.6V$, $V_H = +1V$, $V_L = -1V$	+25°C	± 100	mV
Clamped Overshoot	$V_{IN} = \pm 1V$, $V_H = +1V$, $V_L = -1V$, Input $t_R / t_F = 2ns$	+25°C	7	%
Negative Clamp Range (V_L)		+25°C	-5.0 to +2.0	V
Positive Clamp Range (V_H)		+25°C	-2.0 to +5.0	V
Clamp Input Bias Current	$V_H = +1V$, $V_L = -1V$	+25°C	50	μA
Clamp Input Bandwidth	$V_{IN} = \pm 100mV$, V_H or $V_L = 100mV_{P-P}$	+25°C	500	MHz

NOTE:

1. See Typical Performance Curves for more information.

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