PRELIMINARY

Integrated
Circuit
Systems, Inc.

ICS8421004I-01

FemtoClocks™ Crystal-to-HSTL Frequency Synthesizer

General Description

The ICS8421004I-01 is a 4 output HSTL Synthesizer optimized to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 25MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 156.25MHz, 125MHz and 62.5MHz. The ICS8421004I-01 uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS8421004I-01 is packaged in a small 24-pin TSSOP package.

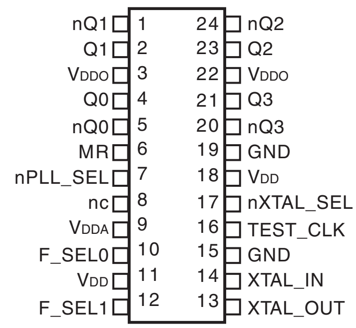
Features

- Four HSTL outputs (VOHmax = 1.4V)
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 156.25MHz, 125MHz, 62.5MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.44ps (typical)
- Power supply modes:
  Core/Output
  3.3V/1.8V
  2.5V/1.8V
- -40°C to 85°C ambient operating temperature

Frequency Select Function Table

F_SEL1	F_SEL0	M Divider Value	N Divider Value	M/N Divider Value	Output Frequency (25MHz Ref.)
0	0	25	4	6.25	156.25
0	1	25	5	5	125
1	0	25	10	2.5	62.5
1	1	25	not used		not used

Pin Assignment



ICS8421004I-01
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

Block Diagram

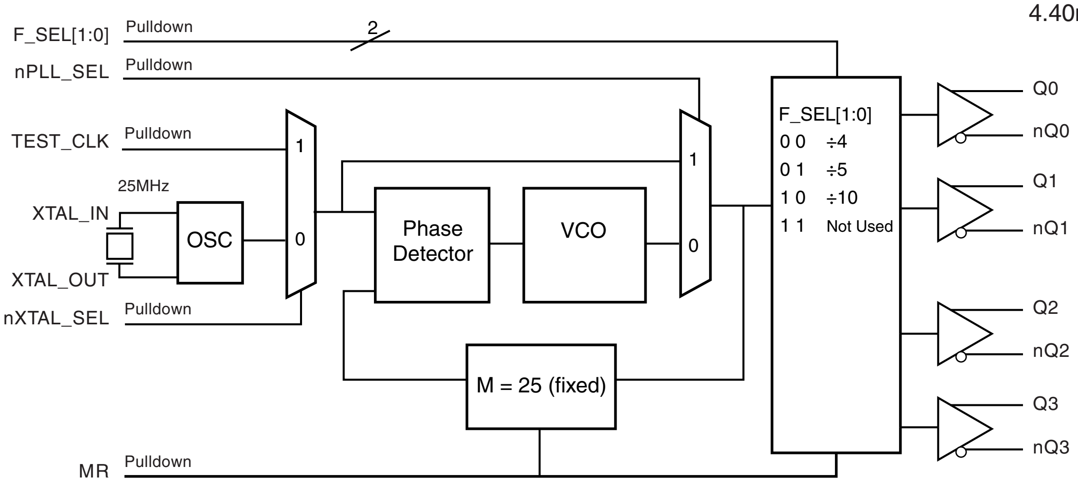


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential output pair. HSTL interface levels.
3, 22	V_{DDO}	Power		Output supply pins.
4, 5	Q0, nQ0	Ouput		Differential output pair. HSTL interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	Selects between the PLL and TEST_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
8, 18	nc	Unused		No connect.
9	V_{DDA}	Power		Analog supply pin.
10, 12	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
11	V_{DD}	Power		Core supply pin.
13, 14	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
15, 19	GND	Power		Power supply ground.
16	TEST_CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
17	nXTAL_SEL	Input	Pulldown	Selects between crystal or TEST_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects TEST_CLK when HIGH. LVCMOS/LVTTL interface levels.
20, 21	nQ3, Q3	Output		Differential output pair. HSTL interface levels.
23, 24	Q2, nQ2	Output		Differential output pair. HSTL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			90		mA
I_{DDA}	Analog Supply Current			10		mA
I_{DDO}	Output Supply Current	No Load		0		mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 2.5V±5%, V_{DDO} = 1.8V±0.2V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			80		mA
I_{DDA}	Analog Supply Current			10		mA
I_{DDO}	Output Supply Current	No Load		0		mA

TABLE 3C. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±5% OR 2.5V±5%, V_{DDO} = 1.8V±0.2V, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	TEST_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL	$V_{DD} = V_{IN}$ = 3.465V or 2.5V			150	µA
I_{IL}	Input Low Current	TEST_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL	V_{DD} = 3.465V or 2.5V, V_{IN} = 0V	-150			µA

TABLE 3D. HSTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%, V_{DDO} = 1.8V±0.2V$, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1.0		1.4	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage; NOTE 2		40		60	%
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: Outputs terminated with 50Ω to ground.
NOTE 2: Defined with respect to output voltage swing at a given condition.

TABLE 3E. HSTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V±5\%, V_{DDO} = 1.8V±0.2V$, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1.0		1.4	V
V_{OL}	Output Low Voltage; NOTE 1			0.235		V
V_{OX}	Output Crossover Voltage; NOTE 2		40		60	%
V_{SWING}	Peak-to-Peak Output Voltage Swing			0.9		V

NOTE 1: Outputs terminated with 50Ω to ground.
NOTE 2: Defined with respect to output voltage swing at a given condition.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		22.4	25	27.2	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $_{DD}$ = V_{DDA} = 3.3V±5%,V_{DDO} = 1.8V±0.2V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	140		170	MHz
		F_SEL[1:0] = 01	112		136	MHz
		F_SEL[1:0] = 10	56		68	MHz
*t*sk(o)	Output Skew; NOTE 1, 3			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	156.25MHz, (1.875MHz - 20MHz)		0.44		ps
		125MHz, (1.875MHz - 20MHz)		0.48		ps
		62.5MHz,(1.875MHz - 20MHz)		0.49		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		450		ps
odc	Output Duty Cycle			50		%

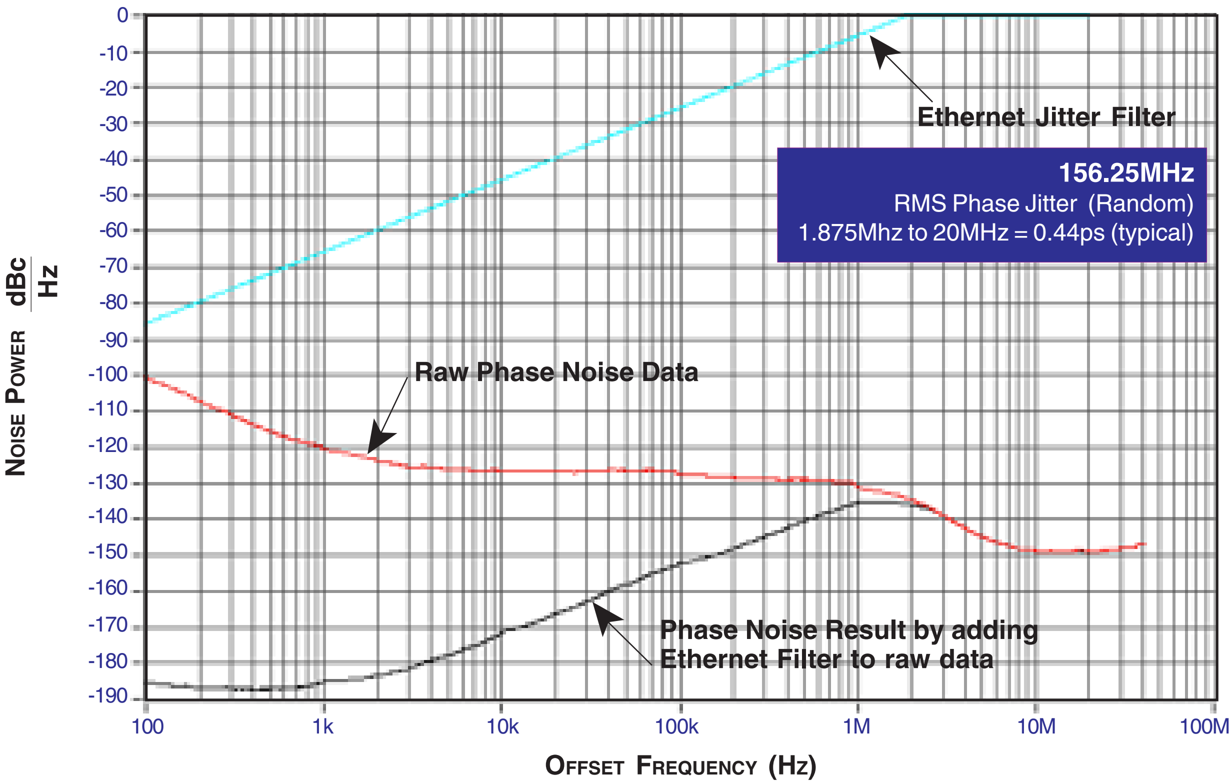
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at V_{DDO}/2.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = V_{DDA} = 2.5V±5%, V_{DDO} = 1.8V±0.2V, TA = -40°C TO 85°C

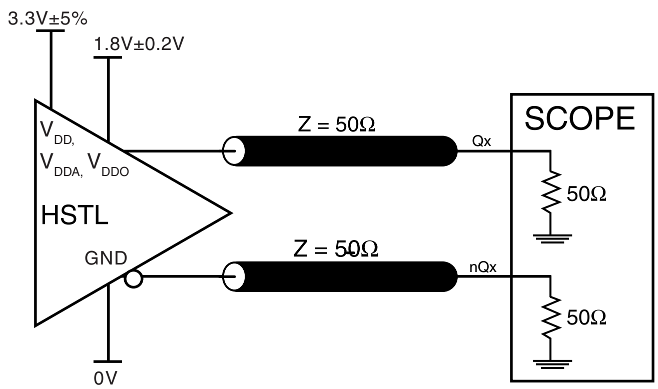
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	140		170	MHz
		F_SEL[1:0] = 01	112		136	MHz
		F_SEL[1:0] = 10	56		68	MHz
*t*sk(o)	Output Skew; NOTE 1, 3			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	156.25MHz, (1.875MHz - 20MHz)		0.41		ps
		125MHz, (1.875MHz - 20MHz)		0.49		ps
		62.5MHz,(1.875MHz - 20MHz)		0.50		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		420		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at V_{DDO}/2.
NOTE 2 Please refer to the Phase Noise Plot.
NOTE 3 This parameter is defined in accordance with JEDEC Standard 65.

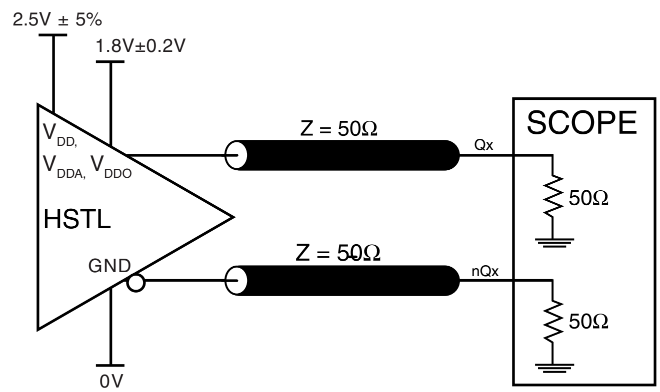
TYPICAL PHASE NOISE AT 156.25MHZ



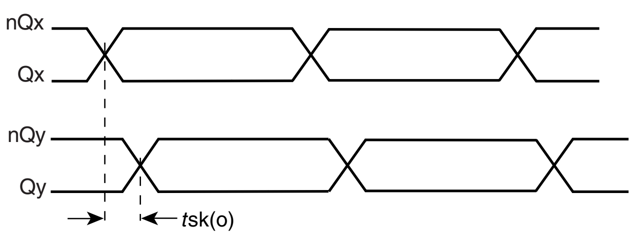
PARAMETER MEASUREMENT INFORMATION



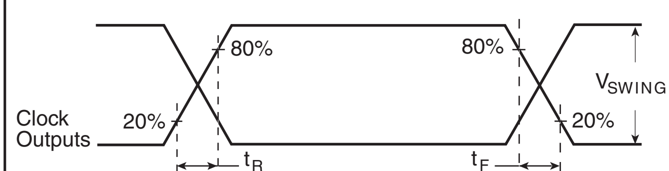
HSTL 3.3V OUTPUT LOAD AC TEST CIRCUIT



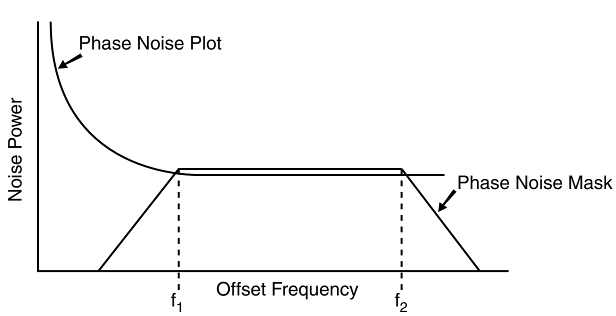
HSTL 2.5V OUTPUT LOAD AC TEST CIRCUIT



OUTPUT SKEW

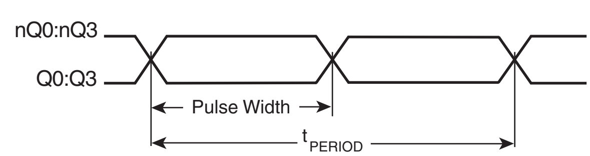


OUTPUT RISE/FALL TIME



$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

RMS PHASE JITTER



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8421004I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

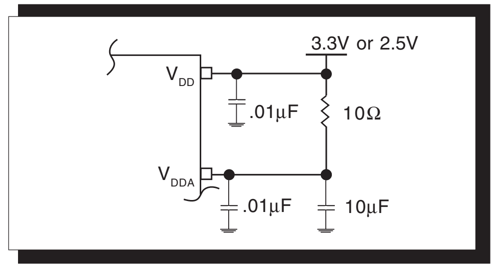


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS8421004I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

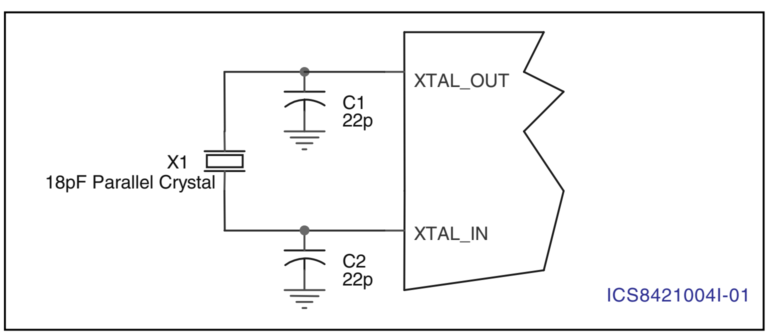


Figure 2. CRYSTAL INPUT INTERFACE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS821004I-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8421004I-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 100mA = **346.5mW**
- Power (outputs)$_{MAX}$ = **32.8mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 x 32.8mW = **131.2mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 346.5mW + 131.2mW = **477.7mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 linear meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.478W * 65°C/W = 99.85°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 24-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 3.*

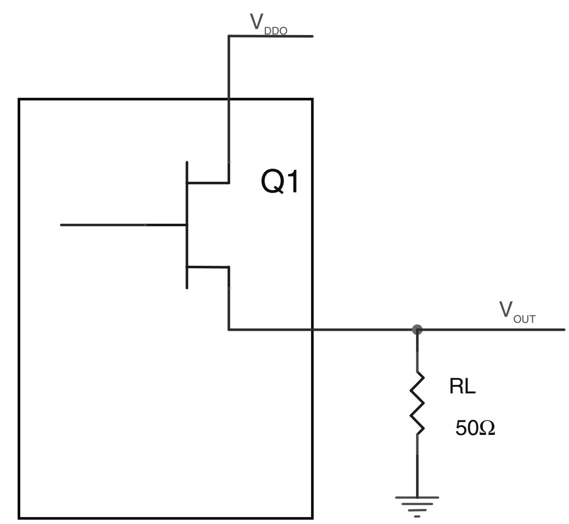


FIGURE 3. HSTL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$$Pd\_H = (V_{OH\_MIN}/R_L) * (V_{DD\_MAX} - V_{OH\_MIN})$$

$$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DD\_MAX} - V_{OL\_MAX})$$

Pd_H = (1V/50Ω) * (2V - 1V) = **20mW**

Pd_L = (0.4V/50Ω) * (2V - 0.4V) = **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.8mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS8421004I-01 is: 2951

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

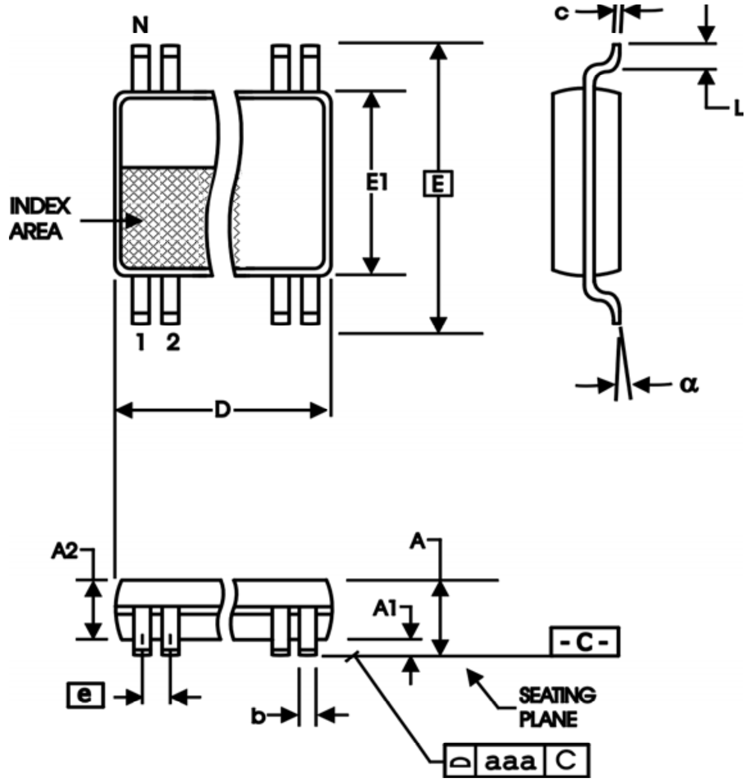


TABLE 8 PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8421004AGI-01	ICS421004AI01	24 Lead TSSOP	60 per tube	-40°C to 85°C
ICS8421004AGI-01T	ICS421004AI01	24 Lead TSSOP on Tape and Reel	2500	-40°C to 85°C