



3.3V CMOS 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVC162525

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4 μ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP, TSSOP, and TVSOP packages

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$ (A port)
- Balanced Output Drivers: $\pm 12mA$ (B port)

APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

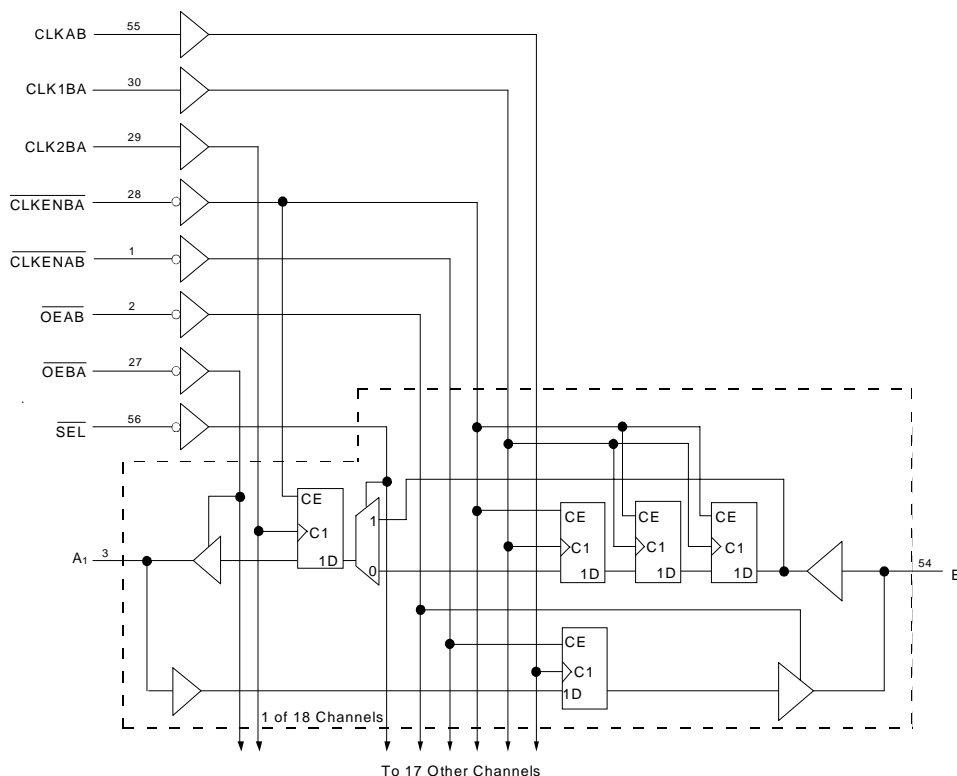
This 18-bit registered bus transceiver is built using advanced dual metal CMOS technology. Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}) and clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of the select (\overline{SEL}) input. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate \overline{CLKEN} inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

The ALVCH162525 has series resistors in the device output structure of the "B" port which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12mA$ at the designated threshold levels. The "A" port has a $\pm 24mA$ driver.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The ALVCH162525 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

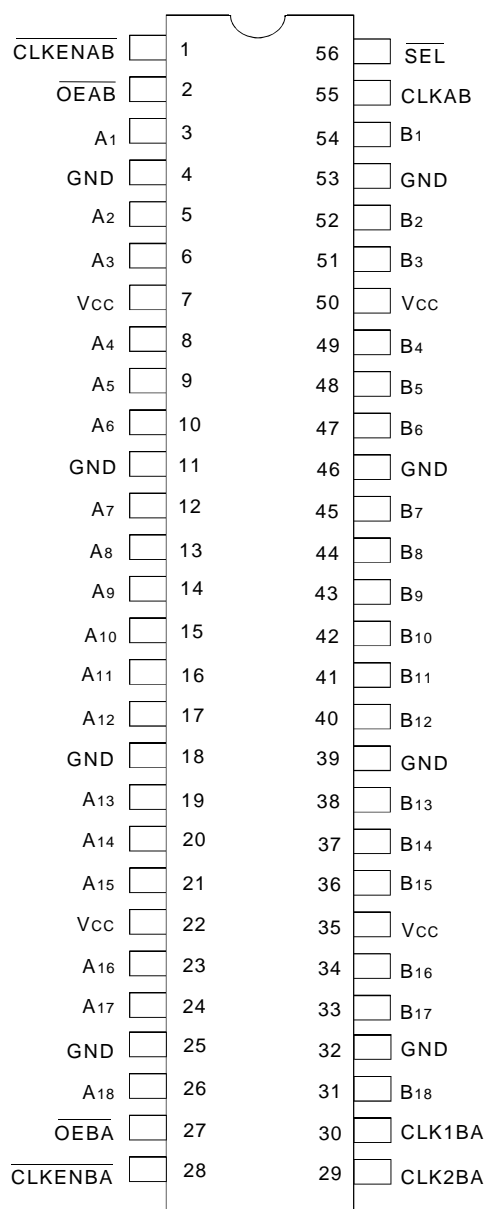


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INDUSTRIAL TEMPERATURE RANGE

MARCH 1999

PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	±50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	-50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{OUT}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
CLKAB	Clock Input for the A to B direction
CLK1BA	Clock Input for the B to A pipeline register
CLK2BA	Clock Input for the B to A output register
CLKENBA	Clock Enable for the CLK1BA and CLK2BA clocks (Active LOW)
CLKENAB	Clock Enable for the CLKAB clock (Active LOW)
OEAB	Output Enable for the B port (Active LOW)
OEBA	Output Enable for the A port (Active LOW)
SEL	Select pin for pipelined/non-pipelined mode in the B-to-A direction (Active LOW)
A x	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
B x	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE⁽¹⁾

A-TO-B STORAGE ($\overline{OEAB} = L$)

Inputs			Outputs
$\overline{CLKENAB}$	CLKAB	Ax	Bx
H	X	X	B ₀ ⁽²⁾
L	↑	L	L
L	↑	H	H

B-TO-A STORAGE ($\overline{OEB\bar{A}} = L$)

Inputs					Outputs
$\overline{CLKENBA}$	CLK2BA	CLK1BA	\overline{SEL}	Bx	Ax
H	X	X	X	X	A ₀ ⁽²⁾
L	↑	X	H	L	L
L	↑	X	H	H	H
L	↑	↑	L	L	L ⁽³⁾
L	↑	↑	L	H	H ⁽³⁾

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
- Output level before the indicated steady-state input conditions were established
- Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when \overline{SEL} is low.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	V _{CC} = 3.6V	V _I = V _{CC}	—	—	±5	μA
I _{IL}	Input LOW Current	V _{CC} = 3.6V	V _I = GND	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = V _{CC}	—	—	±10	μA
			V _O = GND	—	—	±10	
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = 3.6V V _{IN} = GND or V _{CC}		—	0.1	40	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	750	μA

NOTE:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 3V	V _I = 2V	-75	—	—	μA
			V _I = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	-45	—	—	μA
			V _I = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	±500	μA

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS (A PORT)

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = -12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3V		2.4	—	
				V _{CC} = 3V	I _{OH} = -24mA	
VOL	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3V	I _{OL} = 24mA	—	0.55	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OUTPUT DRIVE CHARACTERISTICS (B PORT)

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -4mA	1.9	—	
			I _{OH} = -6mA	1.7	—	
		V _{CC} = 2.7V	I _{OH} = -4mA	2.2	—	
			I _{OH} = -8mA	2	—	
				V _{CC} = 3V	I _{OH} = -6mA	
			I _{OH} = -12mA	2	—	
VOL	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 6mA	—	0.55	
		V _{CC} = 2.7V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 8mA	—	0.6	
				V _{CC} = 3V	I _{OL} = 6mA	
			I _{OL} = 12mA	—	0.8	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	$V_{CC} = 2.5V \pm 0.2V$	$V_{CC} = 3.3V \pm 0.3V$	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	$C_L = 0\text{pF}$, $f = 10\text{MHz}$	—	160	pF
CPD	Power Dissipation Capacitance Outputs disabled		—	160	

SWITCHING CHARACTERISTICS (FOR A AND B PORTS)⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		120	—	125	—	150	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CLKAB to 2Bx	1	5.5	—	5.4	1	4.7	ns
t_{PLH} t_{PHL}	Propagation Delay CLK2BA to Ax	1	4.5	—	4.4	1	4.2	ns
t_{PZH} t_{PZL}	Output Enable Time \overline{OEAB} to Bx	1	6.7	—	6.8	1	5.7	ns
t_{PZH} t_{PZL}	Output Enable Time \overline{OEBA} to Ax	1	6.1	—	6.1	1	5.1	ns
t_{PHZ} t_{PLZ}	Output Disable Time \overline{OEAB} to Bx	1	6.3	—	5.4	1	4.9	ns
t_{PHZ} t_{PLZ}	Output Disable Time \overline{OEBA} to Ax	1	6.3	—	5.4	1	4.9	ns
t_{SU}	Set-up Time, Ax data before CLKAB \uparrow	1.3	—	1.3	—	1.3	—	ns
t_{SU}	Set-up Time, Bx data before CLK2BA \uparrow	2.1	—	1.8	—	1.7	—	ns
t_{SU}	Set-up Time, Bx data before CLK1BA \uparrow	1.3	—	1.2	—	1.1	—	ns
t_{SU}	Set-up Time, \overline{SEL} before CLK2BA \uparrow	3.3	—	3.3	—	3.3	—	ns
t_{SU}	Set-up Time, $\overline{CLKENAB}$ before CLKAB \uparrow	2.1	—	1.9	—	1.6	—	ns
t_{SU}	Set-up Time, $\overline{CLKENBA}$ before CLK1BA \uparrow	2.7	—	2.5	—	2.1	—	ns
t_{SU}	Set-up Time, $\overline{CLKENBA}$ before CLK2BA \uparrow	2.7	—	2.5	—	2.2	—	ns
t_H	Hold Time, Ax data after CLKAB \uparrow	0.7	—	0.4	—	0.9	—	ns
t_H	Hold Time, Bx data before CLK2BA \uparrow	0.4	—	0	—	0.6	—	ns
t_H	Hold Time, Bx data before CLK1BA \uparrow	0.8	—	0.4	—	1	—	ns
t_H	Hold Time, \overline{SEL} before CLK2BA \uparrow	0	—	0	—	0.1	—	ns
t_H	Hold Time, $\overline{CLKENAB}$ before CLKAB \uparrow	0.1	—	0.3	—	0.3	—	ns
t_H	Hold Time, $\overline{CLKENBA}$ before CLK1BA \uparrow	0	—	0	—	0.1	—	ns
t_H	Hold Time, $\overline{CLKENBA}$ before CLK2BA \uparrow	0	—	0	—	0	—	ns
t_W	Pulse Duration, CLK HIGH or LOW	3.2	—	3.2	—	3	—	ns
$t_{SK(O)}$	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

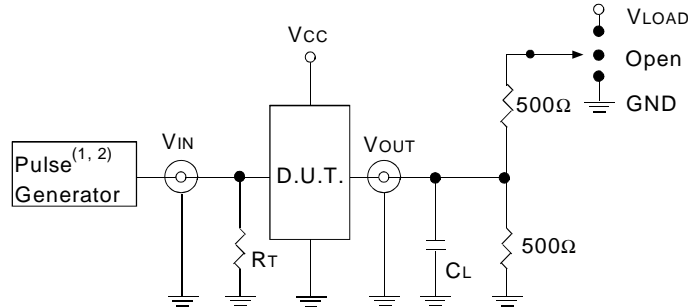
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

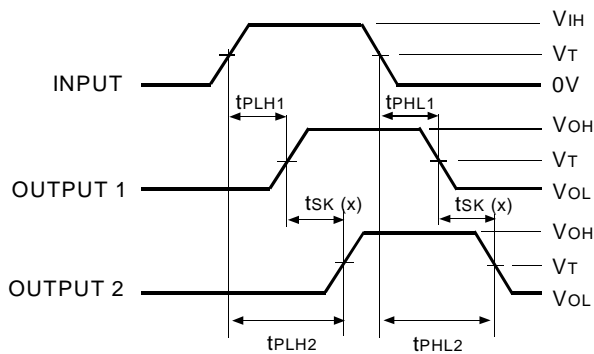
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open

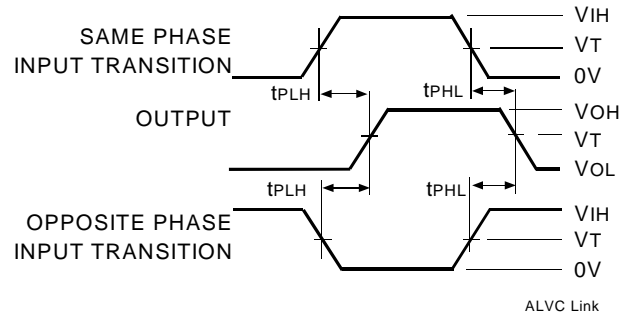


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

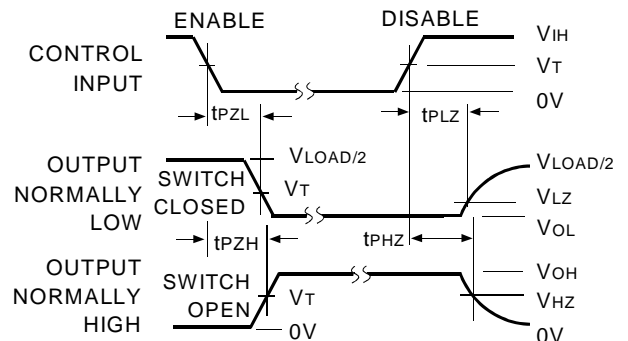
Output Skew - tsk(x)

NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



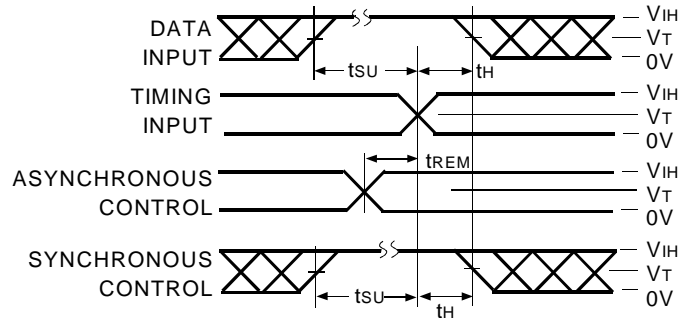
Propagation Delay



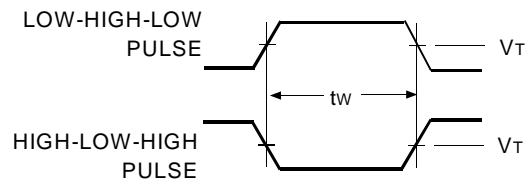
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

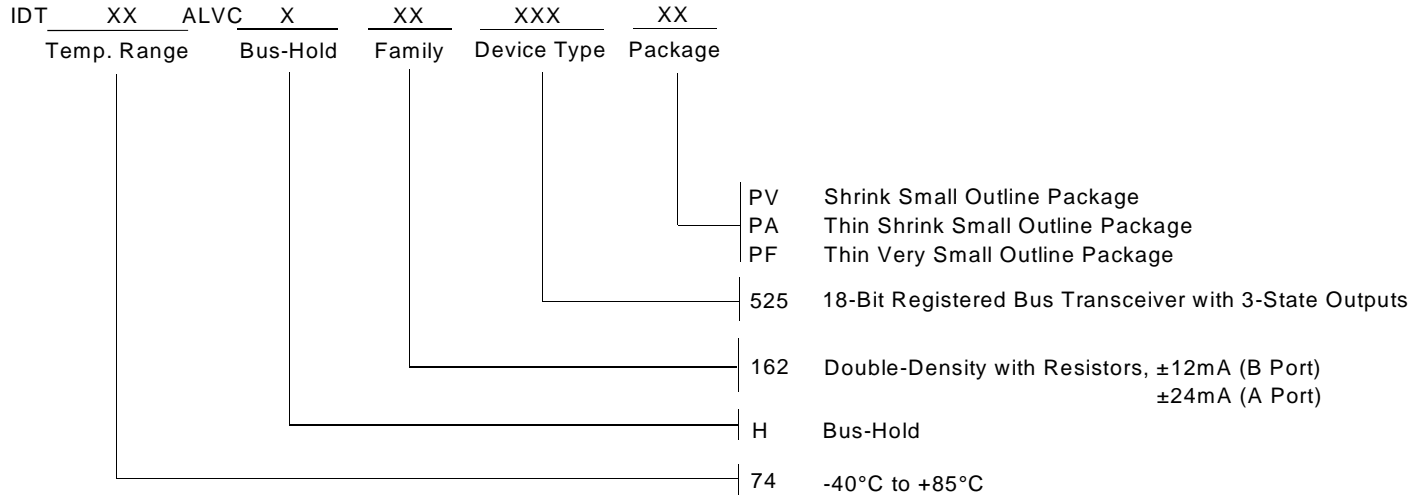


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



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