GENERAL DESCRIPTION

The M2004-04 and its variants are VCSO (Voltage Controlled SAW Oscillator) based clock generator PLLs designed for clock frequency translation and jitter attenuation in a high-speed data communications system. External loop components allow the tailoring of PLL loop response. Includes: a Narrow Bandwidth control input pin (NBW Pin), a Loss of Lock (LOL) output, a Protection Switch Trigger (PST) input, and an external capacitor connection (Cx). Variants of the device add Hitless Switching with Phase Build-out (HS/PBO).

FEATURES

- Ideal for OC-48/192 data clock
- Integrated SAW (surface acoustic wave) delay line
- VCSO frequency from 300 to 700MHz (Specify VCSO center frequency at time of order)
- Low phase jitter of < 0.5ps rms, typical (12kHz to 20MHz or 50kHz to 80MHz)
- Pin-selectable configuration of divider ratios
- Loss of Lock (LOL) output, Narrow Bandwidth input (NBW Pin), Protection Switch Trigger (PST) input, and an external capacitor connection (Cx)
- Hitless Switching with Phase Build-out (HS/PBO) added to the M2004-14 and M2004-24 to ensure SONET/SDH MTIE and TDEV compliance during reference clock reselection
- Differential LVPECL output
- Reference clock inputs support differential LVDS, LVPECL, as well as single-ended LVCMOS, LVTTL
- Industrial temperature available
- Single 3.3V power supply
- Small 9 x 9 mm SMT (surface mount) package

PIN ASSIGNMENT (9 x 9 mm SMT)

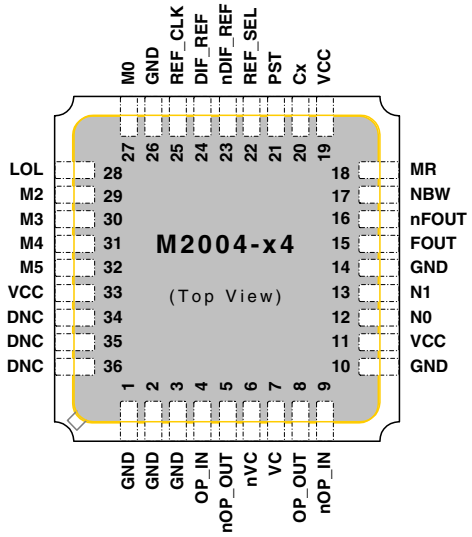

Figure 1: Pin Assignment

Example Input / Output Frequency Combinations

Input Clock (MHz)	VCSO ** Freq (MHz)	Output Freq (MHz)	Application
19.44	622.08	77.76	OC-12 / 48 /192
38.80		155.52	
77.76		311.04	
155.52		622.08	
25.00	625.00	156.25	Gigabit Ethernet

* Series consists of parts numbered M2004-04, -14, and -24.

** Specify VCSO center frequency at time of order.

SIMPLIFIED BLOCK DIAGRAM

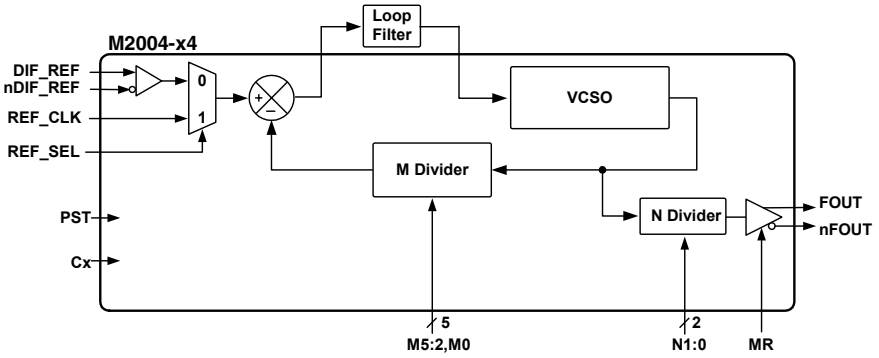

Figure 2: Simplified Block Diagram