

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS M37736MHLXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37736MHLXXXHP is a single-chip microcomputer using the 7700 Family core. This single-chip microcomputer has a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can be an 8-bit parallel processor, and the bus interface unit enhances the memory access efficiency to execute instructions fast. This microcomputer also includes a 32 kHz oscillation circuit, in addition to the ROM, RAM, multiple-function timers, serial I/O, A-D converter, and so on.

Its strong points are the low power dissipation, the low supply voltage, and the small package.

In the M37736MHLXXXHP, as the multiplex method of the external bus, either of 2 types can be selected.

FEATURES

- Number of basic instructions 103
- Memory size ROM 124 Kbytes
 RAM 3968 bytes
- Instruction execution time
 The fastest instruction at 12 MHz frequency 333 ns
- Single power supply 2.7–5.5 V

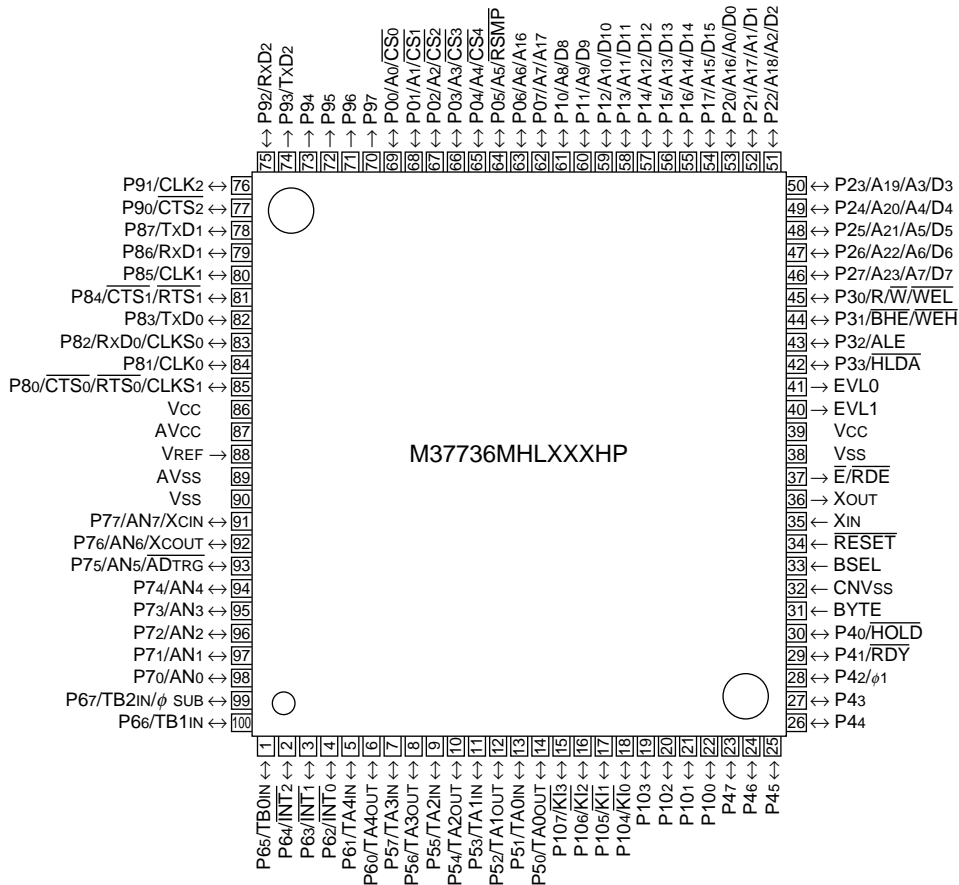
- Low power dissipation (At 3 V supply voltage, 12 MHz frequency) 9 mW (Typ.)
- Interrupts 19 types, 7 levels
- Multiple-function 16-bit timer 5 + 3
- Serial I/O (UART or clock synchronous) 3
- 10-bit A-D converter 8-channel inputs
- 12-bit watchdog timer
- Programmable input/output, output
 (ports P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10) 84
- Clock generating circuit 2 circuits built-in
- Small package 100-pin plastic molded fine-pitch QFP (100P6Q-A; 0.5 mm lead pitch)

APPLICATION

Control devices for general commercial equipment such as office automation, office equipment, personal information equipment, and others.

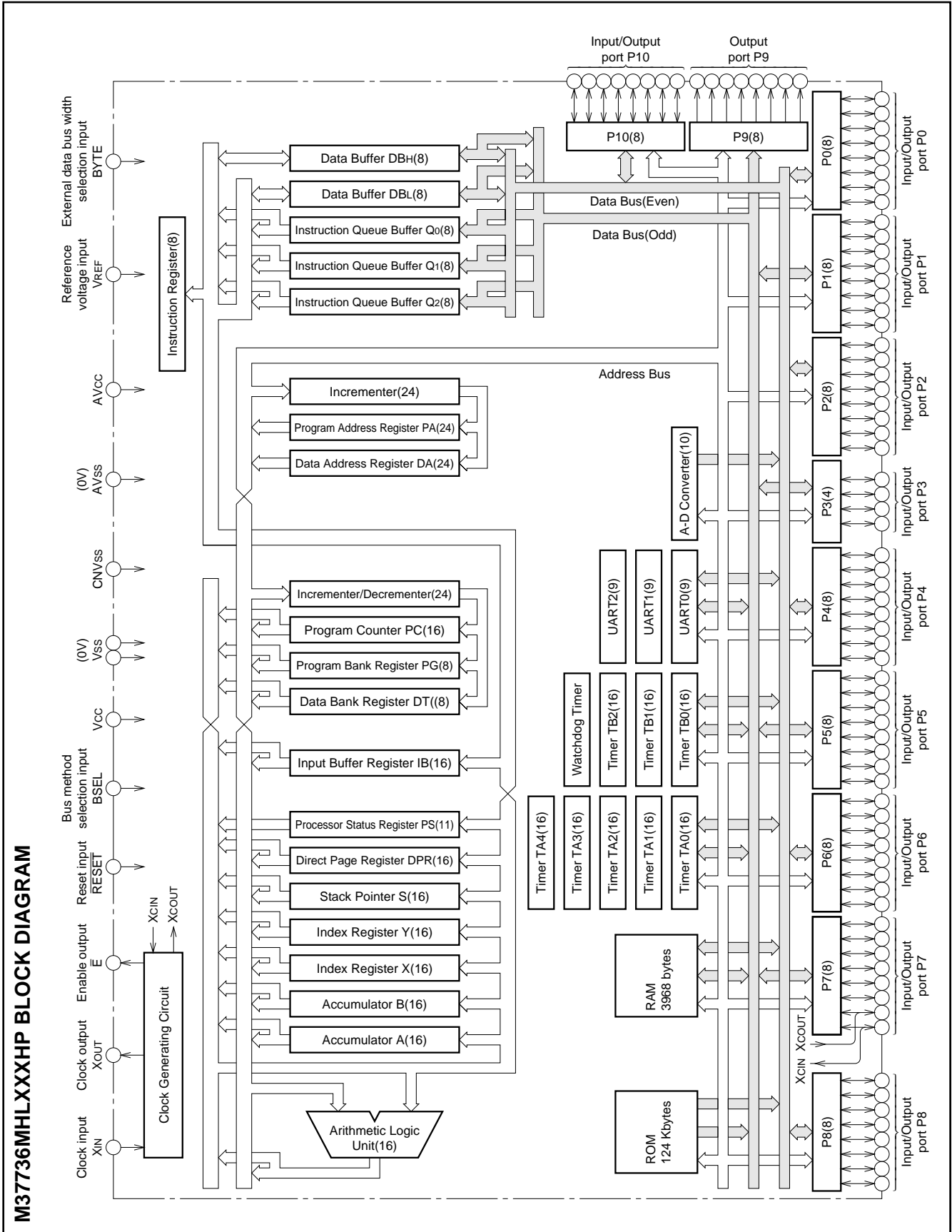
Control devices for general industrial equipment such as communication equipment, and others.

PIN CONFIGURATION (TOP VIEW)



Outline 100P6Q-A

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mitsubishi MICROCOMPUTERS
M37736MHLXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37736MHLXXXHP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		333 ns (the fastest instruction at external clock 12 MHz frequency)
Memory size	ROM	124 Kbytes
	RAM	3968 bytes
Input/Output ports	P0 – P2, P4 – P8, P10	8-bit X 9
	P3	4-bit X 1
Output port	P9	8-bit X 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit X 5
	TB0, TB1, TB2	16-bit X 3
Serial I/O		(UART or clock synchronous serial I/O) X 3
A-D converter		10-bit X 1 (8 channels)
Watchdog timer		12-bit X 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		2.7 – 5.5 V
Power dissipation		9 mW (at 3 V supply voltage, external clock 12 MHz frequency)
		22.5 mW (at 5 V supply voltage, external clock 12 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		External bus mode A; maximum 16 Mbytes, External bus mode B; maximum 1 Mbytes
Operating temperature range		–40 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		100-pin plastic molded fine-pitch QFP (100P6Q-A;0.5 mm lead pitch)

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 2.7 – 5.5 V to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.
RESET	Reset input	Input	When "L" level is applied to this pin, the microcomputer enters the reset state.
XIN	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
E	Enable output	Output	This pin functions as the enable signal output pin which indicates the access status in the internal bus. In the external bus mode B and the memory expansion mode or the microprocessor mode, this pin output signal RDE.
BYTE	External data bus width selection input	Input	In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.
BSEL	Bus method select input	Input	In the memory expansion mode or the microprocessor mode, this pin determines the external bus mode. The bus mode becomes the external bus mode A when "H" signal is input, and the external bus mode B when "L" signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
VREF	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P00 – P07	I/O port P0	I/O	In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset. In the memory expansion mode or the microprocessor mode, these pins output address (A0 – A7) at the external bus mode A, and these pins output signals CS0 – CS4 and RSMP, and addresses (A16, A17) at the external bus mode B.
P10 – P17	I/O port P1	I/O	In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D8 – D15) is input/output or an address (A8 – A15) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A8 – A15) is output.
P20 – P27	I/O port P2	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D0 – D7) is input/output or an address is output. When using the external bus mode A, the address is A16 – A23. When using the external bus mode B, the address is A0 – A7.
P30 – P33	I/O port P3	I/O	In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, R/W, BHE, ALE, and HLDA signals are output at the external bus mode A, and WEL, WEH, ALE, and HLDA signals are output at the external bus mode B.
P40 – P47	I/O port P4	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, P40, P41, and P42 become HOLD and RDY input pins, and a clock ϕ_1 output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, P42 can be selected as an I/O port.
P50 – P57	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3.
P60 – P67	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input (INT0 – INT2) and input pins for timers B0 to B2. P67 also functions as sub-clock ϕ_{SUB} output pin.
P70 – P77	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. Additionally, P76 and P77 have the function as the output pin (XCOUT) and the input pin (XCIN) of the sub-clock (32 kHz) oscillation circuit, respectively. When P76 and P77 are used as the XCOUT and XCIN pins, connect a resonator or an oscillator between the both.
P80 – P87	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.
P90 – P97	Output port P9	Output	Port P9 is an 8-bit I/O port. These ports are floating when reset. When writing to the port latch, these ports become the output mode. P90 – P93 also function as I/O port for UART 2.
P100 – P107	I/O port P10	I/O	In addition to having the same functions as port P0 in the single-chip mode. P104 – P107 also function as input pins for key input interrupt input (K10 – K13).
EVL0, EVL1	—————	Output	These pins should be left open.

BASIC FUNCTION BLOCKS

The M37736MHLXXXHP has the same functions as the M37736MHBXXXGP except for the package and the reset circuit. Refer to the section on the M37736MHBXXXGP.

RESET CIRCUIT

The microcomputer is released from the reset state when the RESET pin is returned to "H" level after holding it at "L" level with the power source voltage at 2.7 – 5.5 V. Program execution starts at the address formed by setting address A23 – A16 to 0016, A15 – A8 to the contents of address FFFF16, and A7 – A0 to the contents of address FFFE16. Figure 1 shows an example of a reset circuit. When the stabilized clock is input from the external to the main-clock oscillation circuit, the reset input voltage must be 0.55 V or less when the power source voltage reaches 2.7 V. When a resonator/oscillator is connected to the main-clock oscillation circuit, change the reset input voltage from "L" to "H" after the main-clock oscillation is fully stabilized.

The status of the internal registers during reset is the same as the M37736MHBXXXGP's.

ADDRESSING MODES

The M37736MHLXXXHP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details.

MACHINE INSTRUCTION LIST

The M37736MHLXXXHP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

- (1) M37736MHLXXXHP mask ROM order confirmation form
- (2) 100P6Q mark specification form (100P6D mark specification form is substituted.)
- (3) ROM data (EPROM 3 sets)

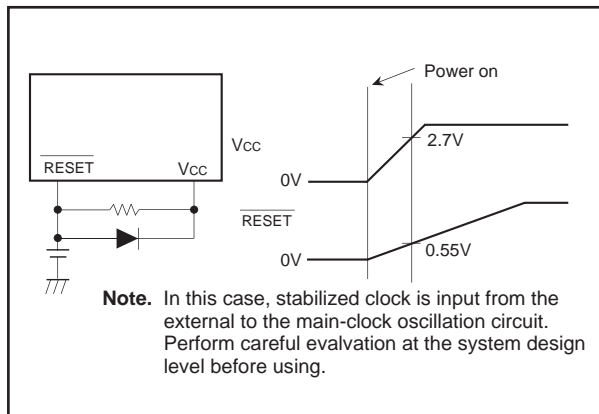


Fig. 1 Example of a reset circuit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Power source voltage		-0.3 to +7	V
AV _{cc}	Analog power source voltage		-0.3 to +7	V
V _i	Input voltage RESET, CNV _{ss} , BYTE		-0.3 to +12	V
V _i	Input voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, V _{REF} , X _{IN} , BSEL		-0.3 to V _{cc} + 0.3	V
V _o	Output voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107, X _{OUT} , E		-0.3 to V _{cc} + 0.3	V
P _d	Power dissipation	T _a = 25 °C	200	mW
T _{opr}	Operating temperature		-40 to +85	°C
T _{stg}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (V_{cc} = 2.7 – 5.5 V, T_a = -40 to +85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V _{cc}	Power source voltage	f(X _{IN}) : Operating	2.7		5.5	V
		f(X _{IN}) : Stopped, f(X _{CIN}) = 32.768 kHz	2.7		5.5	
AV _{cc}	Analog power source voltage			V _{cc}		V
V _{ss}	Power source voltage			0		V
AV _{ss}	Analog power source voltage			0		V
V _{IH}	High-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, X _{IN} , RESET, CNV _{ss} , BYTE, BSEL, X _{CIN} (Note 3)		0.8 V _{cc}		V _{cc}	V
V _{IH}	High-level input voltage P10 – P17, P20 – P27 (in single-chip mode)		0.8 V _{cc}		V _{cc}	V
V _{IH}	High-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)		0.5 V _{cc}		V _{cc}	V
V _{IL}	Low-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, X _{IN} , RESET, CNV _{ss} , BYTE, BSEL, X _{CIN} (Note 3)		0		0.2V _{cc}	V
V _{IL}	Low-level input voltage P10 – P17, P20 – P27 (in single-chip mode)		0		0.2V _{cc}	V
V _{IL}	Low-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)		0		0.16V _{cc}	V
I _{OH(peak)}	High-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107				-10	mA
I _{OH(avg)}	High-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107				-5	mA
I _{OL(peak)}	Low-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P104 – P107				10	mA
I _{OL(peak)}	Low-level peak output current P44 – P47, P100 – P103				16	mA
I _{OL(avg)}	Low-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P104 – P107				5	mA
I _{OL(avg)}	Low-level average output current P44 – P47, P100 – P103				12	mA
f(X _{IN})	Main-clock oscillation frequency (Note 4)				12	MHz
f(X _{CIN})	Sub-clock oscillation frequency			32.768	50	kHz

- Notes**
1. Average output current is the average value of a 100 ms interval.
 2. The sum of I_{OL(peak)} for ports P0, P1, P2, P3, P8, and P9 must be 80 mA or less, the sum of I_{OH(peak)} for ports P0, P1, P2, P3, P8, and P9 must be 80 mA or less, the sum of I_{OL(peak)} for ports P4, P5, P6, P7, and P10 must be 100 mA or less, and the sum of I_{OH(peak)} for ports P4, P5, P6, P7, and P10 must be 80 mA or less.
 3. Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1".
 4. The maximum value of f(X_{IN}) = 6 MHz when the main clock division selection bit = "1".

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -40\text{ to }+85\text{ }^\circ\text{C}$, $f(X_{IN}) = 12\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
V _{OH}	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107	V _{CC} = 5 V, I _{OH} = –10 mA	3			V	
		V _{CC} = 3 V, I _{OH} = –1 mA	2.5				
V _{OH}	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	V _{CC} = 5 V, I _{OH} = –400 μA	4.7			V	
V _{OH}	High-level output voltage P30 – P32	V _{CC} = 5 V, I _{OH} = –10 mA	3.1			V	
		V _{CC} = 5 V, I _{OH} = –400 μA	4.8				
		V _{CC} = 3 V, I _{OH} = –1 mA	2.6				
V _{OH}	High-level output voltage \bar{E}	V _{CC} = 5 V, I _{OH} = –10 mA	3.4			V	
		V _{CC} = 5 V, I _{OH} = –400 μA	4.8				
		V _{CC} = 3 V, I _{OH} = –1 mA	2.6				
V _{OL}	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P43, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P104 – P107	V _{CC} = 5 V, I _{OL} = 10 mA			2	V	
		V _{CC} = 3 V, I _{OL} = 1 mA			0.5		
V _{OL}	Low-level output voltage P44 – P47, P100 – P103	V _{CC} = 5 V, I _{OL} = 16 mA			1.8	V	
		V _{CC} = 3 V, I _{OL} = 10 mA			1.5		
V _{OL}	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	V _{CC} = 5 V, I _{OL} = 2 mA			0.45	V	
V _{OL}	Low-level output voltage P30 – P32	V _{CC} = 5 V, I _{OL} = 10 mA			1.9	V	
		V _{CC} = 5 V, I _{OL} = 2 mA			0.43		
		V _{CC} = 3 V, I _{OL} = 1 mA			0.4		
V _{OL}	Low-level output voltage \bar{E}	V _{CC} = 5 V, I _{OL} = 10 mA			1.6	V	
		V _{CC} = 5 V, I _{OL} = 2 mA			0.4		
		V _{CC} = 3 V, I _{OL} = 1 mA			0.4		
V _{T+} – V _{T–}	Hysteresis $\overline{\text{HOLD}}$, $\overline{\text{RDY}}$, $\overline{\text{TA0IN}}$ – $\overline{\text{TA4IN}}$, $\overline{\text{TB0IN}}$ – $\overline{\text{TB2IN}}$, $\overline{\text{INT0}}$ – $\overline{\text{INT2}}$, $\overline{\text{ADTRG}}$, $\overline{\text{CTS0}}$, $\overline{\text{CTS1}}$, $\overline{\text{CTS2}}$, $\overline{\text{CLK0}}$, $\overline{\text{CLK1}}$, $\overline{\text{CLK2}}$, $\overline{\text{K10}}$ – $\overline{\text{K13}}$	V _{CC} = 5 V	0.4		1	V	
		V _{CC} = 3 V	0.1		0.7		
V _{T+} – V _{T–}	Hysteresis $\overline{\text{RESET}}$	V _{CC} = 5 V	0.2		0.5	V	
		V _{CC} = 3 V	0.1		0.4		
V _{T+} – V _{T–}	Hysteresis X _{IN}	V _{CC} = 5 V	0.1		0.4	V	
		V _{CC} = 3 V	0.06		0.26		
V _{T+} – V _{T–}	Hysteresis X _{CIN} (When external clock is input)	V _{CC} = 5 V	0.1		0.4	V	
		V _{CC} = 3 V	0.06		0.26		
I _{IH}	High-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, X _{IN} , $\overline{\text{RESET}}$, CNV _{SS} , BYTE, BSEL	V _{CC} = 5 V, V _I = 5 V			5	μA	
		V _{CC} = 3 V, V _I = 3 V			4		
I _{IL}	Low-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P53, P60, P61, P65 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P103, X _{IN} , $\overline{\text{RESET}}$, CNV _{SS} , BYTE, BSEL	V _{CC} = 5 V, V _I = 0 V			–5	μA	
		V _{CC} = 3 V, V _I = 0 V			–4		
I _{IL}	Low-level input current P62 – P64, P104 – P107	V _I = 0 V, without a pull-up transistor	V _{CC} = 5 V			–5	μA
			V _{CC} = 3 V			–4	
		V _I = 0 V, with a pull-up transistor	V _{CC} = 5 V	–0.25	–0.5	–1.0	mA
			V _{CC} = 3 V	–0.08	–0.18	–0.35	
V _{RAM}	RAM hold voltage	When clock is stopped.	2			V	

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -40\text{ to }+85\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
I _{CC}	Power source current	When single-chip mode, output pins are open, and other pins are V _{SS} .	V _{CC} = 5 V, f(X _{IN}) = 12 MHz (square waveform), f(f ₂) = 6 MHz, f(X _{CIN}) = 32.768 kHz, in operating (Note 1)		4.5	9	mA
			V _{CC} = 3 V, f(X _{IN}) = 12 MHz (square waveform), f(f ₂) = 6 MHz, f(X _{CIN}) = 32.768 kHz, in operating (Note 1)		3	6	mA
			V _{CC} = 3 V, f(X _{IN}) = 12 MHz (square waveform), f(f ₂) = 0.75 MHz, f(X _{CIN}) : Stopped, in operating		0.4	0.8	mA
			V _{CC} = 3 V, f(X _{IN}) = 12 MHz (square waveform), f(X _{CIN}) = 32.768 kHz, when a WIT instruction is executed (Note 2)		6	12	μ A
			V _{CC} = 3 V, f(X _{IN}) : Stopped, f(X _{CIN}) = 32.768 kHz, in operating (Note 3)		30	60	μ A
			V _{CC} = 3 V, f(X _{IN}) : Stopped, f(X _{CIN}) = 32.768 kHz, when a WIT instruction is executed (Note 4)		3	6	μ A
			T _a = 25 °C, when clock is stopped			1	μ A
			T _a = 85 °C, when clock is stopped			20	μ A

- Notes**
1. This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".
 2. This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".
 3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
 4. This applies when the X_{cout} drivability selection bit = "0" and the system clock stop bit at wait state = "1".

A-D CONVERTER CHARACTERISTICS

($V_{CC} = AV_{CC} = 5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ to }+85\text{ }^\circ\text{C}$, $f(X_{IN}) = 12\text{ MHz}$, unless otherwise noted (Note))

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V _{REF} = V _{CC}			10	Bits
—	Absolute accuracy	V _{REF} = V _{CC}			± 3	LSB
RLADDER	Ladder resistance	V _{REF} = V _{CC}	10		25	kΩ
t _{CONV}	Conversion time		19.6			μ s
V _{REF}	Reference voltage		2.7		V _{CC}	V
V _{IA}	Analog input voltage		0		V _{REF}	V

Note. This applies when the main clock division selection bit = "0" and f(f₂) = 6 MHz.

TIMING REQUIREMENTS ($V_{CC} = 2.7 - 5.5$ V, $V_{SS} = 0$ V, $T_a = -40$ to $+85$ °C, $f(X_{IN}) = 12$ MHz, unless otherwise noted (Note 1))

- Notes 1.** This applies when the main clock division selection bit = "0" and $f(f_2) = 6$ MHz.
2. Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time (Note 3)	83		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 4)	33		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 4)	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Notes 3. When the main clock division selection bit = "1", the minimum value of $t_c = 166$ ns.

4. When the main clock division selection bit = "1", values of $t_{w(H)} / t_c$ and $t_{w(L)} / t_c$ must be set to values from 0.45 through 0.55.

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su}(P0D-E)$	Port P0 input setup time	200		ns
$t_{su}(P1D-E)$	Port P1 input setup time	200		ns
$t_{su}(P2D-E)$	Port P2 input setup time	200		ns
$t_{su}(P3D-E)$	Port P3 input setup time	200		ns
$t_{su}(P4D-E)$	Port P4 input setup time	200		ns
$t_{su}(P5D-E)$	Port P5 input setup time	200		ns
$t_{su}(P6D-E)$	Port P6 input setup time	200		ns
$t_{su}(P7D-E)$	Port P7 input setup time	200		ns
$t_{su}(P8D-E)$	Port P8 input setup time	200		ns
$t_{su}(P10D-E)$	Port P10 input setup time	200		ns
$t_{h}(E-P0D)$	Port P0 input hold time	0		ns
$t_{h}(E-P1D)$	Port P1 input hold time	0		ns
$t_{h}(E-P2D)$	Port P2 input hold time	0		ns
$t_{h}(E-P3D)$	Port P3 input hold time	0		ns
$t_{h}(E-P4D)$	Port P4 input hold time	0		ns
$t_{h}(E-P5D)$	Port P5 input hold time	0		ns
$t_{h}(E-P6D)$	Port P6 input hold time	0		ns
$t_{h}(E-P7D)$	Port P7 input hold time	0		ns
$t_{h}(E-P8D)$	Port P8 input hold time	0		ns
$t_{h}(E-P10D)$	Port P10 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su}(D-E)$	Data input setup time (external bus mode A)	50		ns
$t_{su}(D-RDE)$	Data input setup time (external bus mode B)	50		ns
$t_{su}(RDY-\phi 1)$	RDY input setup time	80		ns
$t_{su}(HOLD-\phi 1)$	HOLD input setup time	80		ns
$t_{h}(E-D)$	Data input hold time (external bus mode A)	0		ns
$t_{h}(RDE-D)$	Data input hold time (external bus mode B)	0		ns
$t_{h}(\phi 1-RDY)$	RDY input hold time	0		ns
$t_{h}(\phi 1-HOLD)$	HOLD input hold time	0		ns

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	250		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width	125		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	125		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time (Note)	666		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width (Note)	333		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time (Note)	666		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width	166		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	166		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high-level pulse width	166		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	166		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	3333		ns
$t_{w(UPH)}$	TAiOUT input high-level pulse width	1666		ns
$t_{w(UPL)}$	TAiOUT input low-level pulse width	1666		ns
$t_{su(UP-T_{IN})}$	TAiOUT input setup time	666		ns
$t_{h(T_{IN}-UP)}$	TAiOUT input hold time	666		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAjIN input cycle time	2000		ns
$t_{su(TAjIN-TAjOUT)}$	TAjIN input setup time	500		ns
$t_{su(TAjOUT-TAjIN)}$	TAjOUT input setup time	500		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(TB)$	TBiIN input cycle time (one edge count)	250		ns
$t_w(TBH)$	TBiIN input high-level pulse width (one edge count)	125		ns
$t_w(TBL)$	TBiIN input low-level pulse width (one edge count)	125		ns
$t_c(TB)$	TBiIN input cycle time (both edges count)	500		ns
$t_w(TBH)$	TBiIN input high-level pulse width (both edges count)	250		ns
$t_w(TBL)$	TBiIN input low-level pulse width (both edges count)	250		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(TB)$	TBiIN input cycle time (Note)	666		ns
$t_w(TBH)$	TBiIN input high-level pulse width (Note)	333		ns
$t_w(TBL)$	TBiIN input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(TB)$	TBiIN input cycle time (Note)	666		ns
$t_w(TBH)$	TBiIN input high-level pulse width (Note)	333		ns
$t_w(TBL)$	TBiIN input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(AD)$	ADTRG input cycle time (minimum allowable trigger)	1333		ns
$t_w(ADL)$	ADTRG input low-level pulse width	166		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(CK)$	CLKi input cycle time	333		ns
$t_w(CKH)$	CLKi input high-level pulse width	166		ns
$t_w(CKL)$	CLKi input low-level pulse width	166		ns
$t_d(C-Q)$	TxDi output delay time		100	ns
$t_h(C-Q)$	TxDi hold time	0		ns
$t_{su}(D-C)$	RxDi input setup time	65		ns
$t_h(C-D)$	RxDi input hold time	75		ns

External interrupt \overline{INT}_i input, key input interrupt \overline{KI}_i input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_w(INH)$	\overline{INT}_i input high-level pulse width	250		ns
$t_w(INL)$	\overline{INT}_i input low-level pulse width	250		ns
$t_w(KIL)$	\overline{KI}_i input low-level pulse width	250		ns

DATA FORMULAS

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_w(TAH)$	TAiIn input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_w(TAL)$	TAiIn input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_w(TBH)$	TBiIn input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_w(TBL)$	TBiIn input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37736MHBXXXGP".

SWITCHING CHARACTERISTICS

(VCC = 2.7 – 5.5 V, VSS = 0 V, Ta = –40 to +85°C, f(XIN) = 12 MHz, unless otherwise noted (Note))

Single-chip mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
td(E–P0Q)	Port P0 data output delay time	Fig. 2		300	ns
td(E–P1Q)	Port P1 data output delay time			300	ns
td(E–P2Q)	Port P2 data output delay time			300	ns
td(E–P3Q)	Port P3 data output delay time			300	ns
td(E–P4Q)	Port P4 data output delay time			300	ns
td(E–P5Q)	Port P5 data output delay time			300	ns
td(E–P6Q)	Port P6 data output delay time			300	ns
td(E–P7Q)	Port P7 data output delay time			300	ns
td(E–P8Q)	Port P8 data output delay time			300	ns
td(E–P9Q)	Port P9 data output delay time			300	ns
td(E–P10Q)	Port P10 data output delay time			300	ns

Note. This applies when the main clock division selection bit = "0" and f(t2) = 6 MHz.

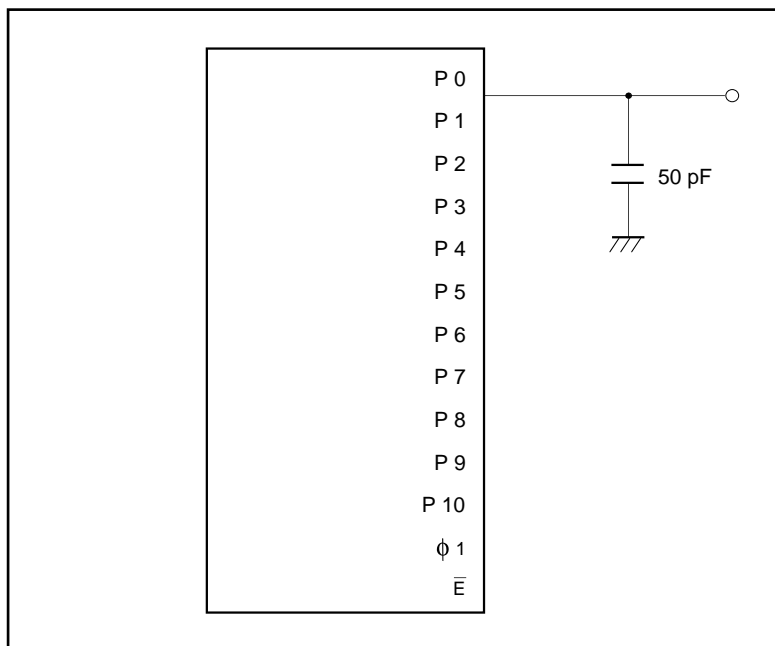


Fig. 2 Measuring circuit for ports P0 – P10 and ϕ 1

**[External bus mode A]
 Memory expansion mode and microprocessor mode**

(V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, T_a = –40 to +85°C, f(XIN) = 12 MHz (Note 1), unless otherwise noted)

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits		Unit	
				Min.	Max.		
t _d (A _n –E)	Address output delay time	No wait	Fig. 2	20		ns	
		Wait 1					
		Wait 0		182		ns	
t _d (A–E)	Address output delay time	No wait		20		ns	
		Wait 1					
		Wait 0		162		ns	
t _h (E–A _n)	Address hold time				40		ns
t _w (ALE)	ALE pulse width	No wait			40		ns
		Wait 1					
		Wait 0			123		ns
t _{su} (A–ALE)	Address output setup time	No wait			10		ns
		Wait 1					
		Wait 0			93		ns
t _h (ALE–A)	Address hold time	No wait			9		ns
		Wait 1					
		Wait 0			40		ns
t _d (ALE–E)	ALE output delay time	No wait			4		ns
		Wait 1					
		Wait 0		40		ns	
t _d (E–DQ)	Data output delay time				90	ns	
t _h (E–DQ)	Data hold time			40		ns	
t _w (EL)	E pulse width	No wait		131		ns	
		Wait 1					
		Wait 0		298		ns	
t _{pxz} (E–DZ)	Floating start delay time				10	ns	
t _{pzx} (E–DZ)	Floating release delay time			53		ns	
t _d (BHE–E)	BHE output delay time	No wait		20		ns	
		Wait 1					
		Wait 0		182		ns	
t _d (R/W–E)	R/W output delay time	No wait		20		ns	
		Wait 1					
		Wait 0		182		ns	
t _h (E–BHE)	BHE hold time			33		ns	
t _h (E–R/W)	R/W hold time			33		ns	
t _d (E–φ 1)	φ 1 output delay time			0	30	ns	
t _d (φ 1–HLDA)	HLDA output delay time				120	ns	

Notes 1. This applies when the main clock division selection bit = "0" and f(f2) = 6 MHz.

2. No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

**[External bus mode A]
 Memory expansion mode and microprocessor mode**

Bus timing data formulas ($V_{CC} = 2.7 - 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = -40 \text{ to } +85 \text{ }^\circ\text{C}$, $f(XIN) = 12 \text{ MHz}$ (Max., Note), unless otherwise noted)

Symbol	Parameter	Wait mode	Limits		Unit
			Min.	Max.	
td(An-E)	Address output delay time	No wait	1×10^9	- 63	ns
		Wait 1	$\frac{2 \cdot f(f_2)}{2}$		
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 68	ns
td(A-E)	Address output delay time	No wait	1×10^9	- 63	ns
		Wait 1	$\frac{2 \cdot f(f_2)}{2}$		
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 88	ns
th(E-An)	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
tw(ALE)	ALE pulse width	No wait	1×10^9	- 43	ns
		Wait 1	$\frac{2 \cdot f(f_2)}{2}$		
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
tsu(A-ALE)	Address output setup time	No wait	1×10^9	- 73	ns
		Wait 1	$\frac{2 \cdot f(f_2)}{2}$		
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 73	ns
th(ALE-A)	Address hold time	No wait	9		ns
		Wait 1			ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
td(ALE-E)	ALE output delay time	No wait	4		ns
		Wait 1			ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
td(E-DQ)	Data output delay time			90	ns
th(E-DQ)	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
tw(EL)	\bar{E} pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 35	ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$	- 35	ns
		Wait 0	$\frac{2 \cdot f(f_2)}{2}$		ns
tpxz(E-DZ)	Floating start delay time			10	ns
tpzx(E-DZ)	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 30	ns
td(BHE-E)	\bar{BHE} output delay time	No wait	1×10^9	- 63	ns
		Wait 1	$\frac{2 \cdot f(f_2)}{2}$		
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 68	ns
td(R/W-E)	$\bar{R/W}$ output delay time	No wait	1×10^9	- 63	ns
		Wait 1	$\frac{2 \cdot f(f_2)}{2}$		
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 68	ns
th(E-BHE)	\bar{BHE} hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 50	ns
th(E-R/W)	$\bar{R/W}$ hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 50	ns
td(E- ϕ 1)	ϕ 1 output delay time		0	30	ns

Notes 1. This applies when the main-clock division selection bit = "0".

2. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37736MHBXXXGP".

**[External bus mode B]
 Memory expansion mode and microprocessor mode**

(V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, T_a = –40 to +85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted (Note 1))

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits		Unit	
				Min.	Max.		
td(CS–WE) td(CS–RDE)	Chip-select output delay time	No wait	Fig. 2	20		ns	
		Wait 1		182		ns	
		Wait 0		4		ns	
th(WE–CS) th(RDE–CS)	Chip-select hold time						
td(A _n –WE) td(A _n –RDE)	Address output delay time	No wait			20		ns
		Wait 1			182		ns
		Wait 0			162		ns
td(A–WE) td(A–RDE)	Address output delay time	No wait			20		ns
		Wait 1			162		ns
		Wait 0			40		ns
th(WE–A _n) th(RDE–A _n)	Address hold time			40		ns	
tw(ALE)	ALE pulse width	No wait		40		ns	
		Wait 1		123		ns	
		Wait 0		10		ns	
tsu(A–ALE)	Address output setup time	No wait		10		ns	
		Wait 1		93		ns	
		Wait 0		9		ns	
th(ALE–A)	Address hold time	No wait		9		ns	
		Wait 1		40		ns	
		Wait 0		4		ns	
td(ALE–WE) td(ALE–RDE)	ALE output delay time	No wait		4		ns	
		Wait 1		40		ns	
		Wait 0		40	90	ns	
td(WE–DQ)	Data output delay time					ns	
th(WE–DQ)	Data hold time			40		ns	
tw(WE)	WE pulse width	No wait		131		ns	
		Wait 1		298		ns	
		Wait 0			10	ns	
tpxz(RDE–DZ)	Floating start delay time					ns	
tpzx(RDE–DZ)	Floating release delay time			53		ns	
tw(RDE)	RDE pulse width	No wait		128		ns	
		Wait 1		295		ns	
		Wait 0		25		ns	
td(RSMP–WE) td(RSMP–RDE)	RSMP output delay time			0		ns	
th(φ ₁ –RSMP)	RSMP hold time			0		ns	
td(WE–φ ₁) td(RDE–φ ₁)	φ ₁ output delay time			0	30	ns	
td(φ ₁ –HLDA)	HLDA output delay time				120	ns	

Notes 1. This applies when the main clock division selection bit = “0” and f(f₂) = 6 MHz.

2. No wait : Wait bit = “1”.

Wait 1 : The external memory area is accessed with wait bit = “0” and wait selection bit = “1”.

Wait 0 : The external memory area is accessed with wait bit = “0” and wait selection bit = “0”.

[External bus mode B]

Bus timing data formulas ($V_{CC} = 2.7 - 5.5V$, $V_{SS} = 0V$, $T_a = -40$ to $+85^\circ C$, $f(XIN) = 12$ MHz (Max.), unless otherwise noted (Note1))

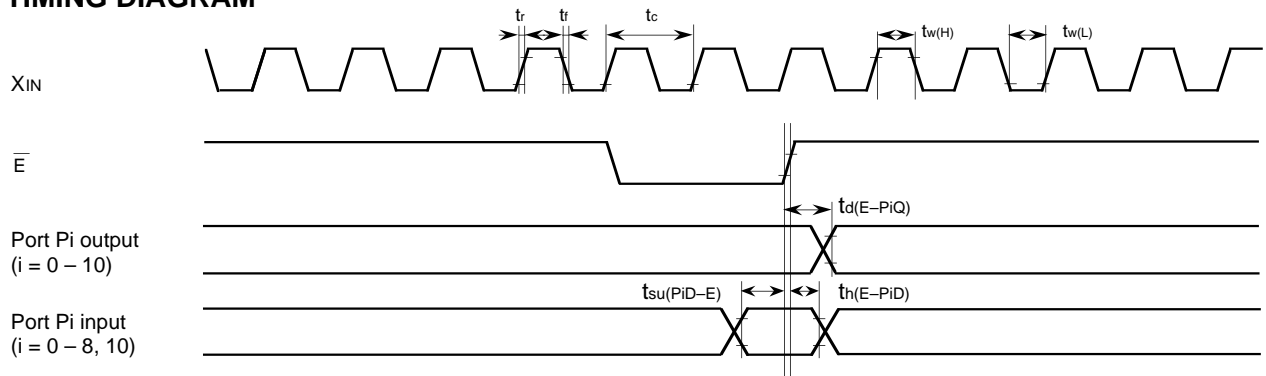
Symbol	Parameter	Wait mode	Limits		Unit
			Min.	Max.	
td(CS-WE) td(CS-RDE)	Chip-select output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 63	ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 68	
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 68	ns
th(WE-CS) th(RDE-CS)	Chip-select hold time		4		ns
td(An-WE) td(An-RDE)	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 63	ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 68	
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 68	ns
td(A-WE) td(A-RDE)	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 63	ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 88	
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 88	ns
th(WE-An) th(RDE-An)	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
tw(ALE)	ALE pulse width	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
		Wait 1	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 43	
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
tsu(A-ALE)	Address output setup time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 73	ns
		Wait 1	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 73	
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 73	ns
th(ALE-A)	Address hold time	No wait	9		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
td(ALE-WE) td(ALE-RDE)	ALE output delay time	No wait	4		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
td(WE-DQ)	Data output delay time			90	ns
th(WE-DQ)	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 43	ns
tw(WE)	WEL/WEH pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 35	ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$	- 35	
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 35	ns
tpxz(RDE-DZ)	Floating start delay time			10	ns
tpxz(RDE-DZ)	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 30	ns
tw(RDE)	RDE pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 38	ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$	- 38	
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 38	ns
td(RSMP-WE) td(RSMP-RDE)	RSMP output delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 58	ns
th(ϕ_1 -RSMP)	RSMP hold time		0		ns
td(WE- ϕ_1) td(RDE- ϕ_1)	ϕ_1 output delay time		0	30	ns

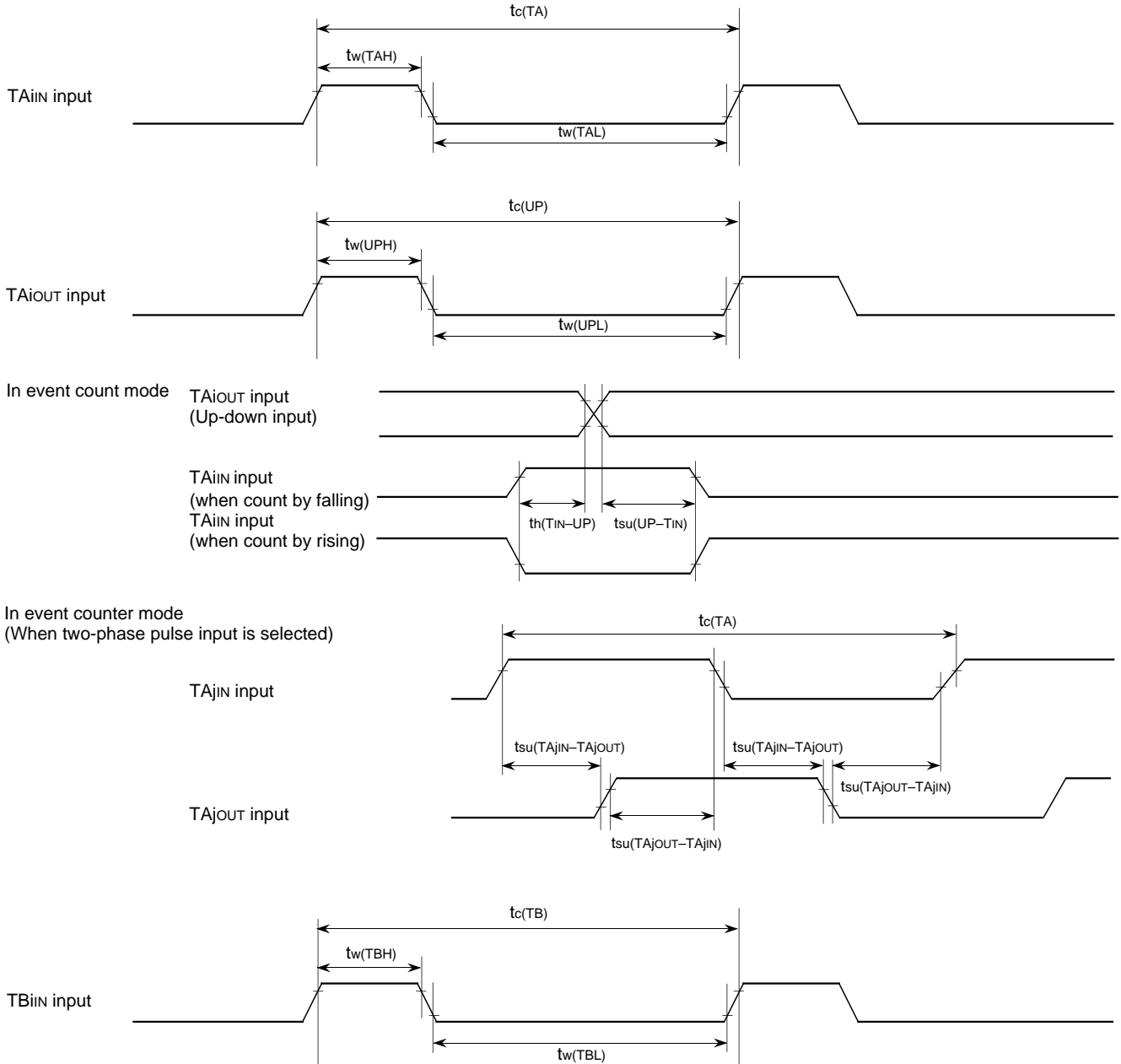
Notes 1. This applies when the main clock division selection bit = "0".

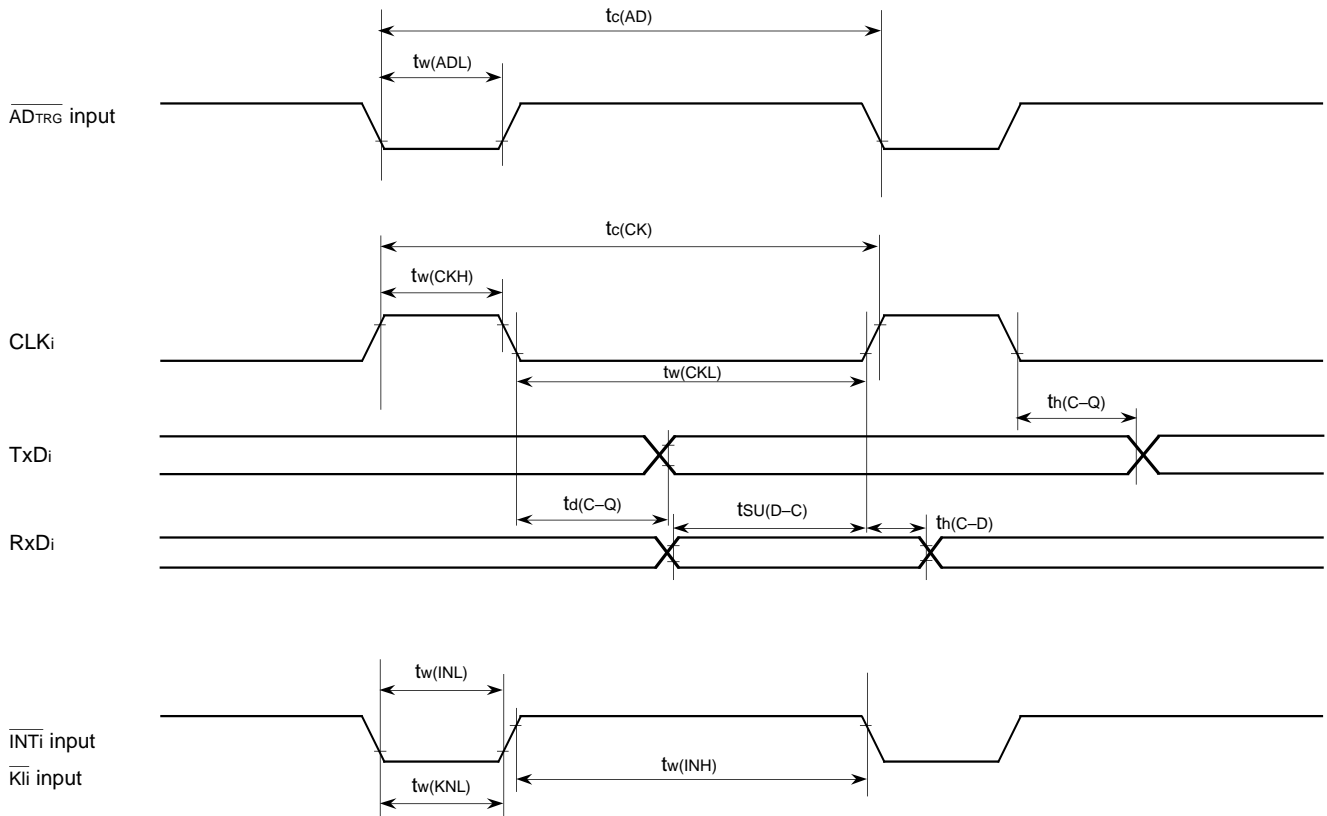
2. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37736MHBXXXGP".

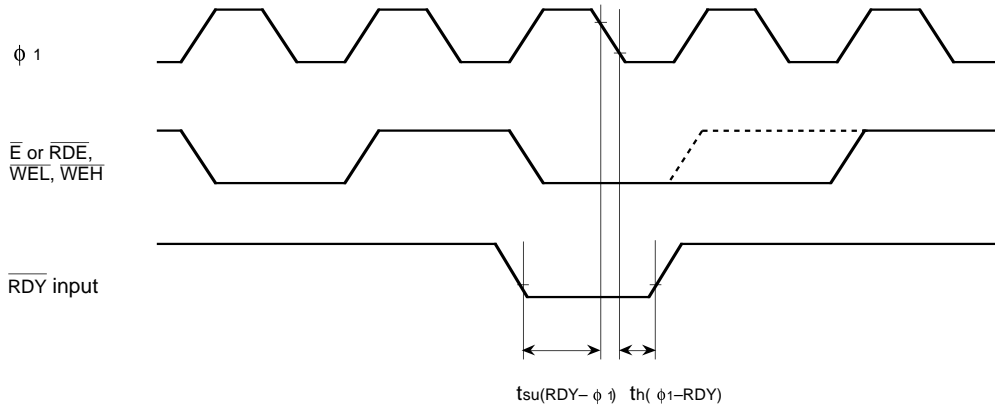
TIMING DIAGRAM



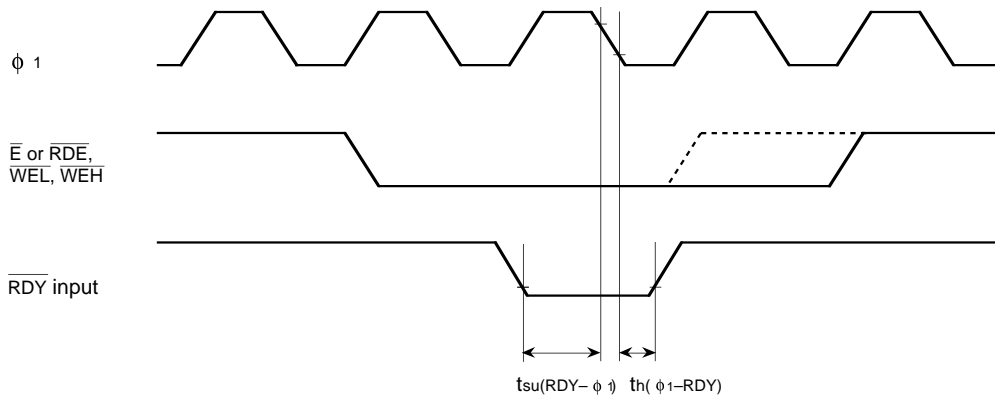




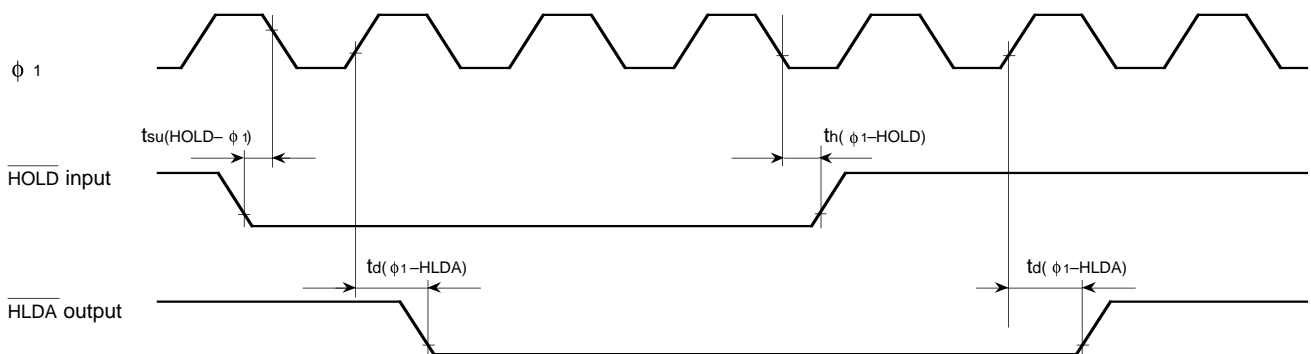
Memory expansion mode and microprocessor mode
 (When wait bit = "1")



(When wait bit = "0")



(When wait bit = "1" or "0" in common)

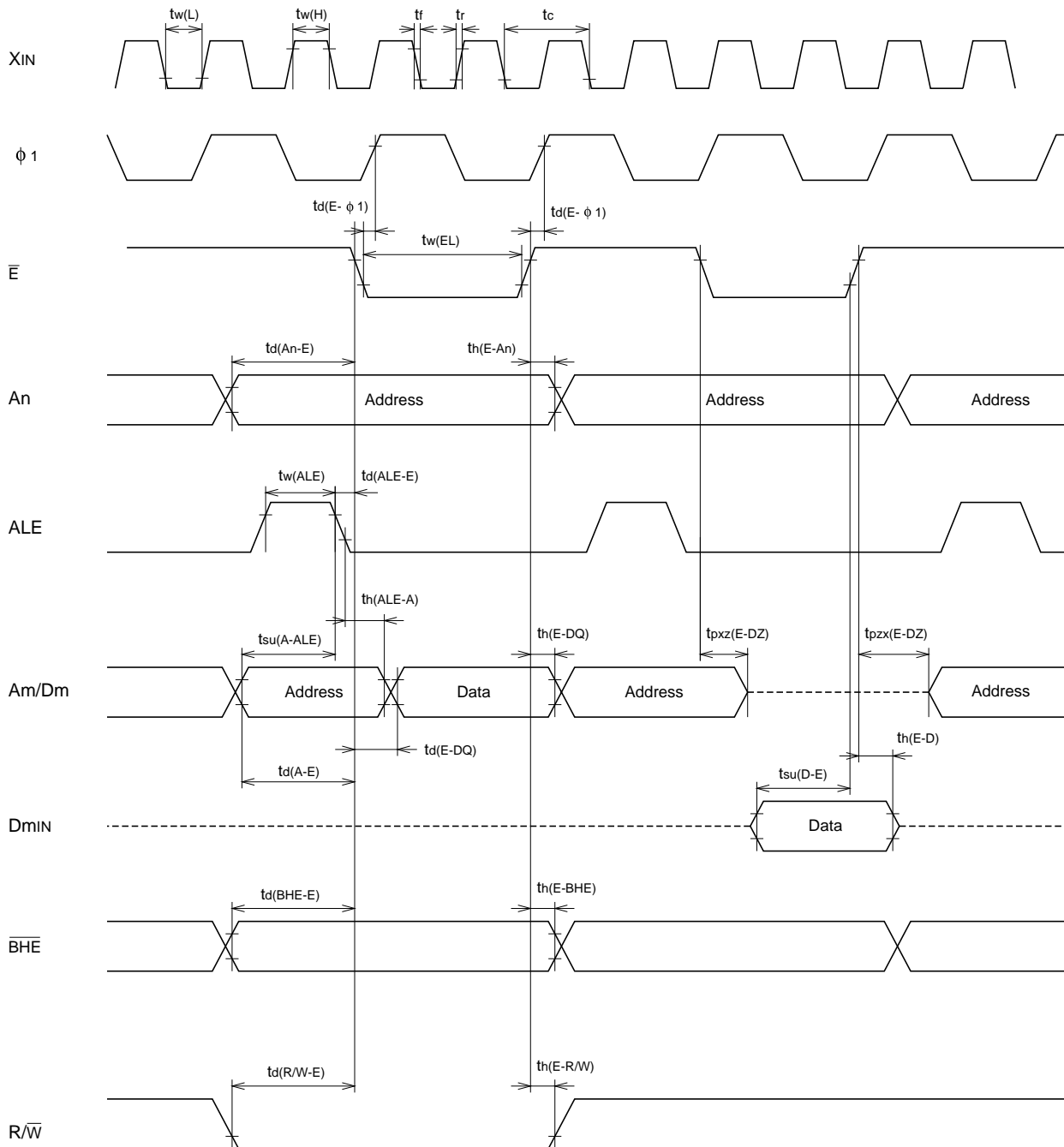


Test conditions

- $V_{CC} = 2.7 - 5.5 V$
- Input timing voltage : $V_{IL} = 0.2 V_{CC}$, $V_{IH} = 0.8 V_{CC}$
- Output timing voltage : $V_{OL} = 0.8 V$, $V_{OH} = 2.0 V$

[External bus mode A]

Memory expansion mode and microprocessor mode
(No wait : When wait bit = "1")



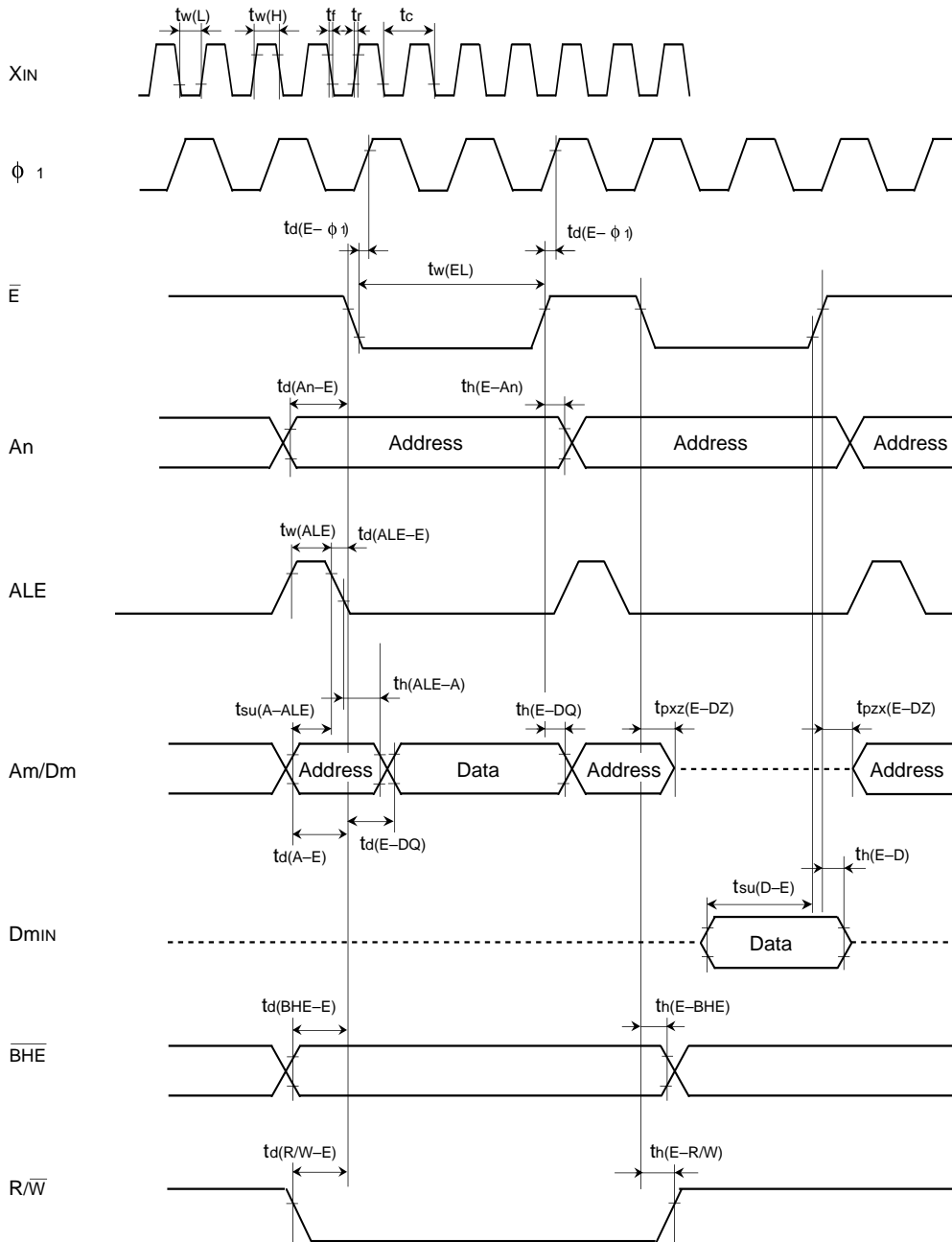
Test conditions

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage : $V_{OL} = 0.8 V, V_{OH} = 2.0 V$
- Data input D_{min} : $V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}$

[External bus mode A]

Memory expansion mode and microprocessor mode

(Wait 1 : The external area is accessed when wait bit = "0" and wait selection bit = "1".)



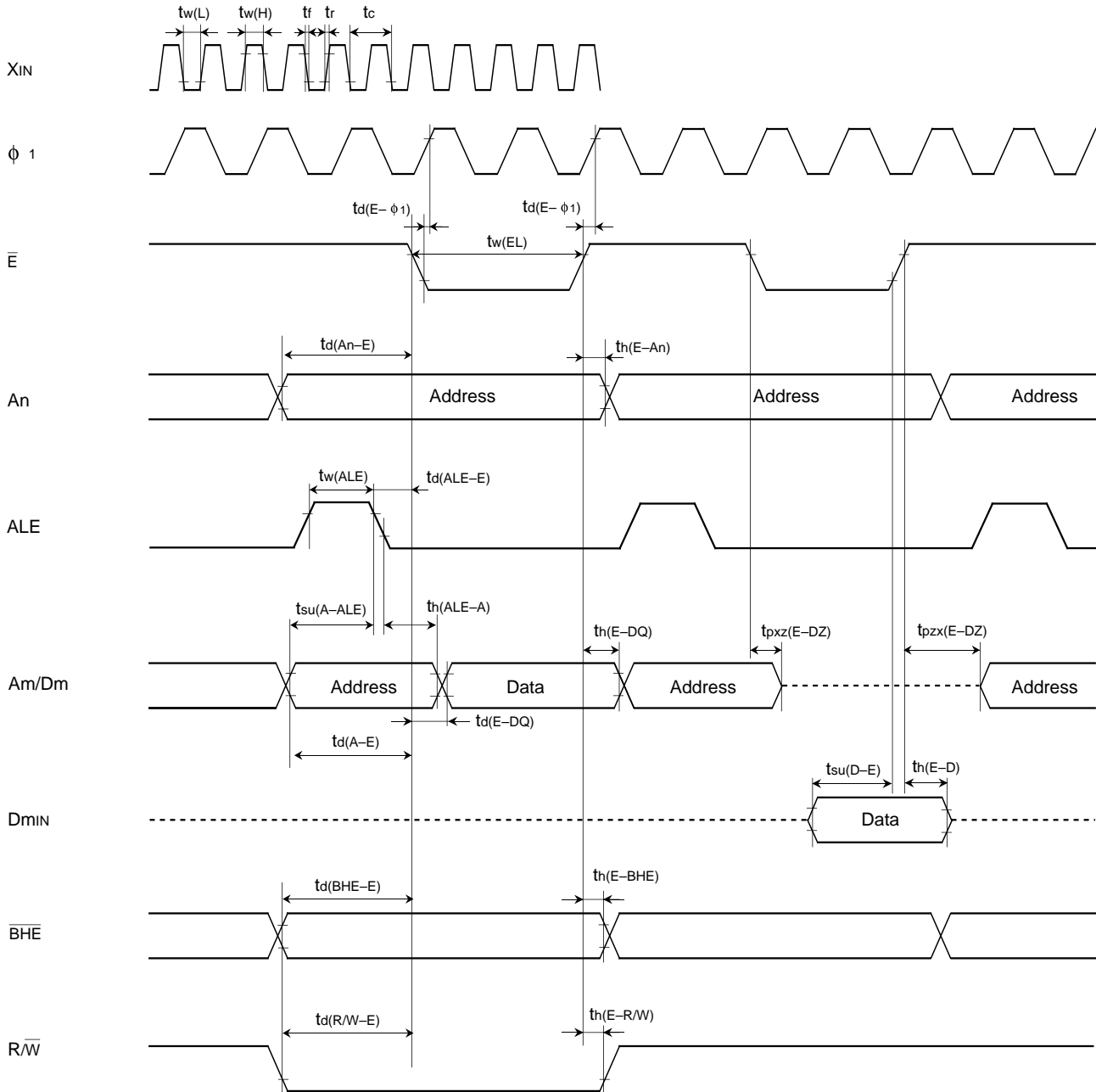
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[External bus mode A]

Memory expansion mode and microprocessor mode

(Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "0".)

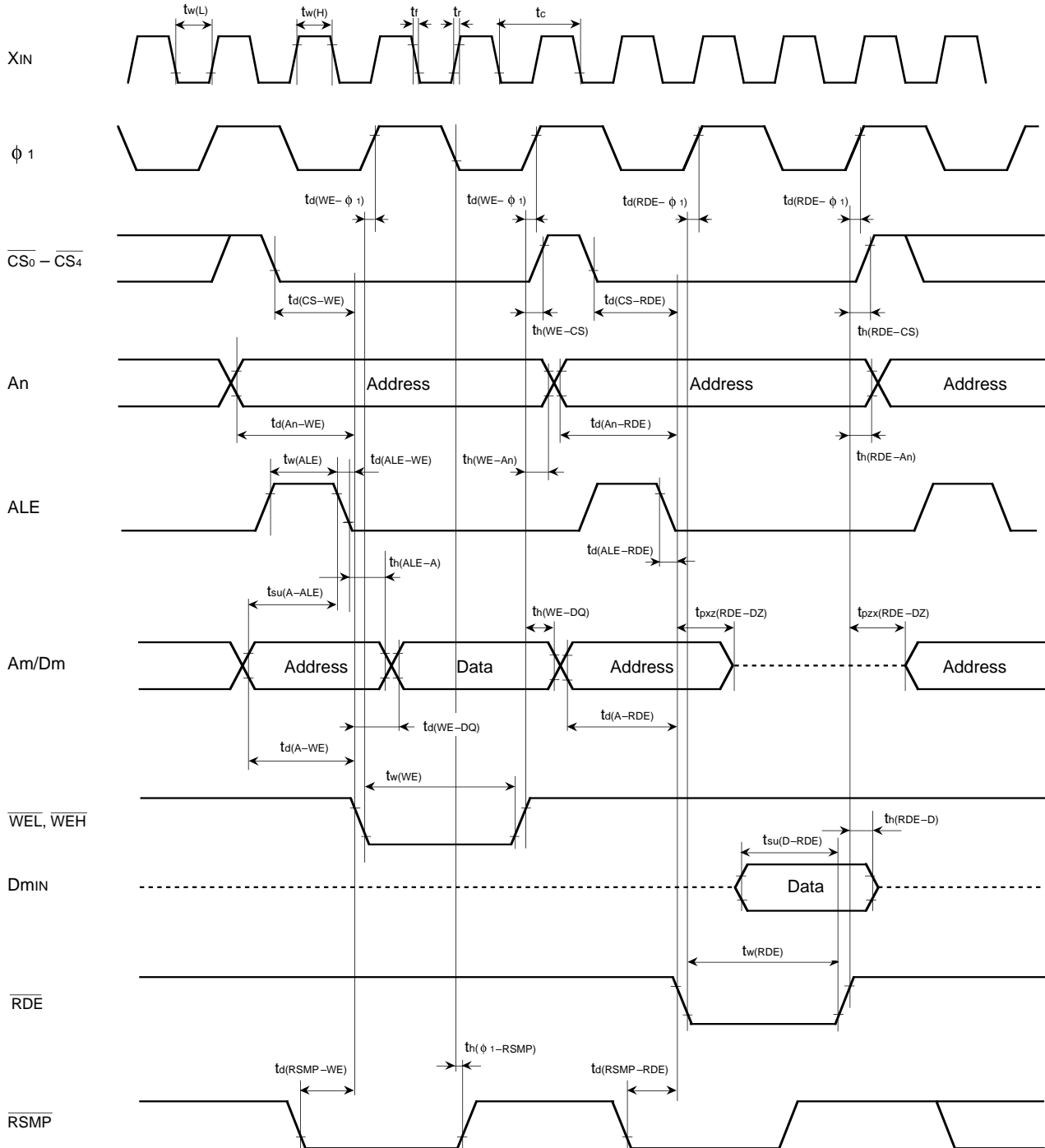


Test conditions

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage : $V_{OL} = 0.8 V$, $V_{OH} = 2.0 V$
- Data input D_{MIN} : $V_{IL} = 0.16 V_{CC}$, $V_{IH} = 0.5 V_{CC}$

[External bus mode B]

Memory expansion and microprocessor mode
 (No wait : When wait bit = "1")

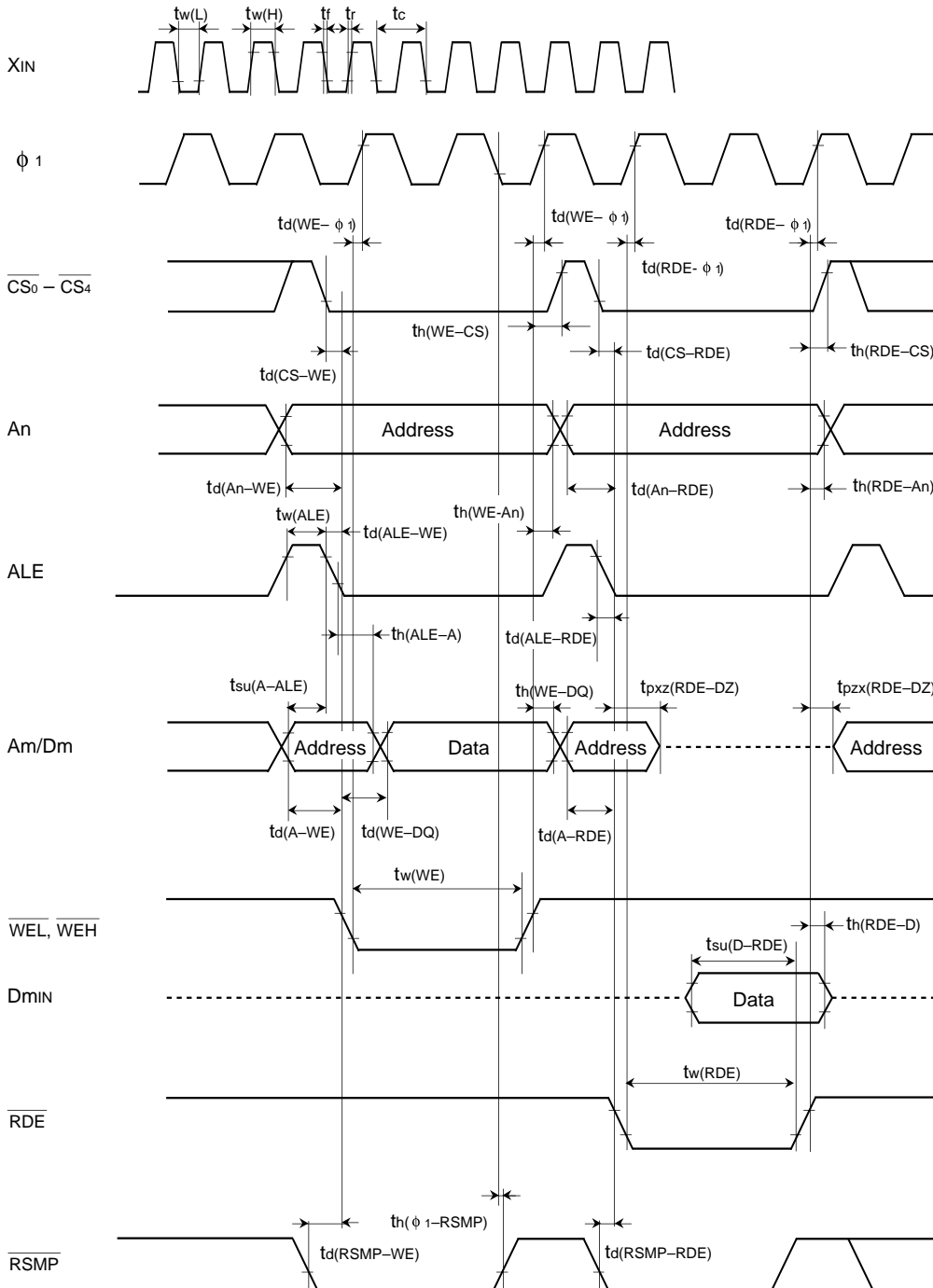


Test conditions
 • $V_{CC} = 2.7 - 5.5 V$
 • Output timing voltage : $V_{OL} = 0.8 V, V_{OH} = 2.0 V$
 • Data input D_{MIN} : $V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}$

[External bus mode B]

Memory expansion and microprocessor mode

(Wait 1 : The external area is accessed when wait bit = "0" and wait selection bit = "1".)



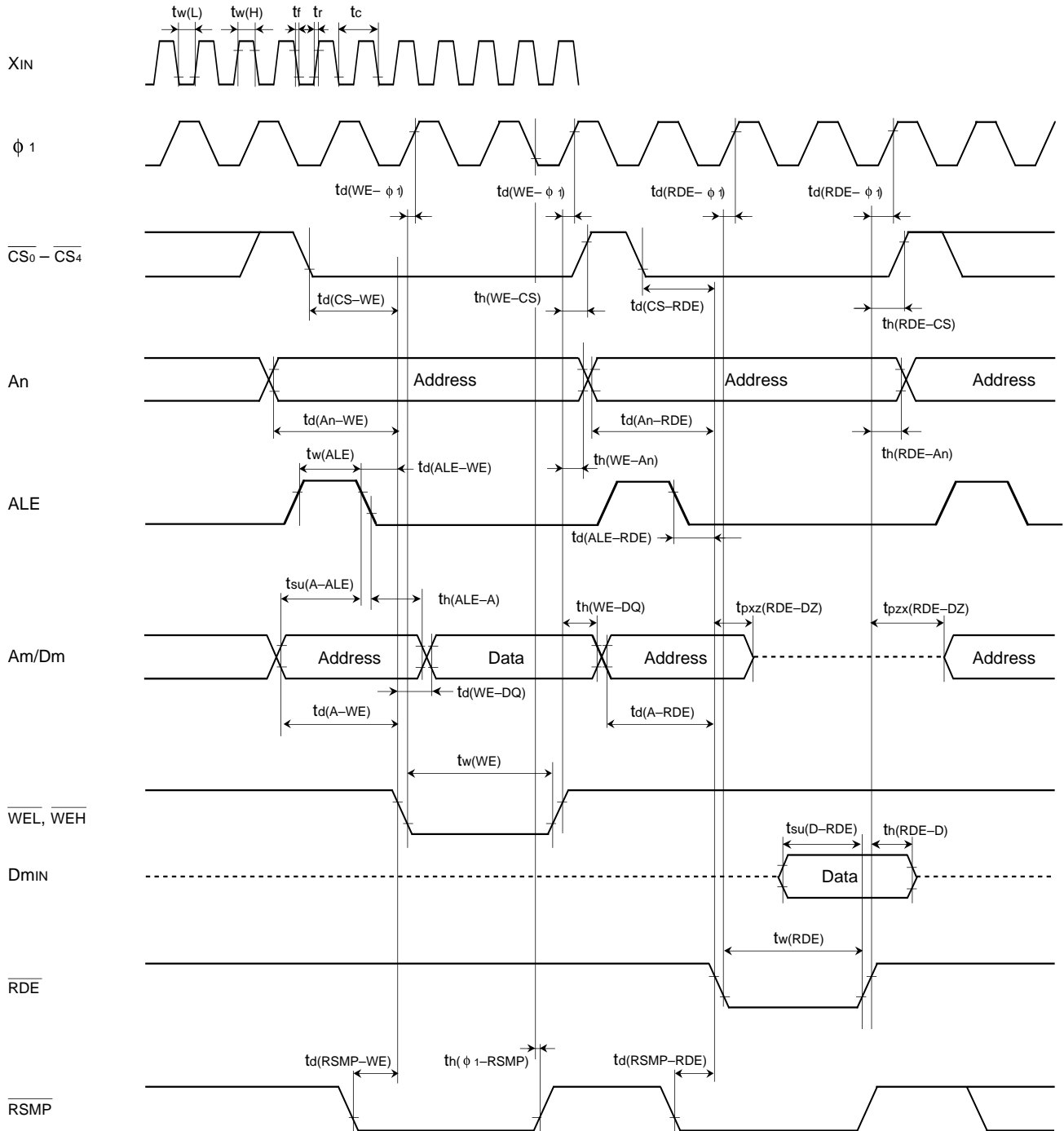
Test conditions

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage : $V_{OL} = 0.8 V, V_{OH} = 2.0 V$
- Data input D_{min} : $V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}$

[External bus mode B]

Memory expansion and microprocessor mode

(Wait 0 : The external memory is accessed when wait bit = "0" and wait selection bit = "0".)



Test conditions

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage : $V_{OL} = 0.8 V$, $V_{OH} = 2.0 V$
- Data input D_{min} : $V_{IL} = 0.16 V_{CC}$, $V_{IH} = 0.5 V_{CC}$

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS
M37736MHLXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

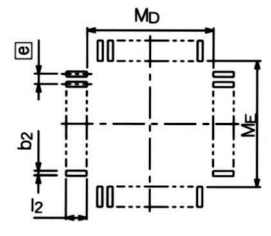
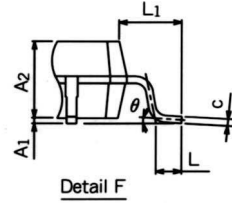
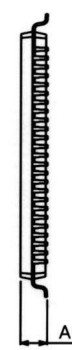
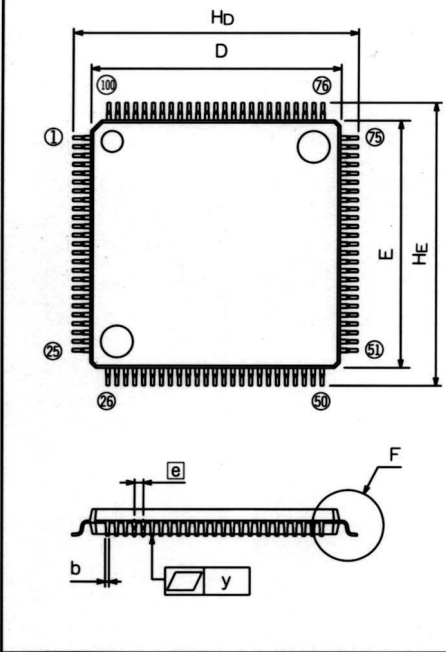
PACKAGE OUTLINE

100P6Q-A

Plastic 100pin 14 X 14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight (g)	Lead Material
LQFP100-P-1414-0.50	-	-	Cu Alloy

Under Development



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	-	0.5	-
Hd	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	-	1.0	-
y	-	-	0.1
theta	0°	-	10°
b2	-	0.225	-
l2	1.0	-	-
MD	-	14.4	-
ME	-	14.4	-

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REVISION DESCRIPTION LIST

M37736MHLXXXHP Datasheet

Rev. No.	Revision Description		Rev. date																																		
1.00	First Edition		970507																																		
2.00	The following are revised:		980731																																		
	Page	Previous Version	Revised Version																																		
	P4 P10 ₀ – P10 ₇	<table border="1"> <tr> <td>P10₀ – P10₇</td> <td>Output port P10</td> <td>I/O</td> </tr> <tr> <td>EVL0, EVL1</td> <td>—</td> <td>Output</td> </tr> </table>	P10 ₀ – P10 ₇	Output port P10	I/O	EVL0, EVL1	—	Output	<table border="1"> <tr> <td>P10₀ – P10₇</td> <td>I/O port P10</td> <td>I/O</td> </tr> <tr> <td>EVL0, EVL1</td> <td>—</td> <td>Output</td> </tr> </table>	P10 ₀ – P10 ₇	I/O port P10	I/O	EVL0, EVL1	—	Output																						
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