

M62055FP

3V POWER SUPPLY with WATCHDOG TIMER

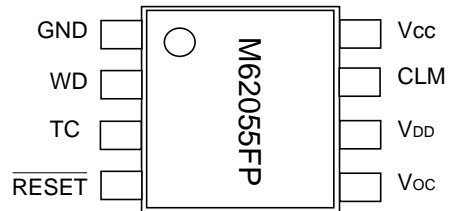
GENERAL DESCRIPTION

M62055FP is a 3V power supply featuring a watchdog timer function for a microcontroller system. It can be a power source of $3V \pm 5\%$ by utilizing the reference voltage and amplifier. It can also generate a reset pulse for the applied systems during power-on, moreover it includes the watchdog timer for a self diagnostics of the system, which can prevent system erroneous functions.

FEATURES

- Power-on reset
- Watchdock timer
- High accuracy voltage source of $3V \pm 5\%$ (max)
- Overcurrent protection circuit
- The voltage detection accuracy of $\pm 5\%$ (max)
- Output power (Vo) cutoff function at erroneous conditions
- Backward voltage protection circuits for inputs and outputs

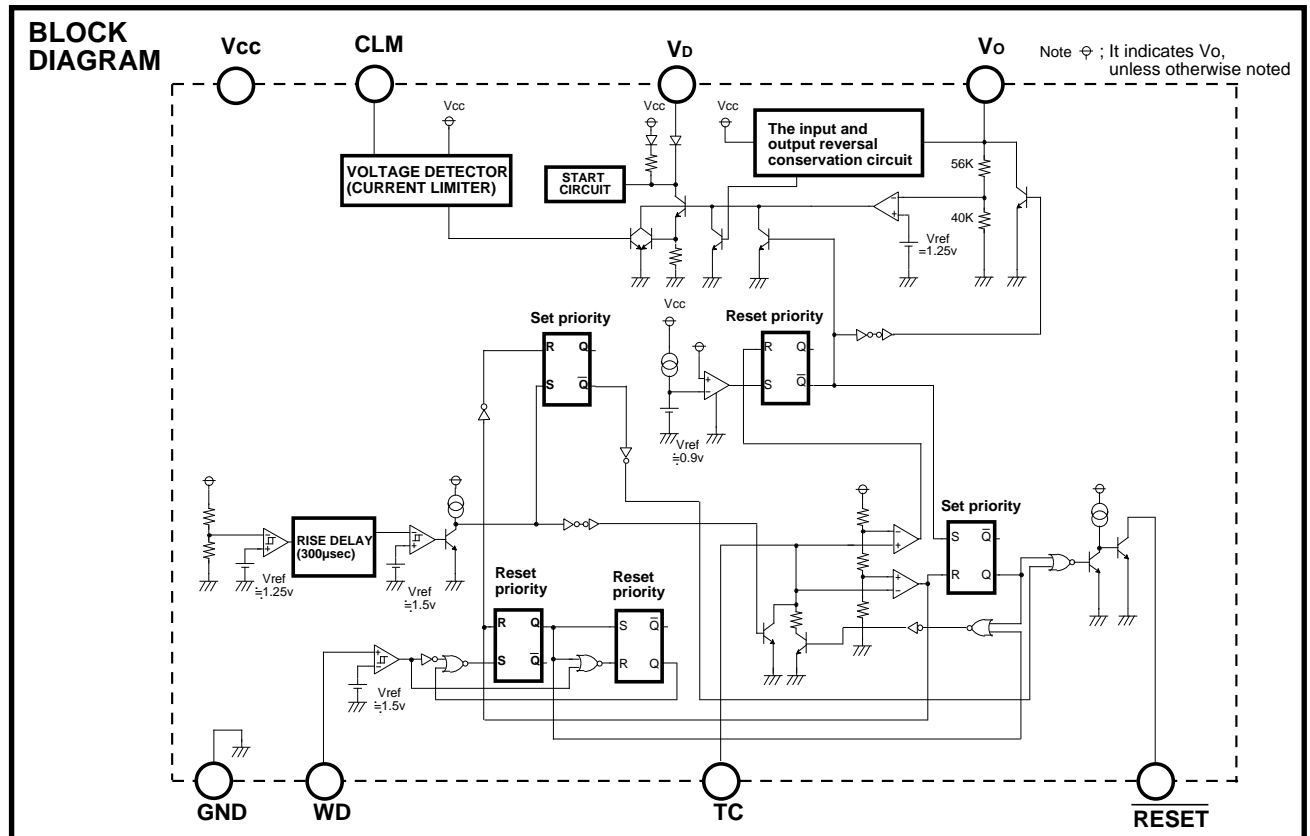
PIN CONFIGURATION(TOP VIEW)



Outline 8P2S

APPLICATION

Handy information terminal equipment, CD-ROM, Portable audio equipment.



Pin Functional description

pin number	symbol	Functional description
1	GND	Ground
2	WD	Input for watchdock timer.
3	TC	Setting up reset timer and watchdock timer.
4	$\overline{\text{RESET}}$	Reset signal output
5	VO	Feedback to a power supply for a MCU.
6	VD	Controlling the stability of an output voltage with a PNP transistor connected externally.
7	CLM	Current limiting
8	Vcc	Power supply voltage

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, Unless otherwise noted)

symbol	Parameter	conditions	Ratings	Unit
Vcc	supply voltage		13	V
VRM	Reset pin	Output voltage	10	V
IRM		Output current	10	mA
VWDM	Watchdock pin input voltage		3	V
K θ	Thermal derating	Ta 25°C	4.0	mW/°C
Topr	Operating temperature		- 20 ~ + 75	°C
Tstg	Storage temperature		- 55 ~ + 150	°C

ELECTRICAL CHARACTERISTICS (Vcc=5.0V, Ta=25°C, Unless otherwise noted)

(1) DC CHARACTERISTICS

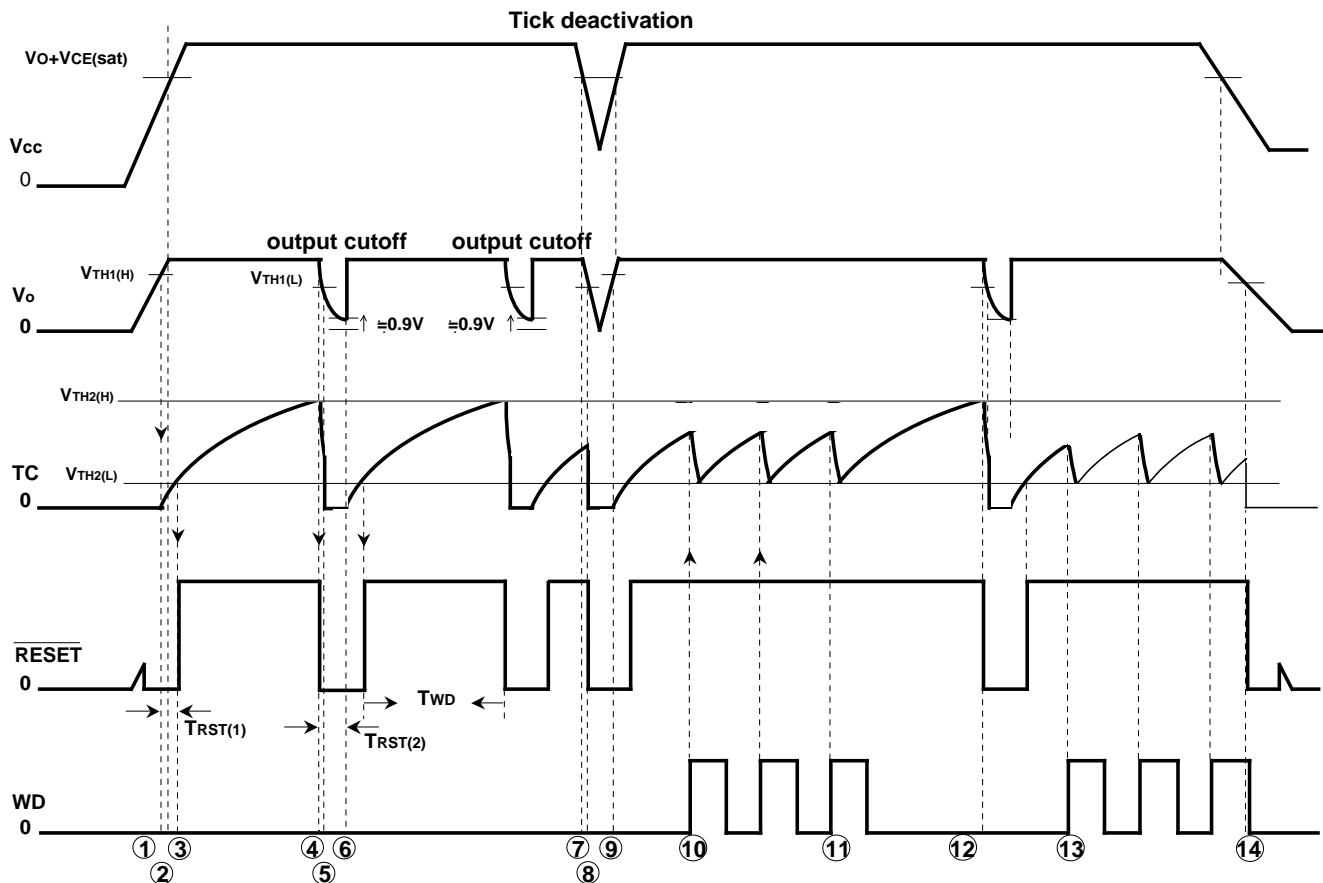
symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Battery* back up* regulator						
Vcc	supply voltage		3.5		13	V
Icc	Circuitry current			650	950	μA
Vo	Output voltage		2.85	3.0	3.15	V
IBmax	Bias current			10		mA
I BSC	Listing short-circuit bias current			1.5		mA
Reg-in	Input voltage regulation	Vcc=3.5V~13V		0.02	0.25	%/V
Reg-lo	Loading voltage regulation	Io=10mA~100mA		1	25	mV
Vo/ T	Output voltage thermal coefficient			0.02		%/T
VTHCLM	CLM threshold voltage		180	200	220	mV
Reset, watch dock timer						
VTH1(H)	Vo detection voltage		2.68	2.82	2.96	V
VTH1(L)			2.58	2.72	2.86	V
VTH1				0.1		V
VOL(RST)	Output voltage	Reset pin Isink=4mA		0.2	0.4	V
Ileak	Output leakage current				5	μA
VTH2(H)	Watchdock timer threshold voltage		2.28	2.4	2.52	V
VTH2(L)			0.95	1.0	1.05	V
IWD	WD input current	VIN=3V			1	μA
VTH(WD)	WD input threshold voltage			1.5		V
I _{tco}	TC output current	VIN=0.8V			1	μA
I _{tc1}	TC input current	VIN=2.4V		2.0		mA
I _{tc2}		In the output cutoff transmission mode	8.0			mA
VCCMIN	Vcc min operating voltage	*1			2.0	V

Note *1; The Vcc minimum operating voltage at which the RESET output is Low

(2) AC CHARACTERISTICS (Vcc=5.0V, Ta=25°C, Unless otherwise noted)

symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tWD	Watch dock timer	C=0.1μF, R1=10K	0.5	1.2	1.7	mS
tRST(1)	Reset timer (1)	C=0.1μF, R1=10K		0.7		mS
tRST(2)	Reset timer (2)	CO=10μF, R1=10K, IL=0	0.1		2.0	mS

FUNCTIONAL DESCRIPTION



- ① : When V_o rises to 0.5 V, \overline{RESET} becomes low. Then, charging to a capacitor C connected to TC will be started at the V_o of 2.82V($V_{TH1(H)}$).
- ② : When V_{CC} rises to $3V+V_{CE(sat)}$, V_o becomes stable.
- ③④ : When TC voltage rises to 1V($V_{TH2(L)}$), \overline{RESET} becomes high. When it rises to 2.4V ($V_{TH2(H)}$) further, the capacitor C is switched to discharge and \overline{RESET} becomes low.
- ⑤ : At the same time of a change-over to the discharge from the capacitor C, V_o is intercepted. Then, TC will be discharged completely at V_o of 2.72V($V_{TH1(L)}$).
- ⑥ : V_o returns to 3V right after it has fallen down to 0.9 V. \overline{RESET} repeats above operation till a normal clock signal is input to WD pin.

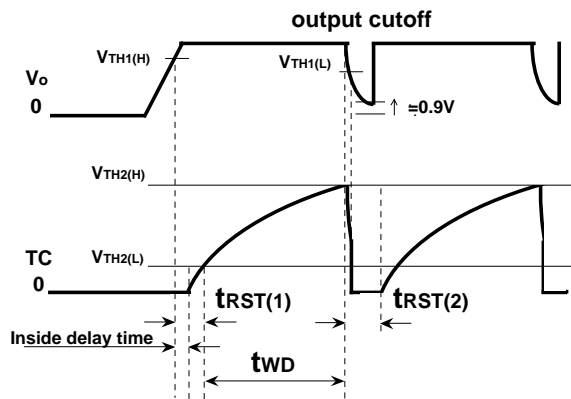
- ⑦⑧ : In the case of a sudden power interruption, V_o falls down according to a decrease of V_{CC} .
- ⑨ : When it falls down to 2.72V, the capacitor C is discharged and \overline{RESET} will be low. In the case of a reversion from the power interruption, V_o rises according to an increase of V_{CC} . When it rises to 2.82V, the charging to the capacitor C is started and \overline{RESET} will be high right after TC voltage reaches 1V.
- ⑩⑪ : In the case a clock signal for discharging the capacitor C is applied to pin WD before TC voltage reaches to 2.4V, a reset signal to \overline{RESET} is canceled.
- ⑫⑬ : In the case an abnormal clock signal is input, TC repeats charging / discharging alternately between 1 V and 2.4 V, so that \overline{RESET} also repeats high / low till a normal clock signal is input.
- ⑭ : When V_o falls down to 2.72 V, \overline{RESET} becomes Low.

DESCRIPTION of TERMS

- $t_{RST(1)}$ Time from when TC begins to charge until it reaches to $V_{TH2(L)}$.
- t_{WD} Time from when TC is $V_{TH2(L)}$ until it reaches to $V_{TH2(H)}$.
- $t_{RST(2)}$ Time from when TC is $V_{TH2(H)}$ until TC starts charging.

1. Pin ③ (TC pin) Charging and discharging time .

When an error is occurred in WD input, TC waveform is as shown below.

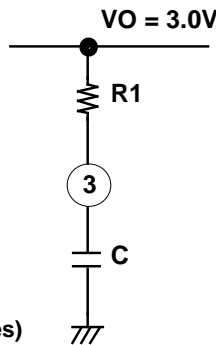


$$t_{RST(1)} = 0.406 \cdot C \cdot R_1 + 300\mu s \quad *1$$

$$t_{WD} = 1.2 \cdot C \cdot R_1$$

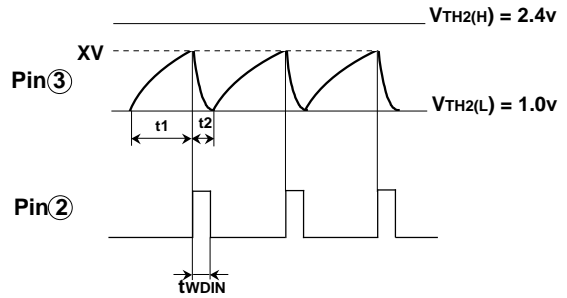
(Charging time)

*1 : Inside delay time (Typical values)



2. Pin ② (WD pin) Input frequency, input pulse width, charge/discharge time .

When input of ② WD is normal, TC waveform ③ is as shown below.



$$t_1 = C \cdot R_1 \cdot \ln \frac{2}{3-X}$$

$$t_2 = 1000 \cdot C \cdot R_1 \cdot \ln \frac{X \left(\frac{R_1}{1000} + 1 \right) - 3}{\frac{R_1}{1000} - 2}$$

Conditions of an input to pin ② (WD pin)

- (1) Input period should be t_{WD} or less.
(Pin discharge is completed before the arrival of $V_{TH2(H)} = 2.4 V$)

$$\frac{1}{1.2 \cdot C \cdot R_1} < f$$

- (2) Input pulse width t_{WDIN} should be t_2 or less.

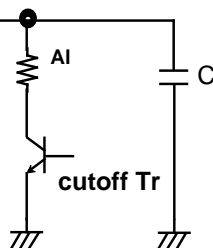
The following formula can be obtained because $t_{RST(2)}$ is equal to the duration of V_o cutoff.

$$t_{RST(2)} = C \cdot R \cdot \ln \left(\frac{3}{0.9} \right) + 300\mu s$$

$$= 40 \cdot C + 300\mu s$$

*2 : Inside delay time (Typical values)

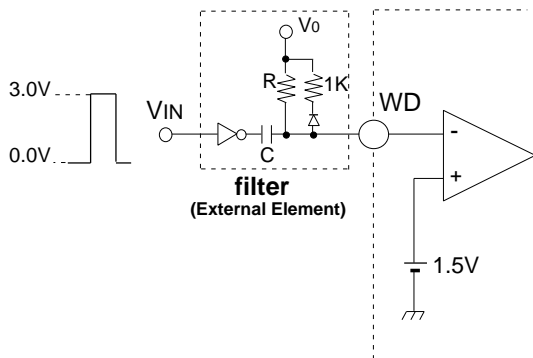
*3 : $R =$ Internal resistance



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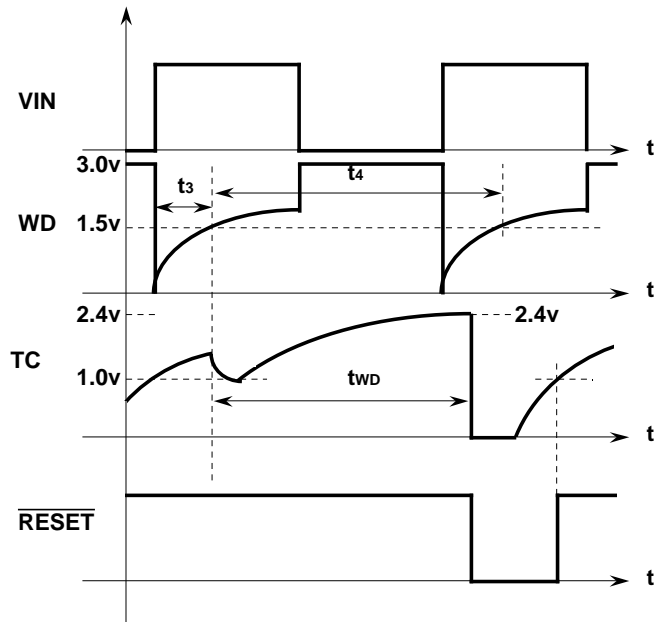
3. Relationship between the input pulse width and the low pass filter



Addition of a low pass filter makes input waveform dull. An input pulse width and CR of a low pass filter is determined referring to the right figure.

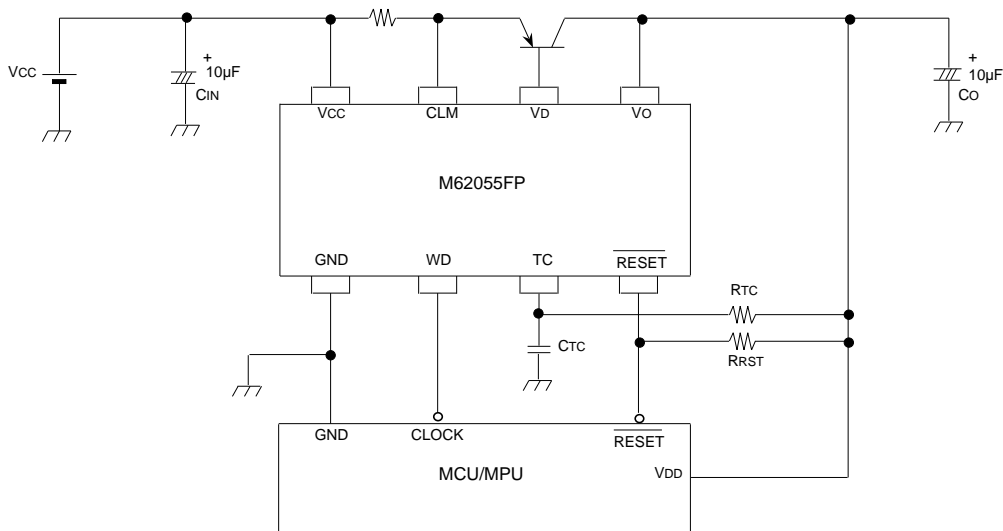
$$t_3 = -C \cdot R \cdot \ln \frac{1.5v}{V_{IN}}$$

$\overline{\text{RESET}}$ is output in the case of $t_4 > t_{wd}$.



If t_3 is too long, the TC waveform changes as shown in the diagram above.
 t_3 is set as follows; t_{wdIN} (3 μ s) or more and t_2 (charging time) or less.
 (t_2 is a discharge time while an input is normal)

APPLICATION



Note : h_{FE} of the external PNP transistor, 100 to 300 is recommended.