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Rev 2.0, 09/2003

Preliminary Information

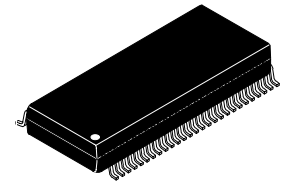
908E625

Integrated Quad Half H-Bridge with Power Supply, Embedded MCU, and LIN Serial Communication

H-BRIDGE POWER SUPPLY WITH EMBEDDED MCU AND LIN

The 908E625 is a highly integrated single-package solution that includes a high-performance HC08 microcontroller with a SMARTMOS™ analog control IC. The HC08 includes flash memory, a timer, enhanced serial communications interface (ESCI), an analog-to-digital converter (ADC), serial peripheral interface (SPI), and an internal clock generator module. The analog control die provides fully protected H-Bridge/high-side outputs, voltage regulator, watchdog, and local interconnect network (LIN) physical layer.

The single-package solution, together with LIN, provides optimal application performance adjustments and space-saving PCB design. It is especially suited for the control of automotive mirror, door lock, and light-levelling applications.



DWB SUFFIX
CASE 1400-01
54-TERMINAL SOICWB-EP

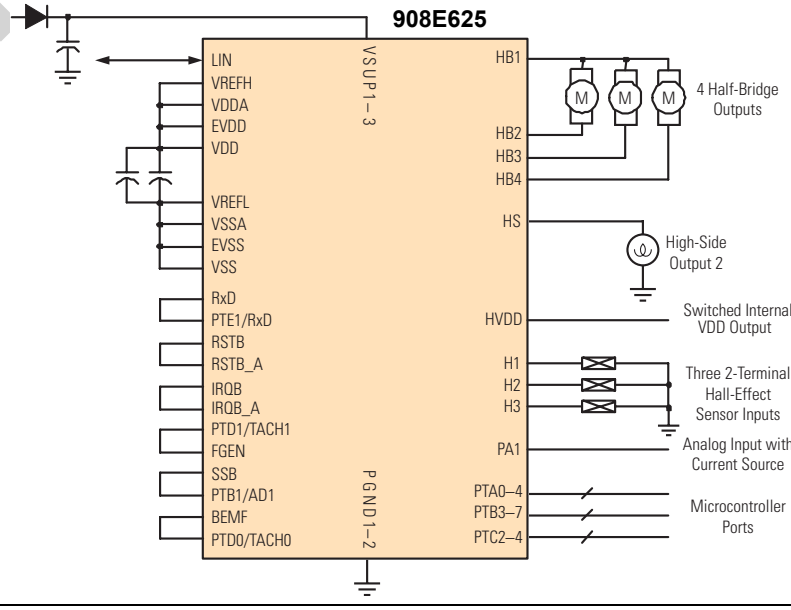
Features

- High-Performance M68HC08 Core
- 16 K Bytes of On-Chip Flash Memory
- 512 Bytes of RAM
- Two 16-Bit, 2-Channel Timers
- 10-Bit Analog-to-Digital Converter (ADC)
- Three 2-Terminal Hall-Effect Sensor Input Ports
- One Analog Input with Switchable Current Source
- Four Low $R_{DS(ON)}$ Half-Bridge Outputs
- One Low $R_{DS(ON)}$ High-Side Output
- 16 Microcontroller I/Os

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
PM908E625ACDWB/R2	-40°C to 85°C	54 SOIC WB-EP

908E625 Simplified Application Diagram



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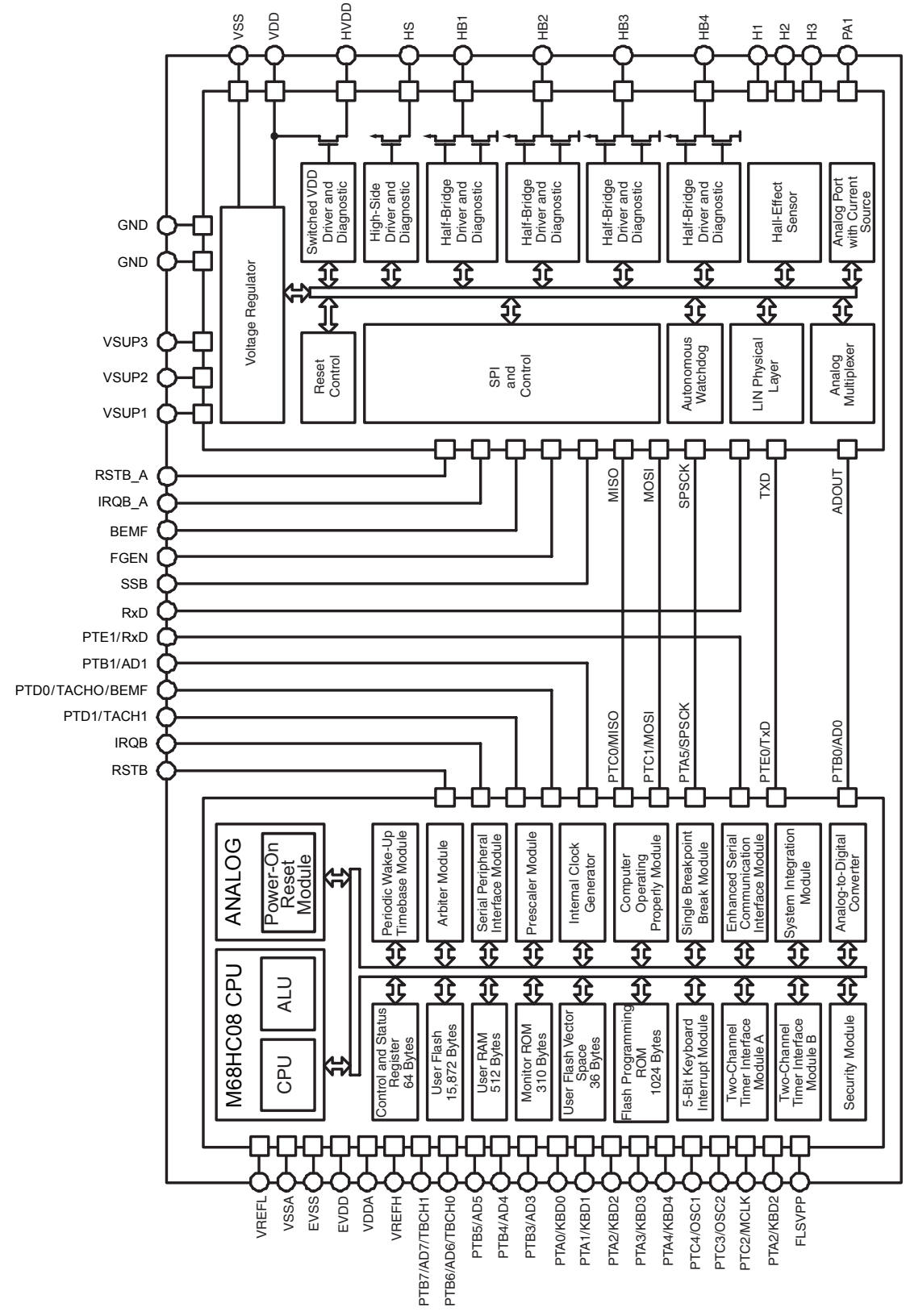
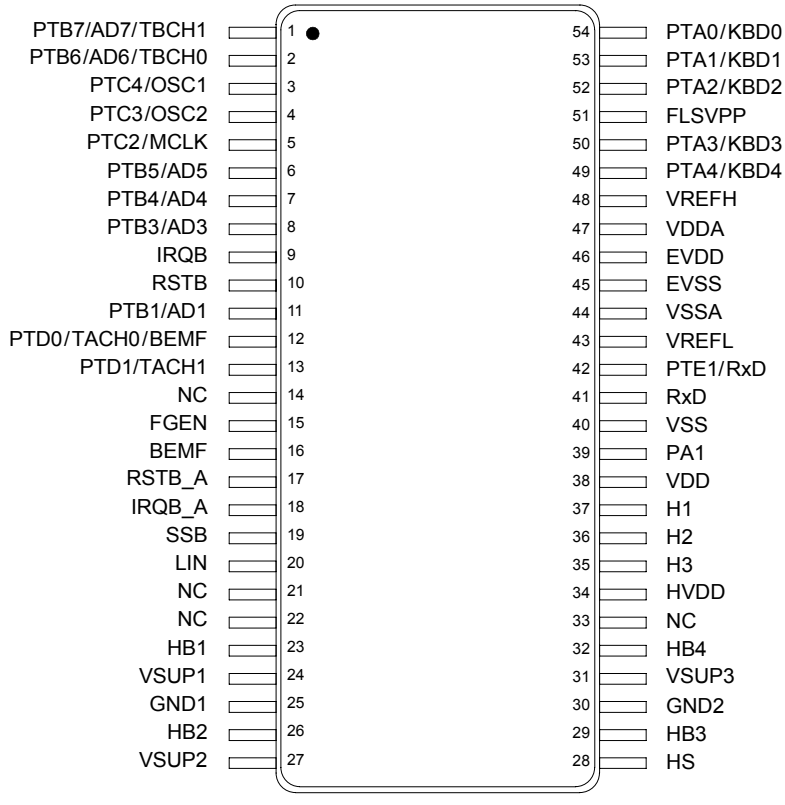


Figure 1. 908E625 Simplified Internal Block Diagram



TERMINAL FUNCTION DESCRIPTION

Terminal	Terminal Name	Die	Description
1	PTB7/AD7/ TBCH1	MCU	Port B, Terminal 7 (shared with ADC and Timer Channel B)
2	PTB6/AD6/ TBCH0	MCU	Port B, Terminal 6 (shared with ADC and Timer Channel B)
3	PTC4/OSC1	MCU	Port C, Terminal 4
4	PTC3/OSC2	MCU	Port C, Terminal 3
5	PTC2/MCLK	MCU	Port C, Terminal 2
6	PTB5/AD5	MCU	Port B, Terminal 5 (shared with ADC)
7	PTB4/AD4	MCU	Port B, Terminal 4 (shared with ADC)
8	PTB3/AD3	MCU	Port B, Terminal 3 (shared with ADC)
9	IRQB	MCU	Interrupt Input Terminal
10	RSTB	MCU	Reset Terminal
11	PTB1/AD1	MCU	Port B, Terminal 1 (shared with ADC)
12	PTD0/TACH0/ BEMF	MCU	Port D, Terminal 0 (shared with ADC, Timer Channel A, and BEMF Counter)
13	PTD1/TACH1	MCU	Port D, Terminal 1 (shared with ADC and Timer Channel A)
14, 21, 22, 33	NC	–	No Connected

TERMINAL FUNCTION DESCRIPTION (continued)

Terminal	Terminal Name	Die	Description
15	FGEN	Analog	Current Limitation Frequency Input Terminal
16	BEMF	Analog	Back Electromagnetic Force Output Terminal
17	RSTB_A	Analog	Reset Terminal
18	IRQB_A	Analog	Interrupt Output Terminal
19	SSB	Analog	SPI Port—Slave Select Terminal
20	SIO	Analog	LIN Bus Line
23, 26, 29, 32	HB1, HB2, HB3, HB4	Analog	Half-Bridge Outputs 1 to 4 Terminals
24, 27, 31	VSUP1, VSUP2, VSUP3	Analog	Supply Voltage Terminals 1 to 3
25, 30	GND1, GND2	Analog	Ground Terminals 1 and 2
28	HS	Analog	High-Side Output Terminal
34	HVDD	Analog	Switchable 5.0 V Output
35–37	H3, H2, H1	Analog	Hall-Effect Sensor Input Terminals 3 to 1
38	VDD	Analog	Voltage Regulator Output Terminal
39	PA1	Analog	Input Terminal (with Current Source)
40	VSS	Analog	Voltage Regulator Ground Terminal
41	RxD	Analog	LIN Receiver Output Terminal
42	PTE1/RxD	MCU	Port E, Terminal 1 (shared with SCI RX Line)
43, 48	VREFL, VREFH	MCU	ADC Supply Terminals
44	VSSA	MCU	Supply Terminal
45	EVSS	MCU	Supply Terminal
46	EVDD	MCU	Supply Terminal
47	VDDA	MCU	Supply Terminal
49	PTA4/KBD4	MCU	Port A, Terminal 4 (shared with Keyboard Module)
50	PTA3/KBD3	MCU	Port A, Terminal 3 (shared with Keyboard Module)
51	DNC	MCU	FLSVPP Test Terminal
52	PTA2/KBD2	MCU	Port A, Terminal 2 (shared with Keyboard Module)
53	PTA1/KBD1	MCU	Port A, Terminal 1 (shared with Keyboard Module)
54	PTA0/KBD0	MCU	Port A, Terminal 0 (shared with Keyboard Module)

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage Analog Chip Supply Voltage under Normal Operation (Steady-State) Analog Chip Supply Voltage under Transient Conditions (Note 1) Microcontroller Chip Supply Voltage	 $V_{SUP(ss)}$ $V_{SUP(pk)}$ V_{DD}	 -0.3 to 28 -0.3 to 40 -0.3 to 6.0	V
Input Terminal Voltage Analog Chip (Note 2) Microcontroller Chip	 $V_{in(ANALOG)}$ $V_{in(MCU)}$	 -0.3 to 5.5 V_{SS}-0.3 to V_{DD}+0.3	V
Maximum Microcontroller Current per Terminal All Terminals Except VDD/VSS/PTA0–PTA6/PTC0–PTC1 Terminals PTA0–PTA6 and PTC0–PTC1	 $I_{pin(1)}$ $I_{pin(2)}$	 ±15 ±25	mA
Maximum Microcontroller V_{SS} Output Current	I_{MVSS}	100	mA
Maximum Microcontroller V_{DD} Input Current	I_{MVDD}	100	mA
LIN Supply Voltage (Note 3) Normal Operation (Steady-State) Transient Conditions (Note 1)	 $V_{BUS(ss)}$ $V_{BUS(dynamic)}$	 -18 to 28 40	V
Output Self-Limiting Current (Note 4)	$I_{OUT(lim)}$	5.0	A
ESD Voltage Human Body Model (Microcontroller/SmartMOS) (Note 5) Machine Model (Note 6) Charge Device Model	 V_{ESD1} V_{ESD2} V_{ESD3}	 ±2000/±4000 ±200 ±500	V
THERMAL RATINGS			
Storage Temperature	T_{STG}	-40 to 150	°C
Operating Case Temperature (Note 7)	T_C	+85	°C
Operating Junction Temperature	T_J	-40 to 125	°C
Terminal Soldering Temperature (Note 8)	T_{SOLDER}	245	°C
Thermal Resistance (Junction to Ambient) All Outputs ON (Note 9), (Note 11) Single Output ON (Note 10), (Note 11)	 $R_{\theta JA1}$ $R_{\theta JA2}$	 24 27	°C/W

Notes

1. Transient capability for pulses with a time of t < 0.5 sec.
2. Exceeding the limits on any parallel input, SSB, or Reset terminal may cause permanent damage to the devices.
3. Exceeding the limits on the LIN terminal may cause permanent damage to the device.
4. Overcurrent shutdown on HB1/HB2/HB3/HB4 and HS terminals.
5. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
6. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
7. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
8. Terminal soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. All outputs ON and dissipating equal power.
10. One output ON and dissipating power.
11. Per JEDEC JESD51-2 at natural convection, still air condition; and 2s2p thermal test board per JEDEC JESD51-7 and JESD51-5 (thermal vias connected to top ground plane).

STATIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE RANGE					
Nominal Operating Voltage	V_{SUP}	8.0	–	18	V
SUPPLY CURRENT RANGE					
STOP Mode (Note 12) V_{SUP} = 12 V, Cyclic Wake-Up Disabled	$I_{SUPSTOP}$	–	–	60	μA
DIGITAL INTERFACE RATINGS					
Output Terminals (RSTB, IRQ, BEMF)					V
High-State Output Voltage (I_{OUT} = 1.5 mA)	V_{OH}	3.75	–	–	
Low-State Output Voltage (I_{OUT} = - 250 μA)	V_{OL}	–	–	0.9	
Input Terminals (RSTB, IRQ, FGEN, SSB)					V
Input Logic Low Voltage	V_{ILL}	–	–	1.5	
Input Logic High Voltage	V_{ILH}	3.5	–	–	
Input Terminals (RSTB, IRQ, FGEN, SSB) - Input Logic Hysteresis	V_{IHH}	100	550	800	mV
Input Terminals (RSTB, IRQ, FGEN, SSB) - Input Current (0 V < V_{IN} < V_{DD})	I_{IN}	–	20	–	μA
Input Terminals (RSTB, IRQ, FGEN, SSB) - Input Capacitance (Note 13)	C_{IN}	–	TBD	–	pF
Input Terminals (RSTB, IRQ, FGEN, SSB) - Pull-up Resistor (IRQ, RSTB, SSB)	R_{Pullup}	–	60	–	kΩ
SYSTEM RESETS AND INTERRUPTS					
High-Voltage Reset					V
Threshold	V_{HVRON}	27	30	33	
Hysteresis	V_{HVRH}	–	1.5	–	
Low-Voltage Reset					
Threshold	V_{LVRON}	3.6	4.0	4.5	V
Hysteresis	V_{LVRH}		100		mV
High-Voltage Interrupt					V
Threshold	V_{HVION}	17.5	21	23	
Hysteresis	V_{HVIH}	–	1.0	–	
Low-Voltage Interrupt					V
Threshold	V_{LVION}	6.5	–	8.0	
Hysteresis	V_{LVIH}	–	0.4	–	
High-Temperature Reset (Note 14)					°C
Threshold	T_{RON}	–	170	–	
Hysteresis	T_{IH}	5.0	–	–	

Notes

12. STOP mode current will increase if V_{SUP} exceeds 15 V.
13. This parameter is guaranteed by process monitoring but is not tested in production.
14. High-Temperature Interrupt (HTI) threshold is linked to High-Temperature Reset (HTR) threshold (HTR = HTI + 10°C).

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS (continued)					
High-Temperature Interrupt					°C
Threshold	T_{ION}	–	160	–	
Hysteresis	T_{IH}	5.0	–	–	
VOLTAGE REGULATOR					
Normal Mode Output Voltage					V
I_{OUT} = 60 mA, 9.0 V < V_{SUP} < 16 V	V_{DDRUN1}	4.75	5.0	5.25	
I_{OUT} = 60 mA, V_{SUP} < 9.0 V and V_{SUP} > 16 V	V_{DDRUN2}	4.5	5.0	5.5	
Normal Mode Total Output Current	I_{OUTRUN}	60	–	–	mA
Load Regulation	V_{LR}				mA
I_{OUT} = 60 mA, V_{SUP} = 9.0 V, T_J = 125°C		–	–	100	
STOP Mode Output Voltage (Max. Output Current 100 μA)	V_{DDSTOP}	4.5	4.7	4.9	V
Low-Voltage Reset Threshold	V_{LVRON}	3.6	4.0	4.5	V
Low-Voltage Reset Hysteresis	V_{LVRH}	50	100	150	mV
PHYSICAL LAYER					
Output Low Level	$V_{LIN-LOW}$				V
Tx Low, I_{OUT} = 40 mA		–	–	1.4	
Output High Level	$V_{LIN-HIGH}$				V
Tx High, I_{OUT} = 1.0 μA		V_{SUP}-1	–	–	
Pull-Up Resistor to V_{SUP}	R_{SLAVE}	20	30	60	kΩ
Output Current Limit	I_{BLIM}	50	–	–	mA
Leakage Current to GND	I_{LEAK1}				μA
Recessive State (-0.5 V < V_{BUS} < V_{SUP})		0	–	10	
Leakage Current to GND (V_{SUP} Disconnected)					μA
Excluding Internal Pull-Up Resistor, V_{LIN} Between -18 V and +18 V	I_{LEAK2}	-40	–	40	
Including Internal Pull-Up Resistor, V_{LIN} @ -18 V	I_{LEAK3}	–	-600	–	
Including Internal Pull-Up Resistor, V_{LIN} @ +18 V	I_{LEAK4}	–	25	–	
LIN Receiver					V
Recessive	V_{IH}	0.6 V_{BUS}	–	V_{SUP}	
Dominant	V_{IL}	0	–	0.4 V_{BUS}	
Threshold	V_{ITH}	–	V_{SUP}/2	–	
Input Hysteresis	VIH	0.05 V_{SUP}	–	0.1 V_{SUP}	
LIN Wake-Up Threshold	V_{WTH}	–	V_{SUP}-3	–	V

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HIGH-SIDE OUTPUT					
Switch On Resistance @ T_J = 25°C with I_{LOAD} = 1.0 A	$R_{DS(ON)-HS}$	–	600	700	mΩ
High-Side Overcurrent Shutdown	I_{HSOC}	4.0	–	6.5	A
High-Side Switching Frequency	f_{PWMHS}	–	–	20	kHz
HALF-BRIDGE OUTPUTS					
Switch On Resistance @ T_J = 25°C with I_{LOAD} = 1.0 A	$R_{DS(ON)HB}$				mΩ
High Side		–	425	500	
Low Side		–	400	500	
High-Side Overcurrent Shutdown	I_{HBOC}	5.0	–	8.0	A
Low-Side Overcurrent VDS Voltage	V_{OCDS}	–	3.6	–	V
High-Side Switching Frequency	f_{PWMHS}	–	20	–	kHz
Low-Side Switching Frequency	f_{PWMLS}	–	25	–	kHz
Low-Side Current Limitation					mA
Current Limit 1 (CLS2 = 0, CLS1 = 1, CLS0 = 1)	I_{CL1}	35	55	75	
Current Limit 2 (CLS2 = 1, CLS1 = 0, CLS0 = 0)	I_{CL2}	210	260	310	
Current Limit 3 (CLS2 = 1, CLS1 = 0, CLS0 = 1)	I_{CL3}	300	370	440	
Current Limit 4 (CLS2 = 1, CLS1 = 1, CLS0 = 0)	I_{CL4}	450	550	650	
Current Limit 5 (CLS2 = 1, CLS1 = 1, CLS0 = 1)	I_{CL5}	600	740	880	
Half-Bridge Output HIGH Threshold for BEMF Detection	V_{BEMFH}	–	–	0	V
Half-Bridge Output LOW Threshold for BEMF Detection	V_{BEMFL}	–	-60	-10	mV
Hysteresis for BEMF Detection	V_{BEMFHY}	–	60	–	mV
Low-Side Current-to-Voltage Ratio (V_{ADOUT} [V] / I_{HB} [A])					V/A
CSA = 1	$RATIO_H$	7.0	10	13	
CSA = 0	$RATIO_L$	1.4	2.0	2.6	
SWITCHABLE V_{DD} OUTPUT (HV_{DD})					
Overcurrent Shutdown Threshold	$I_{HVDDOCT}$	24	30	36	mA
V_{SUP} DOWN-SCALER					
Voltage Ratio ($RATIO_{VSUP}$ = V_{SUP} /V_{ADOUT}	$RATIO_{VSUP}$	4.85	5.1	5.35	–
HALL-EFFECT SENSOR INPUT TERMINAL					
Output Voltage	V_{HALL}	–	V_{SUP}	15	V
Sense Current					mA
Threshold	I_{HSCT}	7.0	8.8	10.6	
Hysteresis	I_{HSCH}	–	0.88	–	
Output Current Limitation	I_{HL}	–	100	–	mA
PHOC Flag Threshold	I_{PHOCT}	–	3.5	–	V
Drop-Out Voltage @ I_{LOAD} = 15 mA	V_{PH-DO}	–	0.5	–	V

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ANALOG INPUT					
Current Source PAx					μA
CSSEL1 = 0, CSSEL0 = 0	t_{CS1}	60	70	80	
CSSEL1 = 0, CSSEL0 = 1	t_{CS2}	180	210	240	
CSSEL1 = 1, CSSEL0 = 0	t_{CS3}	380	420	460	
CSSEL1 = 1, CSSEL0 = 1	t_{CS4}	625	700	775	

DYNAMIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Please refer to the specification for 68HC908EY16 for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PHYSICAL LAYER					
Propagation Delay					µs
Tx Low to LIN Low	$t_{TX\text{-}LIN\text{-}low}$	–	–	4.0	
Tx High to LIN High	$t_{TX\text{-}LIN\text{-}high}$	–	–	4.0	
LIN Low to Rx Low	$t_{LIN\text{-}Rx\text{-}low}$	–	4.0	6.0	
LIN High to Rx High	$t_{LIN\text{-}Rx\text{-}high}$	–	4.0	6.0	
Bus Wake-Up to $\overline{IRQ}$ Low	t_{PDWU}	–	TBD	–	
Output Falling Edge Slew Rate	SR_F				V/µs
80% to 20%		-1.0	-2.0	-3.0	
Output Rising Edge Slew Rate	SR_R				V/µs
20% to 80%, R_{BUS} > 1.0 kΩ, C_{BUS} < 10 nF		1.0	2.0	3.0	
Rise/Fall Slew Rate Symmetry	SR_S	-2.0	–	2.0	µs
HALL-EFFECT SENSOR INPUT PORT					
Dynamic Output Voltage Range	V_{DR}	1.5	–	–	V
Propagation Delay	t_{PHPD}	–	1.0	–	µs
AUTONOMOUS WATCHDOG (AWD)					
AWD Oscillator Period	t_{OSC}	–	40	–	µs
AWD Period Low = 512 * t_{OSC}	t_{AWDPH}	16	22	28	ms
AWD Period High = 256 * t_{OSC}	t_{AWDPL}	8.0	11	14	ms

MICROCONTROLLER

For a detailed microcontroller description, refer to the MC68HC908EY16 specification.

Module	Description
Core	High-Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	2 x 16-Bit Timers with 2 Channels (TIM A and TIM B)
Flash	16 K Bytes
RAM	512 Bytes
ADC	10-Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard SCI Module Bit-Time Measurement Arbitration Prescaler with Fine Baud-Rate Adjustment
ICG	Internal Clock Generation Module (25% Accuracy with Trim Capability to 2%)
BEMF Counter	Special Counter for SmartMOS BEMF Output

Timing Diagrams

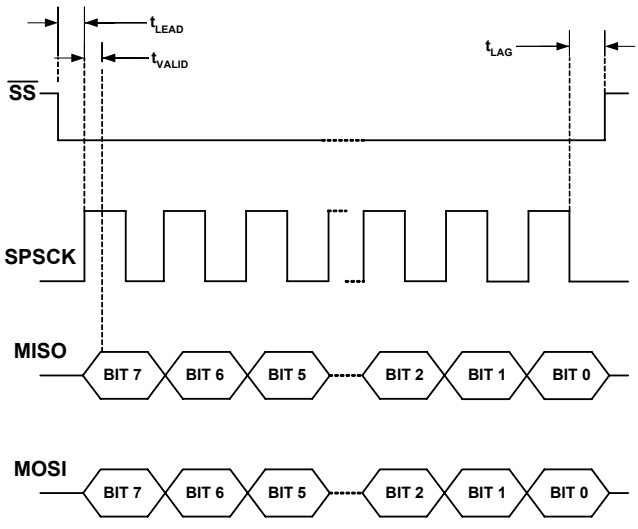


Figure 2. SPI Timing Diagram

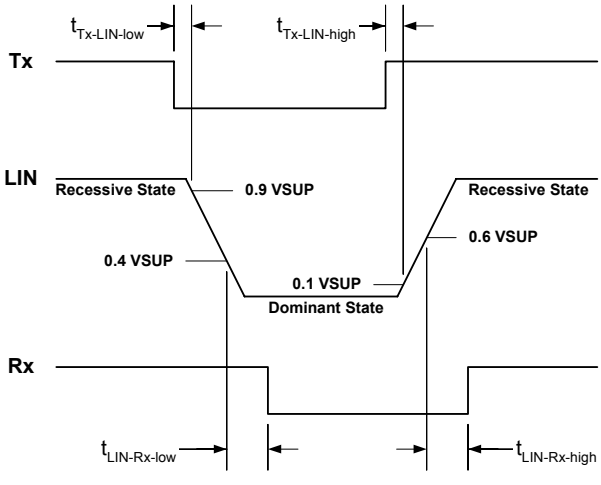


Figure 3. LIN Timing Description

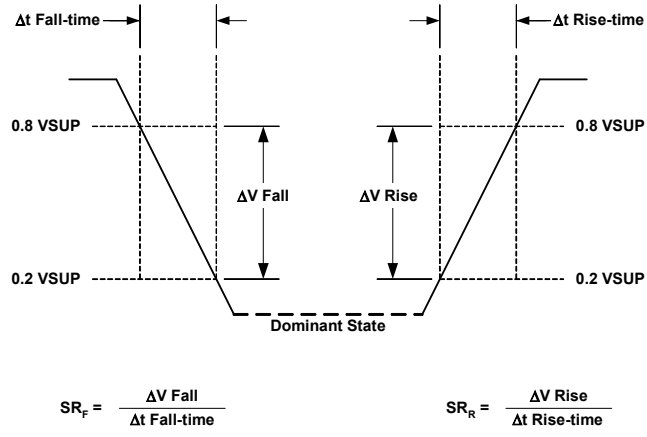


Figure 4. LIN Slew Rate Description

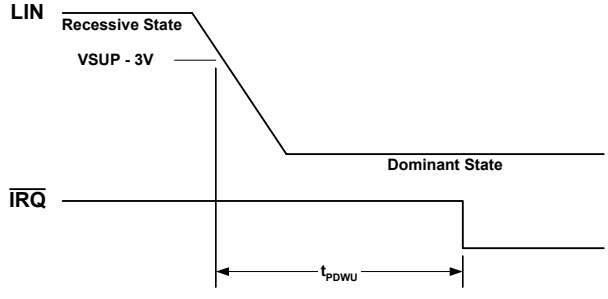


Figure 5. Wake-Up Terminal Wake-Up Timing

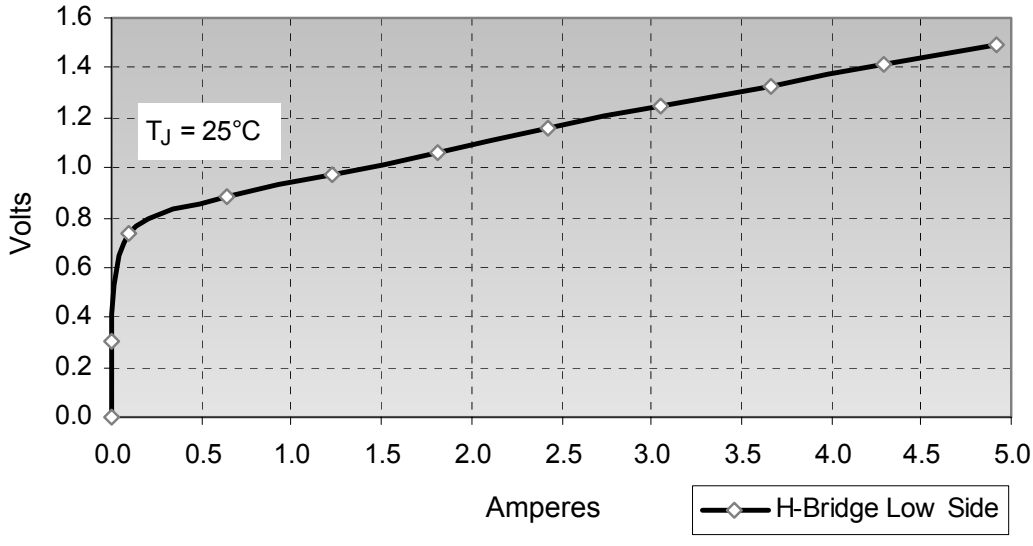


Figure 6. Free Wheel Diode Forward Voltage

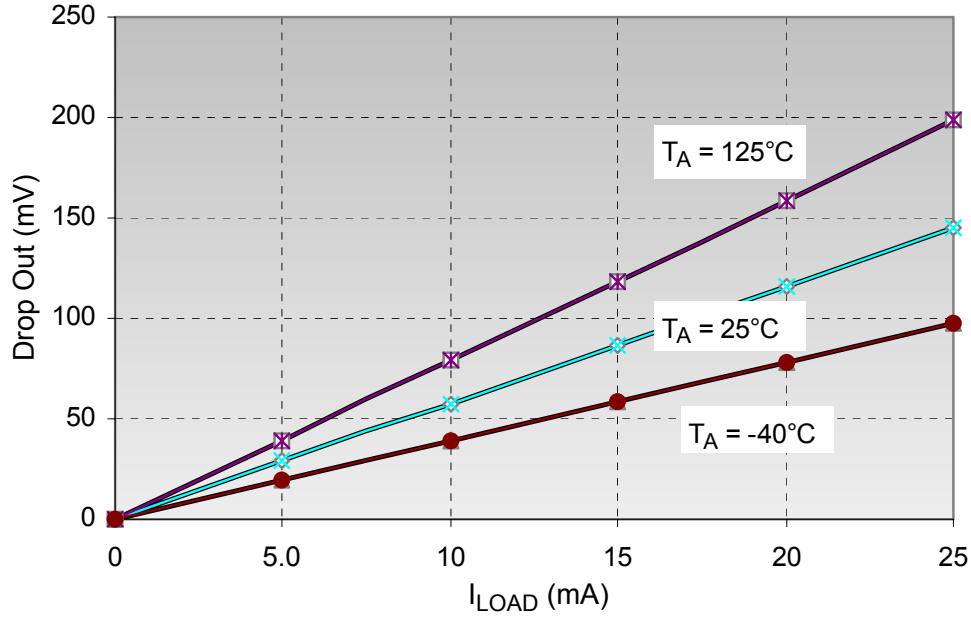


Figure 7. Drop-Out Voltage on HVDD

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 908E625 device was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E625 is well suited to perform complete mirror, door lock, and light-levelling control all via a 3-wire LIN bus.

This device combines an HC08 MCU core with flash memory together with a SmartMOS IC chip. The SmartMOS IC chip combines power and control in one chip. Power switches are provided on the SmartMOS IC configured as half-bridge outputs with one high-side switch. Other ports are also provided, which include Hall sensor input ports, analog input ports, a wake-up terminal, and a selectable HVDD terminal. An internal voltage regulator is provided on the SmartMOS IC chip, which provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and the third for ground.

FUNCTIONAL TERMINAL DESCRIPTION

Power Supply Terminals (VSUP1, VSUP2, and VSUP3)

Terminals are device power supply terminals. The nominal input voltage is designed for operation from 12 V systems. Owing to the low on-resistance and current requirements of the half-bridge driver outputs and high-side output driver, multiple terminals are provided.

All VSUP terminals must be connected to get full chip functionality.

Power Ground Terminals (GND1 and GND2)

GND1 and GND2 are device power ground connections. Owing to the low on-resistance and current requirements of the half-bridge driver outputs and high-side output driver, multiple terminals are provided.

All GND terminals must be connected to get full chip functionality.

Half-Bridge Output Terminals (HB1, HB2, HB3, and HB4)

The 908E625 device includes power MOSFETs configured as four half-bridge driver outputs with a $R_{DS(ON)}$ of 500 mΩ. These outputs may be configured for stepper-motor drivers, DC motor drivers, or as high-side and low-side switches.

These outputs are short-circuit and overtemperature protected, and they feature current recopy, current limitation, and BEMF generation. The protection is done on the high-side and low-side FETs (high-side with real current measurement and low-side with VDS monitoring), while current limitation and recopy are done on the low-side FETs.

High-Side Output Terminal (HS)

This output is a low $R_{DS(ON)}$ high-side switch. The switch is protected against overtemperature and overcurrent. The output is capable of limiting the inrush current with an automatic PWM generation using the FGEN module.

Hall-Effect Sensor Input Terminals (H1, H2, and H3)

The Hall-effect sensor input terminals provide inputs for Hall-effect sensors and switches.

Analog Input (PA1)

This terminal is an analog input port with selectable source values.

Switchable V_{DD} Output Terminal (HVDD)

Terminal HVDD is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply (e.g., 3-terminal Hall-effect sensors). The output is short-circuit protected.

LIN Bus Terminal (LIN)

This terminal represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN Bus Specification.

Non-Power Ground Terminal (VSS)

Ground terminal for the connection of all non-power ground connections (microcontroller and sensors).

Note VSS, EVSS, VSSA, and VREFL must be connected together.

+5.0 V Supply Output Terminal (VDD)

Voltage regulator output terminal. Terminal needed to place an external capacitor to stabilize the regulated output voltage. This terminal is not protected against shorts to GND. Therefore, it should not be used to supply loads others than the implemented microcontroller.

Note VDD, EVDD, VDDA, and VREFH must be connected together.

Slave Select (SSB)

This is terminal is the SPI Slave Select terminal for the analog chip. All other SPI connections are done internally. SSB must be connected to PTB1 or any other logic I/O of the microcontroller.

Interrupt Terminal (IRQB_A)

IRQ_A is the interrupt output terminal of the analog die indicating errors or wake-up events. This terminal must be connected to the IRQB terminal of the MCU.

Reset Terminal (RSTB_A)

RSTB_A is the bidirectional reset terminal of the analog die. This terminal needs to be connected to the RSTB terminal of the MCU.

BEMF Terminal

This terminal gives the user information about back electromagnetic force (BEMF). This feature is mainly used in stepper motor applications for detecting a stalled motor. In order to evaluate this signal the terminal must be directly connected to terminal PTD0/TACH0/BEMF.

FGEN Terminal

Input terminal for the half-bridge current limitation and the HS inrush current limiter PWM frequency. This input is not a real PWM input terminal; it should just supply the period of the PWM. The duty cycle will be generate automatically.

Port A I/O Terminals

Port A input/output (I/O) terminals (PTA6/SS, PTA5/SPSCK, PTA4/KDB4, PTA3/KBD3, PTA2/KBD2, PTA1/KBD1, and PTA0/KBD0) are special-function, bidirectional I/O port terminals. PTA5 is shared with the serial peripheral interface (SPI). PTA4–PTA0 can be programmed to serve as keyboard interrupt terminals.

PTA5 is shared with the serial peripheral interface (SPI) but not directly accessible in the multichip approach. This terminal is internally directly connected to the SPI clock of the analog die.

PTA6 is not accessible in the multi-die approach.

For details refer to 68HC908EY16 Specification.

Port B I/O Terminals

PTB7/AD7/TBCH1, PTB6/AD6/TBCH0, and PTB5/AD5–PTB0/AD0 are special-function, bidirectional I/O port terminals that can also be used for ADC inputs. PTB7/AD7/TBCH1 and PTB6/AD6/TBCH0 are special function.

PTB2 is not accessible in the multi-die approach.

PTB0 is internally directly connected to terminal ADOUT. This input is used for all analog measurements done by the analog die (e.g., current recopy, V_{SUP}, etc.).

For details refer to the 68HC908EY16 specification.

Port C I/O Terminals

PTC4/OSC1 and PTC0/MISO are special-function, bidirectional I/O port terminals. PTC3/OSC2 and PTC4/OSC1 are shared with the on-chip oscillator circuit through configuration options.

For details refer to the 68HC908EY16 specification.

Depending on application requirements:

- PTC3/OSC2 can be programmed to be OSC2.
- PTC4/OSC1 can be programmed to be OSC1.
- PTC2/MCLK is software selectable to be MCLK or bus clock out.

PTC0 and PTC1 are not directly accessible in the multi-die approach. These terminals are internally connected to the MISO and MOSI SPI terminals of the analog die.

Port D I/O Terminals (PTD1/TACH1 and PTD0/TACH0/BEMF)

PTD1/TACH1 and PTD0/TACH0 are special-function, bidirectional I/O port terminals that can also be programmed to be timer terminals.

In stepper motor applications the PTD0 terminal should be connected to the BEMF output of the analog die in order to evaluate the BEMF signal without using a timer channel.

PTD1 terminal is recommended to be used as an output terminal for generating the FGEN signal if required by the application.

Port E I/O Terminals (PTE1/RxD and PTE0/TxD)

PTE1/RxD and PTE0/TxD are special-function, bidirectional I/O port terminals that can also be programmed to be enhanced serial communication.

PTE0/TxD is internally connected to the TxD terminal of the analog die. The connection for the receiver functionality must be done externally.

External Reset Terminal (RSTB)

A logic [0] on the RSTB terminal forces the MCU to a known startup state. RSTB is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. This terminal contains an internal pull-up resistor that is always activated, even when the reset terminal is pulled low.

For details refer to the 68HC908EY16 specification.

External Interrupt Terminal (IRQB)

IRQB is an asynchronous external interrupt terminal. This terminal contains an internal pull-up resistor that is always activated, even when the IRQB terminal is pulled low.

For details refer to the 68HC908EY16 specification.

Power Supply Terminals (VDD and VSS)

VDD and VSS are the power supply and ground terminals. The MCU operates from a single power supply.

Fast signal transitions on MCU terminals place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details refer to the 68HC908EY16 specification.

Analog Power Supply/Reference Terminals (VDDA, VREFH, VSSA, and VREFL)

VDDA and VSSA are the power supply terminals for the analog-to-digital converter (ADC). Decoupling of these terminals should be as per the digital supply.

Note VREFH is the high reference supply for the ADC. VDDA should be tied to the same potential as VDD via separate traces. VREFL is the low reference supply for the ADC. VSSA should be tied to the same potential as VSS via separate traces.

For details refer to the 68HC908EY16 specification.

ANALOG DIE DESCRIPTION

Interrupt Description

The device has seven different interrupt sources. The interrupts can be disabled or enabled via the SPI. After RESET all interrupts are automatically disabled.

Low-Voltage Interrupt

The Low-Voltage Interrupt (LVI) is related to the external supply voltage, V_{SUP}. If this voltage falls below the LVI threshold, it will set the LVI flag. In case the low-voltage interrupt is enabled, an interrupt will be initiated.

With LVI the H-Bridges (high-side FET only) and the Lamp driver are switched off. All other modules are not influenced by this interrupt.

During STOP mode the LVI circuitry is disabled.

High-Voltage Interrupt

The High-Voltage Interrupt (HVI) is related to the external supply voltage, V_{SUP}. If this voltage rises above the HVI threshold it will set the HVI flag. In case the High-Voltage Interrupt is enabled, a interrupt will be initiated.

With HVI the H-Bridges (high-side FET only) and the Lamp and the high-side driver are switched off. All other modules are not influenced by this interrupt.

During STOP mode the HVI circuitry is disabled.

High-Temperature Interrupt

The High-Temperature Interrupt (HTI) is generated by the on-chip temperature sensors. If the chip temperature is above the HTI threshold, the HTI flag will be set. In case the High-Temperature Interrupt is enabled, a interrupt will be initiated.

During STOP mode the HTI circuitry is disabled.

Autonomous Watchdog Interrupt (AWD)

Refer to Autonomous Watchdog (AWD) on page 35.

SIO Interrupt

If the ISOIE bit is set, a falling edge on the SIO terminal will generate an interrupt. During STOP mode this interrupt will initiate a system wake-up.

Hall-Effect Sensor Input Terminal Interrupt

If the PHIE bit is set, the enabled Hall-effect sensor input terminals H0–H2 can generate an interrupt if a current above the threshold is detected. During STOP mode this interrupt, combined with the cyclic wake-up feature of the AWD, can wake up the system (refer to Hall-Effect Sensor Input Terminal section).

Overcurrent Interrupt

If an overcurrent condition on a half-bridge occurs, the high-side or the HVDD output is detected and the OCIE bit is set and an interrupt generated.

System Wake-Up

System wake-up can be initiated by four sources:

1. A falling edge on the SIO terminal.
2. A wake-up signal from the AWD.
3. Logic [1] at Hall-effect sensor input terminal during cyclic check via AWD.
4. An LVR condition occurs.

If one of these wake-up events occurs and the interrupt mask bit for this event is set, the interrupt will wake up the microcontroller as well as the main voltage regulator (MREG) (see Figure 8).

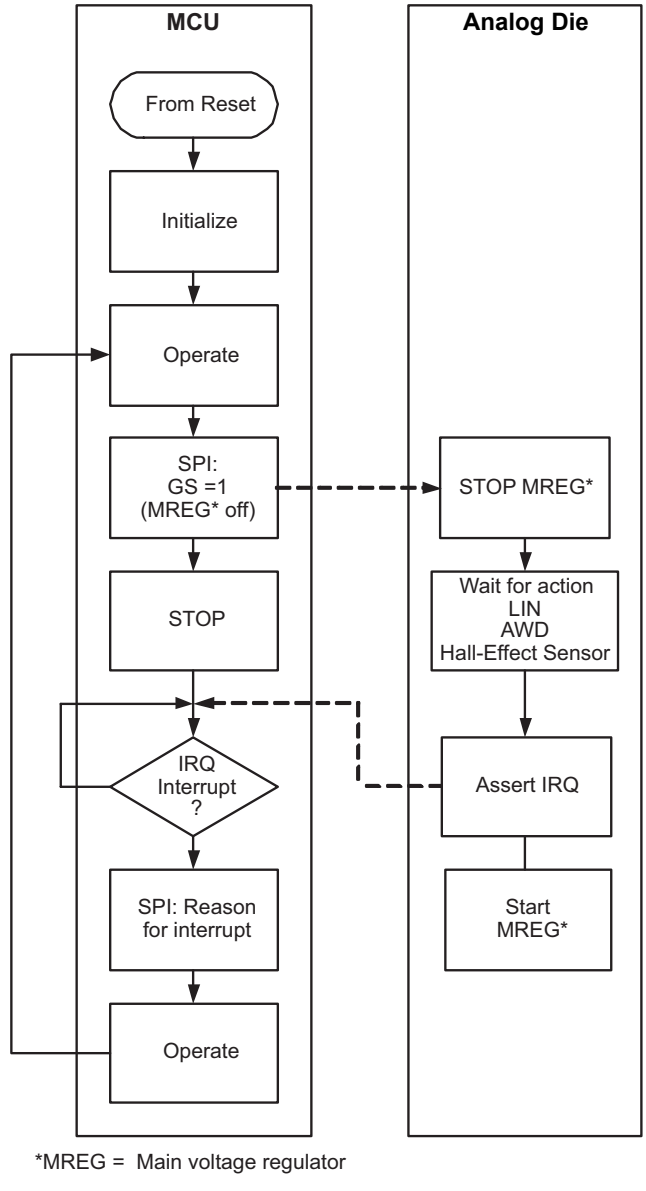


Figure 8. STOP Mode/Wake-Up Procedure

Interrupt Flag Register

Register Name and Address: IFR - $05

	Bit7	6	5	4	3	2	1	Bit0
Read	0	PHF	ISOF	HTF	LVF	HVF	OCF	0
Write								
Reset	0	0	0	0	0	0	0	0

PHF—Hall-Effect Sensor Input Terminal Flag Bit

This read/write flag is set depending on run/STOP mode.

RUN Mode Interrupt will generated when a state change on any enabled Hall-effect sensor input terminal is detected. Clear PHF by writing a logic [1] to PHF. Reset clears the PHF bit. Writing a logic [0] to PHF has no effect.

- 1 = State change on the hallflags detected.
- 0 = No state change on the hallflags detected.

STOP Mode Interrupt will be generated when AWDCC is set and a current above threshold is detected on any enabled Hall-effect sensor input terminal. Clear PHF by writing a logic [1] to PHF. Reset clears the PHF bit. Writing a logic [0] to PHF has no effect.

- 1 = One or more of the selected Hall-effect sensor input terminals had been pulled high.
- 0 = None of the selected Hall-effect sensor input terminals has been pulled high.

ISOF—ISO Flag Bit

This read/write flag is set on falling edge at the ISO9141 data line. Clear ISOF by writing a logic [1] to ISOF. Reset clears the ISOF bit. Writing a logic [0] to ISOF has no effect.

- 1 = Falling edge on ISO9141 data line has occurred.
- 0 = Falling edge on ISO9141 data line has not occurred since last clear.

HTF—High-Temperature Flag Bit

This read/write flag is set on high-temperature condition. Clear HTF by writing a logic [1] to HTF. If high-temperature condition is still present while writing a logical one to HTF, the writing has no effect. Therefore, a high-temperature interrupt cannot be lost due to inadvertent clearing of HTF. Reset clears the HTF bit. Writing a logic [0] to HTF has no effect.

- 1 = High-temperature condition has occurred.
- 0 = High-temperature condition has not occurred.

LVF—Low-Voltage Flag Bit

This read/write flag is set on low voltage condition. Clear LVF by writing a logic [1] to LVF. If low-voltage condition is still present while writing a logical one to LVF, the writing has no effect. Therefore, a low-voltage interrupt cannot be lost due to inadvertent clearing of LVF. Reset clears the LVF bit. Writing a logic [0] to LVF has no effect.

- 1 = Low-voltage condition has occurred.
- 0 = Low-voltage condition has not occurred.

HVF—High-Voltage Flag Bit

This read/write flag is set on high-voltage condition. Clear HVF by writing a logic [1] to HVF. If high-voltage condition is still present while writing a logical one to HVF, the writing has no effect. Therefore, a high-voltage interrupt cannot be lost due to inadvertent clearing of HVF. Reset clears the HVF bit. Writing a logic [0] to HVF has no effect.

- 1 = High-voltage condition has occurred.
- 0 = High-voltage condition has not occurred.

OCF—Overcurrent Flag Bit

This read-only flag is set on overcurrent condition. Reset clears the OCF bit. To clear this flag, write a logic [1] to the appropriate overcurrent flag in the SYSSTAT Register. See Figure 9, which shows the three signals triggering the OCF.

- 1 = High-current condition has occurred.
- 0 = High-current condition has not occurred.

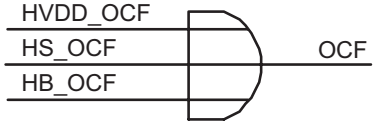


Figure 9. Principal Implementation for OCF

Interrupt Mask Register (IMR)

Register Name and Address: IMR - $04

	Bit7	6	5	4	3	2	1	Bit0
Read	0	PHIE	ISOIE	HTIE	LVIE	HVIE	OCIE	0
Write								
Reset	0	0	0	0	0	0	0	0

PHIE—Hall-Effect Sensor Input Terminal Interrupt Enable Bit

This read/write bit enables CPU interrupts by the Hall-effect sensor input terminal flag, PHF. Reset clears the PHIE bit.

- 1 = Interrupt requests from PHF flag enabled.
- 0 = Interrupt requests from PHF flag disabled.

ISOIE—ISO9141 Line Interrupt Enable Bit

This read/write bit enables CPU interrupts by the ISO flag, ISOF. Reset clears the ISOIE bit.

- 1 = Interrupt requests from ISOF flag enabled.
- 0 = Interrupt requests from ISOF flag disabled.

HTIE—High-Temperature Interrupt Enable Bit

This read/ write bit enables CPU interrupts by the high-temperature flag, HTF. Reset clears the HTIE bit.

- 1 = Interrupt requests from HTF flag enabled.
- 0 = Interrupt requests from HTF flag disabled.

LVIE—Low-Voltage Interrupt Enable Bit

This read/write bit enables CPU interrupts by the low-voltage flag, LVF. Reset clears the LVIE bit.

- 1 = Interrupt requests from LVF flag enabled.
- 0 = Interrupt requests from LVF flag disabled.

HVIE—High-Voltage Interrupt Enable Bit

This read/write bit enables CPU interrupts by the high-voltage flag, HVF. Reset clears the HVIE bit.

- 1 = Interrupt requests from HVF flag enabled.
- 0 = Interrupt requests from HVF flag disabled.

OCIE—Overcurrent Interrupt Enable Bit

This read/write bit enables CPU interrupts by overcurrent flag, OCF. Reset clears the OCIE bit.

- 1 = Interrupt requests from OCF flag enabled.
- 0 = Interrupt requests from OCF flag disabled.

Reset

The 908E625 chip has four internal and one external reset sources, as shown in Figure 10.

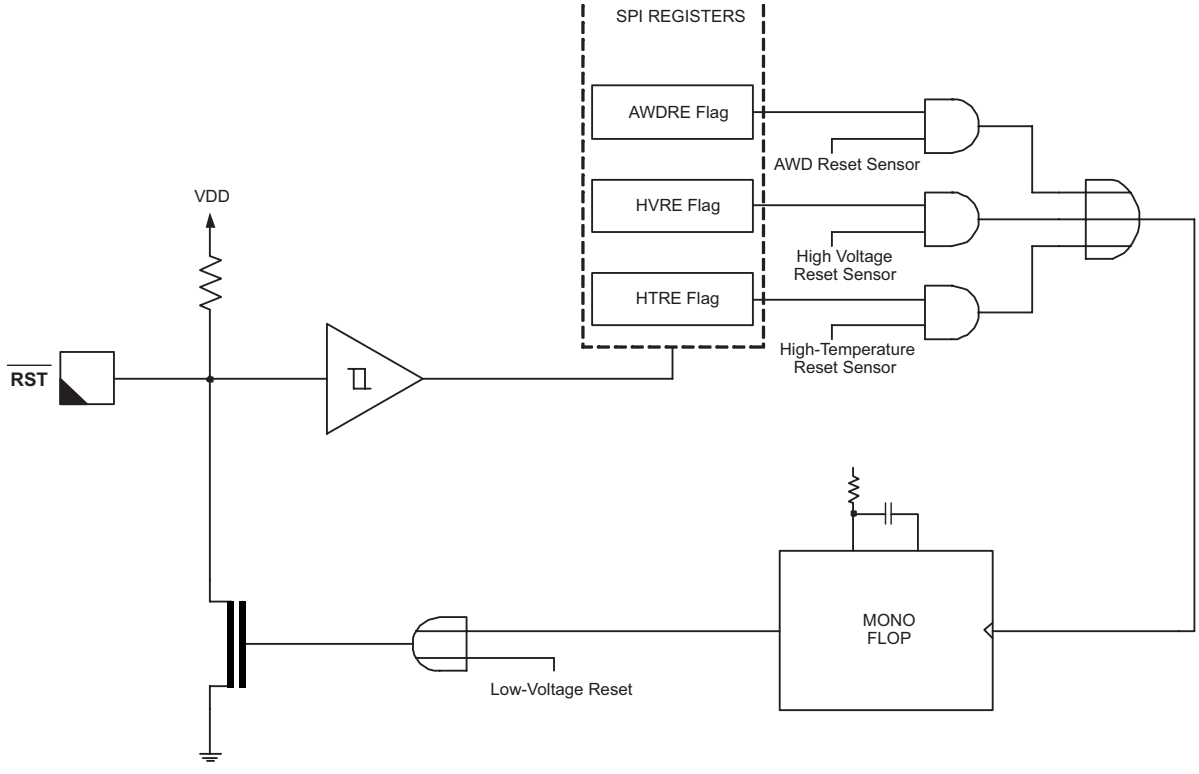


Figure 10. Internal Reset Routing

Internal Sources

Autonomous Watchdog

AWD modules generates RESET because of time-out (watchdog function).

High-Temperature Reset

To prevent a damage of the device, a RESET will be initiate if the temperature rises above a certain value. The reset is maskable with bit HTRE in the Reset Mask Register. After a reset the high-temperature reset is disabled.

Low-Voltage Reset

The LVR is related to the internal VDD. In case the voltage falls below a certain threshold, it will pull down the RESET terminal.

High-Voltage Reset

The HVR is related to the external V_{SUP} voltage. In case the voltage is above a certain threshold, it will pull down the RESET terminal. The reset is maskable with bit HVRE in the Reset Mask Register. After a reset the high-voltage reset is disabled.

External Sources

Reset Terminal

The microcontroller has the capability of resetting the SmartMOS device by pulling down the RESET terminal.

Reset Mask Register (RMR)

Register Name and Address: RMR - $06

	Bit7	6	5	4	3	2	1	Bit0
Read	TTEST	0	0	0	0	0	HVRE	HTRE
Write								
Reset	0	0	0	0	0	0	0	0

HVRE—High-Voltage Reset Enable Bit

This read/write bit enables resets on high-voltage conditions. Reset clears the HVRE bit.

1 = High-voltage reset enabled.

0 = High-voltage reset disabled.

HTRE—High-Temperature Reset Enable Bit

This read/write bit enables resets on high-temperature conditions. Reset clears the HTRE bit.

- 1 = High-temperature reset enabled.
- 0 = High-temperature reset disabled.

TTEST—High-Temperature Reset Test

This read/write bit is for test purpose only. It decrease the overtemperature shutdown limit for final test. Reset clears the HTRE bit.

- 1 = Low-temperature threshold enabled.
- 0 = High-temperature threshold disabled.

Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) creates the communication link between the microcontroller and the 908E625.

The interface consists of four terminals (see Figure 11):

- MOSI—Master-Out Slave-In (Internal Pull-Down)
- MISO—Master-In Slave-Out (Internal Pull-Down)
- SPSCK—Serial Clock
- $\overline{SS}$—Slave Select (Internal Pull-Up)

A complete data transfer via the SPI consist of 2 bytes. The master sends address and data, the slave system status, and data of the selected address.

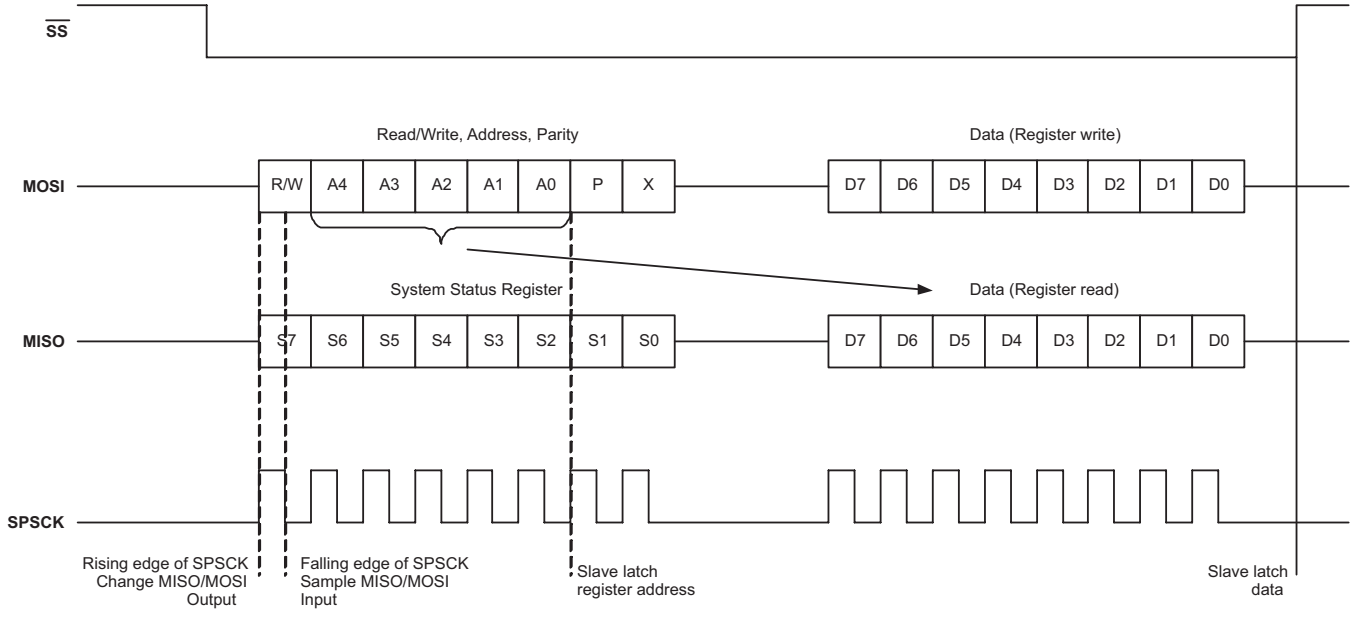


Figure 11. Principle SPI Protocol

During the inactive phase of $\overline{SS}$, the new data transfer will be prepared. The falling edge on the $\overline{SS}$ line indicates the start of a new data transfer and puts MISO in the low impedance mode. The first valid data are moved to MISO with the rising edge of SPSCK.

The MISO output will change data on a rising edge of SPSCK. The MOSI input will be sampled on a falling edge of SPSCK. The data transfer is only valid if exactly 16 sample clock edges are present in the active phase of $\overline{SS}$.

After a write operation, the transmitted data will be latched into the register by the rising edge of $\overline{SS}$.

Register read data is internally latched into the SPI at the time when the parity bit is transferred.

$\overline{SS}$ high will force MISO to high impedance.

Master Address Byte

A4–A0

Includes the address of the desired register.

R/$\overline{W}$

Includes the information if it is a read or a write operation.

- If R/$\overline{W}$ = 1, the second byte of master contains no valid information, slave just transmits back register data.
- If R/$\overline{W}$ = 0, the master sends data to be written in the second byte, slave sends concurrently contents of selected register prior to write operation, write data is latched in the SmartMOS register on rising edge of $\overline{SS}$.

Parity P

Completes the total number of 1 bits of (R/$\overline{W}$,A[4:0]) to an even number; e.g., (R/$\overline{W}$,A[4:0]) = 100001 -> P0 = 0.

The parity bit is only evaluated during a write operation.

Bit X

Not used.

Master Data Byte

This byte includes data to be written or no valid data during a read operation.

Slave Status Byte

This byte includes always the contents of the sYstem Status Register ($0c) independent if it is a write or read operation or which register was selected.

Slave Data Byte

This byte includes the contents of selected register, during write operation in includes the register content prior to write operation.

SPI Register Overview

Table 1 summarizes the SPI Register addresses and the bit names of each register.

Table 1. List of Registers

Addr	Register Name	R/W	Bit							
			7	6	5	4	3	2	1	0
$01	H-Bridge Output (HBOUT)	R	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
		W								
$02	H-Bridge Control (HBCTL)	R	OFC_EN	CSA	0	0	0	CLS2	CLS1	CLS0
		W								
$03	System Control (SYSCTL)	R	PSON	SRS1	SRS0	0	0	0	0	0
		W								GS
$04	Interrupt Mask (IMR)	R	0	PHIE	ISOIE	HTIE	LVIE	HVIE	OCIE	0
		W								
$05	Interrupt Flag (IFR)	R	0	PHF	ISOF	HTF	LVF	HVF	OCF	0
		W								
$06	Reset Mask (RMR)	R	TTEST	0	0	0	0	0	HVRE	HTRE
		W								
$07	A/D Output (ADOUT)	R	0	0	0	0	SS3	SS2	SS1	SS0
		W								
$08	Hall-Effect Sensor Input Terminal Control (HACTL)	R	0	0	0	0	0	H3EN	H2EN	H1EN
		W								
$09	Hall-Effect Sensor Input Terminal Status (HASTAT)	R	0	0	0	0	0	H3F	H2F	H1F
		W								
$0a	AWD Control (AWDCTL)	R	0	0	0	AWDRE	AWDIE	AWDCC	AWDF	AWDR
		W			AWDRST					
$0b	Power Output (POUT)	R	0	0	CSSEL1	CSSEL0	CSEN1	CSEN0	HVDDON	HS_ON
		W								
$0c	System Status Register (SYSSTAT)	R	HP_OCF	SICL	HVDD_OCF	HS_OCF	LVF	HVF	HB_OCF	HTF
		W								

Analog Die I/Os

LIN Physical Layer

This I/O provides a physical layer for full-/half duplex communication in automotive applications. The physical layer is designed to meet the LIN physical layer specification.

Single-Wire Interface (SIO)

The SIO terminal is the LIN interface, which is suited for automotive bus systems.

The driver is a low-side transistor with a internal current limitation and a thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. The fall time from dominate to recessive and the rise time from recessive to dominate is controlled. The symmetry between both slew rate controls is guaranteed.

The terminal offers high susceptibility immunity level from external disturbance in order to guarantee communication during external disturbance.

The LIN transmitter circuitry will be enabled by setting bit PSON in the System Control Register. If the transmitter work in the current limitation region, the SICL bit in the System Status Register is set. The software should switch off the transmitter owing to high power dissipation.

TxD Terminal

This terminal is the MCU interface to control the state of the LIN transmitter. When TxD is low, LIN output is low. When TxD is high, LIN output transistor is turned off. The terminal has an internal pull-up current source in order to set the bus in recessive state in case the microcontroller could not control it during system power-up or power-down for instance.

RxD Terminal

This terminal is the MCU interface, which reports the state of the LIN bus voltage. LIN high is reported by a high level on RxD, LIN low reported by a low voltage on RxD.

STOP Mode/Wake-Up Feature

During STOP mode operation the transmitter of the physical layer is disabled. The receiver terminal is still active to be able to detect wake-up events on the busline.

If the SIO interrupt is enabled (SIOIE bit in the Interrupt Mask Register is set), a falling edge on the SIO line will cause an interrupt. This interrupt will switch on the main voltage regulator and generate a system wake-up.

Analog Multiplexer/ADOUT Terminal

The ADOUT terminal is the analog output interface to the ADC of the MCU. To be able to have different sources for the MCU, an analog multiplexer is integrated. This multiplexer has nine different sources.

Current Recopy

The multiplexer is connected to the four low side current sense circuits of the half-bridges. This sense circuits offers a voltage proportional to the current through the low side transistor. The resolution is selectable between 5.0 V/2.5 A or 5.0 V/500 mA. (Refer to Half-Bridge Current Recopy on page 30.)

Analog Inputs

Each analog input is directly connected to the analog multiplexer. It offers the possibility to read analog values from the periphery.

Temperature Sensor

The MC33980 includes a on-chip temperature sensor. This sensor offers a voltage which is proportional to the actual chip junction temperature.

V_{SUP} Prescaler

The V_{SUP} prescaler offers a possibility to read or measure the external supply voltage. The output of this voltage is V_{SUP}/ $RATIO_{VSUP}$.

The different sources can be selected with the ADOUT Register.

Analog Multiplexer Configuration Register (ADOUT)

Register Name and Address: ADOUT - $07

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	SS3	SS2	SS1	SS0
Write								
Reset	0	0	0	0	0	0	0	0

SS3, SS2, SS1, and SS0—A/D Input Select Bits

These read/write bits select the input to the ADC in the microcontroller according to Table 2, page 23. Reset clears SS3, SS2, SS1, and SS0 bits.

Table 2. Analog Multiplexer Configuration Register

SS3	SS2	SS1	SS0	Channel
0	0	0	0	Current Recopy HB1
0	0	0	1	Current Recopy HB2
0	0	1	0	Current Recopy HB3
0	0	1	1	Current Recopy HB4
0	1	0	0	V_{SUP} Prescaler
0	1	0	1	Temperature
0	1	1	0	Not Used
0	1	1	1	PA1 Terminal
1	0	0	0	Not Used
1	0	0	1	Not Used
1	0	1	0	Not Used
1	0	1	1	Not Used
1	1	0	0	Not Used
1	1	0	1	Not Used
1	1	1	0	Not Used
1	1	1	1	Not Used

The Port A provides one analog input used for reading switches or as analog inputs for potentiometers, NTC, etc.

The PA1 is an input terminal for reading analog values. The terminal is internally connected to the analog multiplexer. In addition the terminal has a switchable current source (see Figure 12).

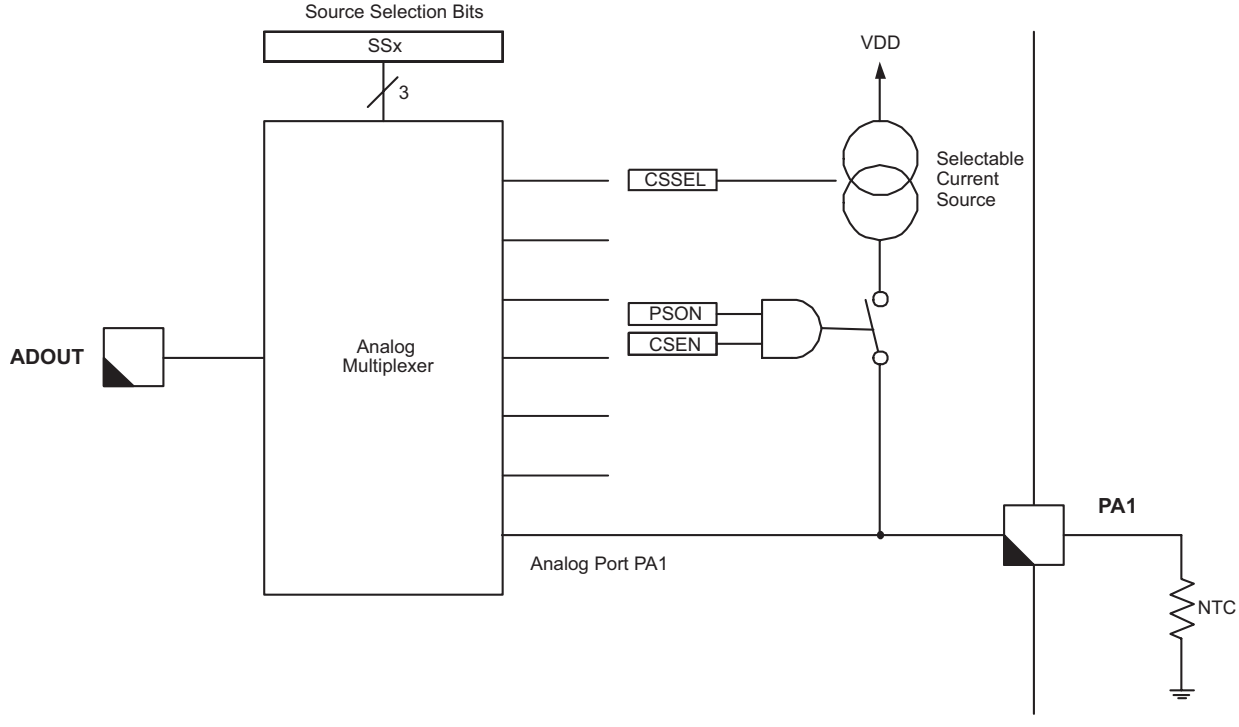


Figure 12. Analog Input + Multiplexer

PORT A Current Source

PA1 provides a switchable current source, to be able to read in switches, NTC, etc., without the need of an additional supply line for the sensor. With this feature it is possible to read multiple switches on one input. The overall enable of this feature is done by setting the PSON bit in the System Control Register. The switch on of each individual current source is done by the CSEN bit in the Power Output Register. The value of the current source is selected by CSSELx.

With the CSSELx bits, four different current source values can be selected: 60 μA, 180 μA, 360 μA, and 600 μA.

This function ceases during STOP mode operation.

Power Output Register (POUT)

Register Name and Address: IMR - $0b

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	CSSEL 1	CSSEL 0	CSEN	0 (Note 15)	HVDDON	HS_ON
Write								
Reset	0	0	0	0	0	0	0	0

Notes

15. This bit must always be set to “0”.

HVDDON—HVDD On Bit

This read/write bit enables HVDD output. Reset clears HVDDON bit.

- 1 = HVDD enabled.
- 0 = HVDD disabled.

HS_ON—Lamp Driver On Bit

This read/write bit enables the Lamp driver. Reset clears HS_ON bit.

- 1 = Lamp driver enabled.
- 0 = Lamp driver disabled.

CSEN—Current Source Enable Bits

This read/write bit enables the current source for PA0–PA2. Reset clears CSENx bits (refer to Table 3).

Table 3. PA1 Current Source Enable Bit

CSEN	Current Source Enable
0	Current Source Off
1	PA1 Current Source Enabled

CSSEL0–CSSEL1—Current Source Select Bits

This read/write bit selects the current source values. Reset clears CSSEL0–CSSEL1 bits (refer to Table 4).

Table 4. PA1 Current Source Level Selection Bits

CSSEL1	CSSEL0	Current Source Enable (typ.)
0	0	70 μA
0	1	210 μA
1	0	420 μA
1	1	700 μA

Hall-Effect Sensor Input Terminals

Function

The Hall-effect sensor input terminals provide three inputs for two-terminal Hall-effect sensors to be able to detect stall and position or to read Hall-effect sensor contact switches. The Hall-effect sensor input terminals are not influenced by the PSON bit in the System Control Register.

Each terminal of the Hall-effect sensor can be enabled by setting the HxEN bit in the Hall-Effect Sensor Input Terminal Control Register. If the terminals are enabled, the Hall-effect sensors are supplied with V_{SUP} voltage and the sense circuitry is working. This sense circuitry monitors the current to VSS. The result of this sense operation is given by the HxF flags in the Hall-Effect Sensor Input Terminal Status Register.

The flag is high if the sensed current is higher than I_{REC}. To prevent noise on this flag, a hysteresis is implemented on these terminals.

After switching on the Hall-effect sensor input terminals (HxEN = 1), the Hall-effect sensors need some time to stabilize the output. In RUN mode the software must take care to wait a few microseconds before sensing the hallflags.

The Hall-effect sensor input terminal is working in an dynamic output voltage range from V_{SUP} to 1.5 V. Below 1.5 V the hallflags are not functional anymore. In case the output voltage is below a certain threshold, the Hall-Effect Sensor Input Terminal Overcurrent Flag (HP_OCF) in the System Status Register is set.

Figures 13 through 15, pp. 25–26, show the connections to the Hall-effect input sensors.

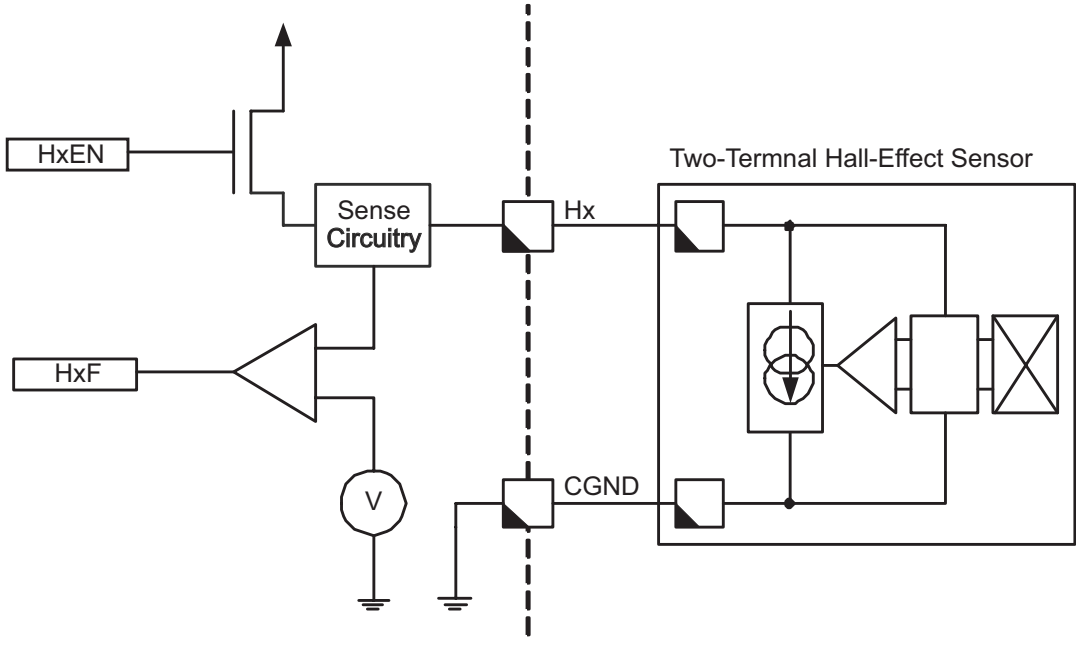


Figure 13. Hall-Effect Sensor Input Terminal Connected to Two-Terminal Hall-Effect Sensor

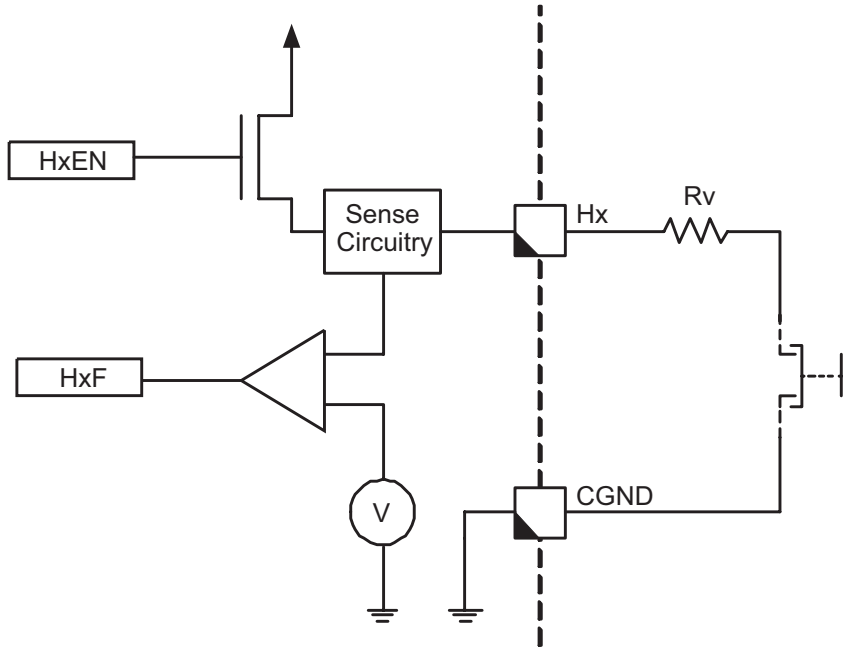


Figure 14. Hall-Effect Sensor Input Terminal Connected to Local Switch

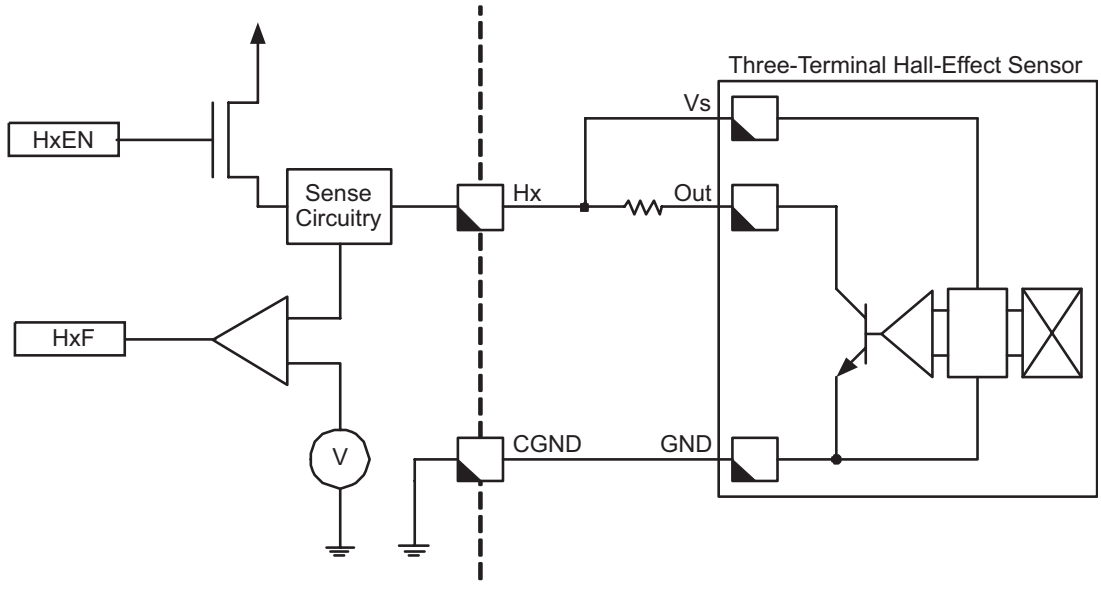


Figure 15. Hall-Effect Sensor Input Terminal Connected to Three-Terminal Hall-Effect Sensor

Interrupts

The Hall-effect sensor input terminal is interrupt capable. How and when an interrupt occurs is dependent on the actual operating mode.

RUN Mode

In RUN mode the Hall-effect sensor input terminal interrupt flag (PHF) will be set if a state change on the hallflags (HxF) is detected. The interrupt is maskable with the PHIE bit in the Interrupt Mask Register. Before enabling the interrupt, the flag should be cleared in order to prevent a wrong interrupt.

STOP Mode

In STOP mode the Hall-effect sensor input terminals are disabled independent of the state of the HxEN flags.

Cyclic Wake-Up

The Hall-effect sensor inputs can be used to wake up the system. This wake-up function will be provided by the cyclic check wake-up feature of the AWD (autonomous watchdog).

If the cyclic check wake-up feature is enabled (AWDCC bit is set), the AWD will switch on the enabled Hall-effect sensor terminals periodically. To be sure that the Hall-effect sensor current after switch on is stabilized, the inputs are sensed after ~32 μs. If a “1” is detected ($I_{Hall\ sensor} > I_{REC}$) and the interrupt mask bit PHIE is set, an interrupt will be performed. This will wake up the MCU and start the main voltage regulator.

The wake-up function via this input is available when all three conditions exist:

- The 2-terminal Hall-effect sensor input is enabled (HxEN = 1).
- The cyclic wake-up of the AWD is enabled (AWDCC = 1) (see Figure 16, page 27).
- The Hall-effect sensor input terminal interrupt is enabled (PHIE = 1).

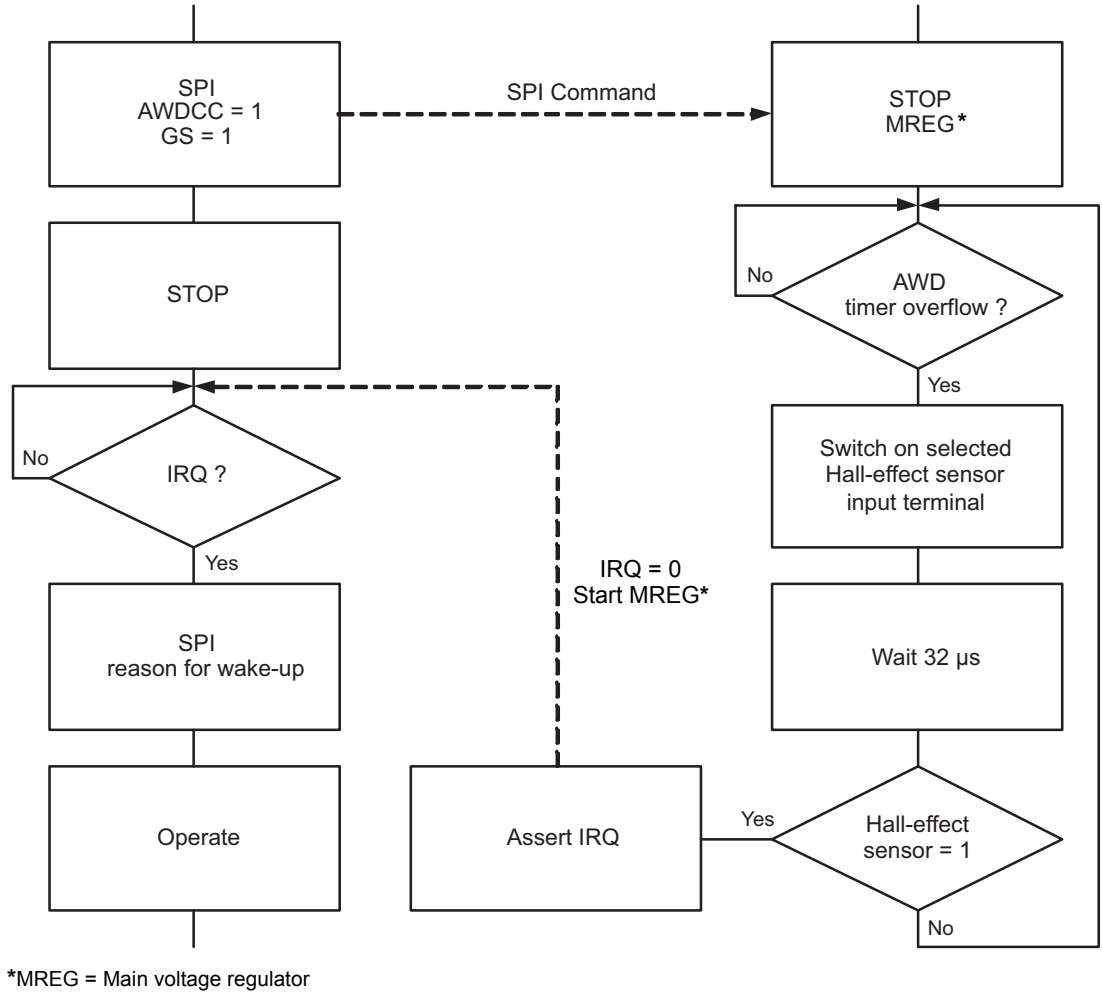


Figure 16. Hall-Effect Sensor Input Terminal Cyclic Check Wake-Up Feature

Hall-Effect Sensor Input Terminal Control Register (HACTL)

Register Name and Address: HACTL - $08

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	0	H3EN	H2EN	H1EN
Write								
Reset	0	0	0	0	0	0	0	0

H3EN, H2EN, and H1EN—Hall-Effect Sensor Input Terminal Enable Bits

These read/write bits enable the Hall-effect sensor input terminals. Reset clears H3EN, H2EN, and H1EN bit.

- 1 = Hall-effect sensor input terminal Hx is switched on and sensed.
- 0 = Hall-effect sensor input terminal Hx disabled.

Hall-Effect Sensor Input Terminal Status Register (HASTAT)

Register Name and Address: HASTAT - $09

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	0	H3F	H2F	H1F
Write								
Reset	0	0	0	0	0	0	0	0

H3F, H2F, and H1F—Hall-Effect Sensor Input Terminal Flag Bits

This read/write flag reflects the input Hx while the Hall-effect sensor input terminal Hx is enabled (HxEN = 1). Reset clears the HxF bit.

- 1 = Hall-effect sensor input terminal current above threshold.
- 0 = Hall-effect sensor input terminal current below threshold.

Half-Bridges

The outputs provide four low resistive half-bridge output stages. The half-bridges can be used in H-Bridge, high-side, or low-side configurations.

Reset clears all bits in the H-Bridge Output Register owing to the fact that all half-bridge outputs are switched off.

The output features:

- Short circuit protection on high-side and low-side FETs (low side just via VDS monitoring).
- Current recopy feature (low side).
- Overtemperature protection.
- Overvoltage and undervoltage protection.
- Current limitation feature (low side).

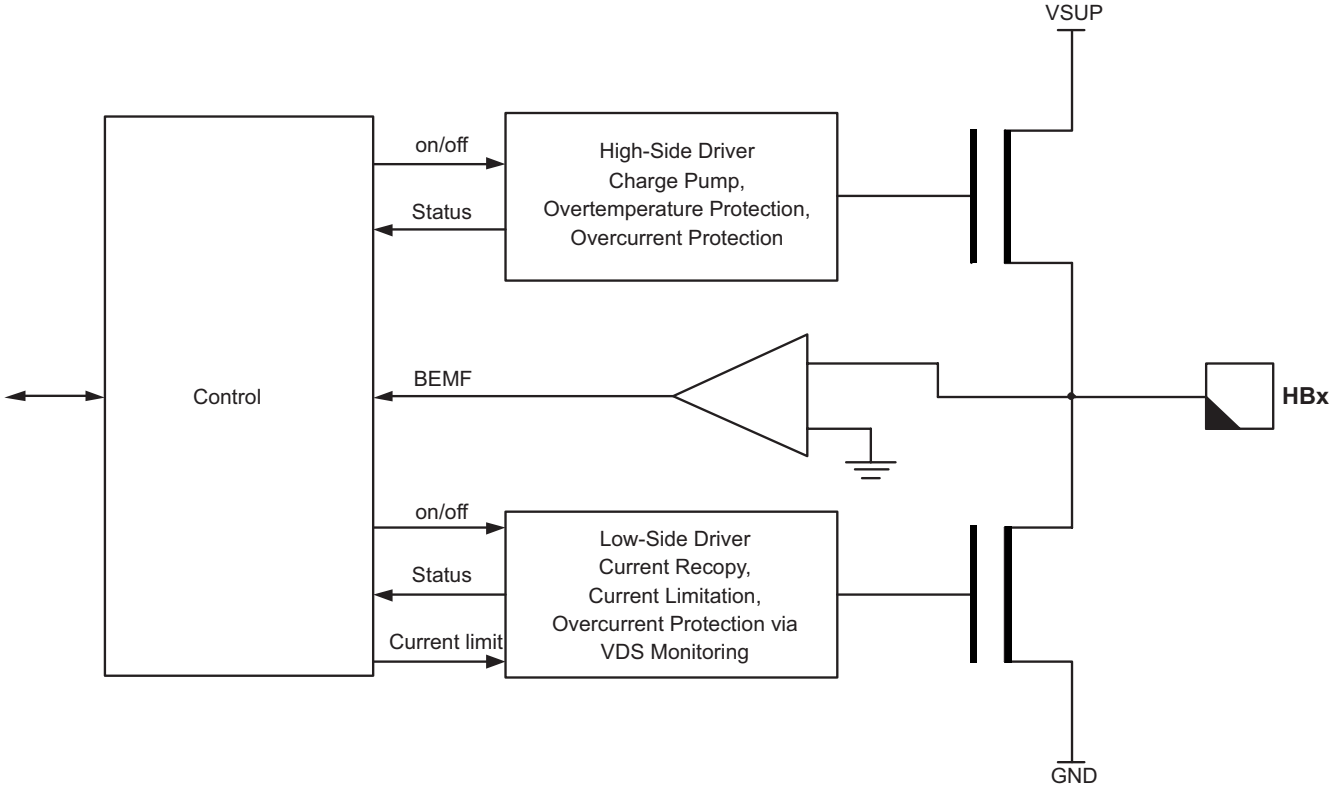


Figure 17. Half-Bridge Push-Pull Output Driver

Half-Bridge Control

Each output FET can be controlled individually. The general enable of the circuitry is done by setting PSON in the System Control Register. HBx_L and HBx_H form one half-bridge. It is not possible to switch on both FETs in one half-bridge at the same time.

In case both bits are set, the high-side transistor has a higher priority. To avoid cross conduction while switching the output transistors, a break before make circuit exists. The switch on of the high-side transistor is inhibited as long as the potential between gate and VSS is not below a certain threshold. The switch on of the low-side transistor is blocked as long as the potential between gate and source of the high-side transistor did not fall below a certain threshold.

Half-Bridge Output Register (HBOUT)

Register Name and Address: HBOUT - $01

	Bit7	6	5	4	3	2	1	Bit0
Read Write	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB!_H	HB1_L
Reset	0	0	0	0	0	0	0	0

HBx_L—Low-Side On/Off Bits

These read/write bits turn on the low-side FETs. Reset clears the HBx_L bits.

- 1 = Low side is turned on for Output x.
- 0 = Low side is turned off for Output x.

HBx_H—High-Side On/Off Bits

These read/write bits turn on the high-side FETs. Reset clears the HBx_H bits.

1 = High-side driver turned on for Output x.

0 = High-side driver turned off for Output x.

Half-Bridge Current Limitation

Each low-side transistor offers a current limit or constant current feature. This features is realized by a pulse width modulation on the low-side transistors. The pulse width modulation on the outputs is controlled by the FGEN input and the load characteristic. The FGEN input provides the PWM frequency, whereas the duty cycle is controlled by the load characteristics.

The maximum input frequency for the FGEN and the PWM is ~25 kHz.

Functionality

Each low-side transistor will switch off if a current above the selected current limit was detected. The 908E625 offers five different current limits: 60 mA, 250 mA, 350 mA, 500 mA, and 700 mA.

The output transistor will switch on again if a rising edge on the FGEN input was detected (see Figure 18).

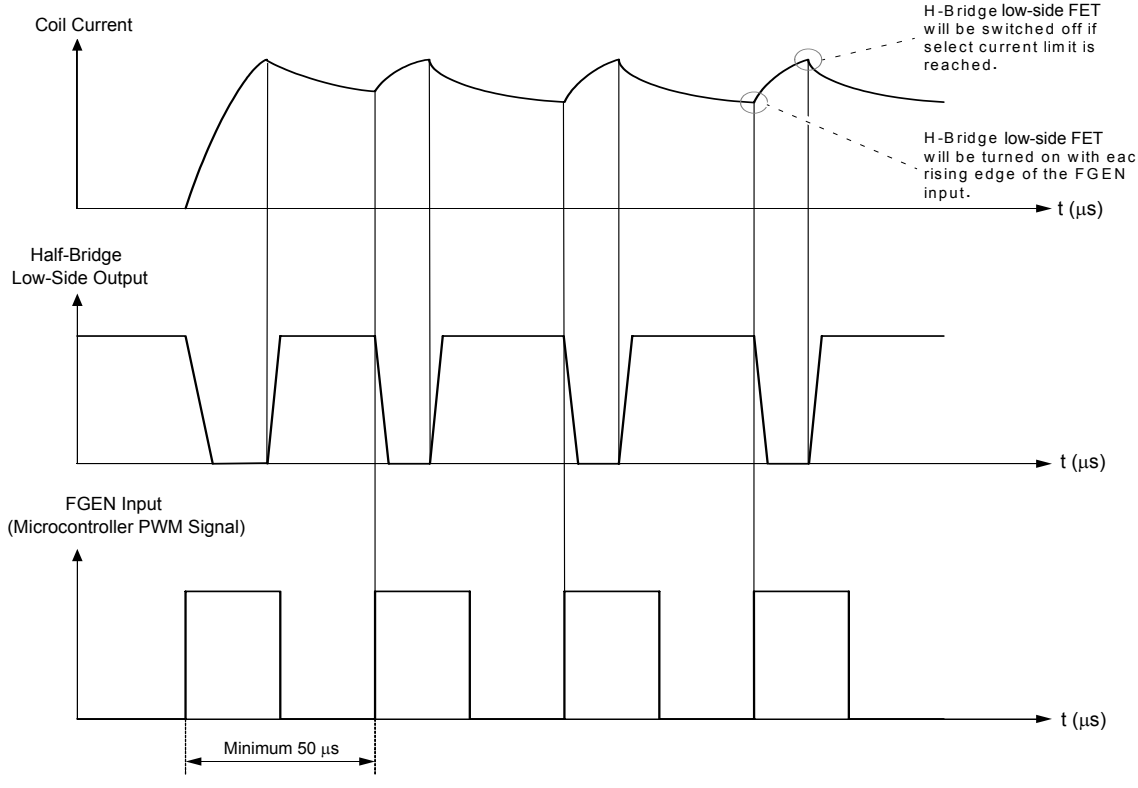


Figure 18. Current Limitation

Offset Chopping

If Bit OFC_EN in the H-Bridge Control Register is set, HB3 and HB4 will switch on the low-side-FETs after detecting a falling edge on the FGEN input. In stepper motor applications this feature allows the reduction of EMI due to a reduction of the di/dt (see Figure 19).

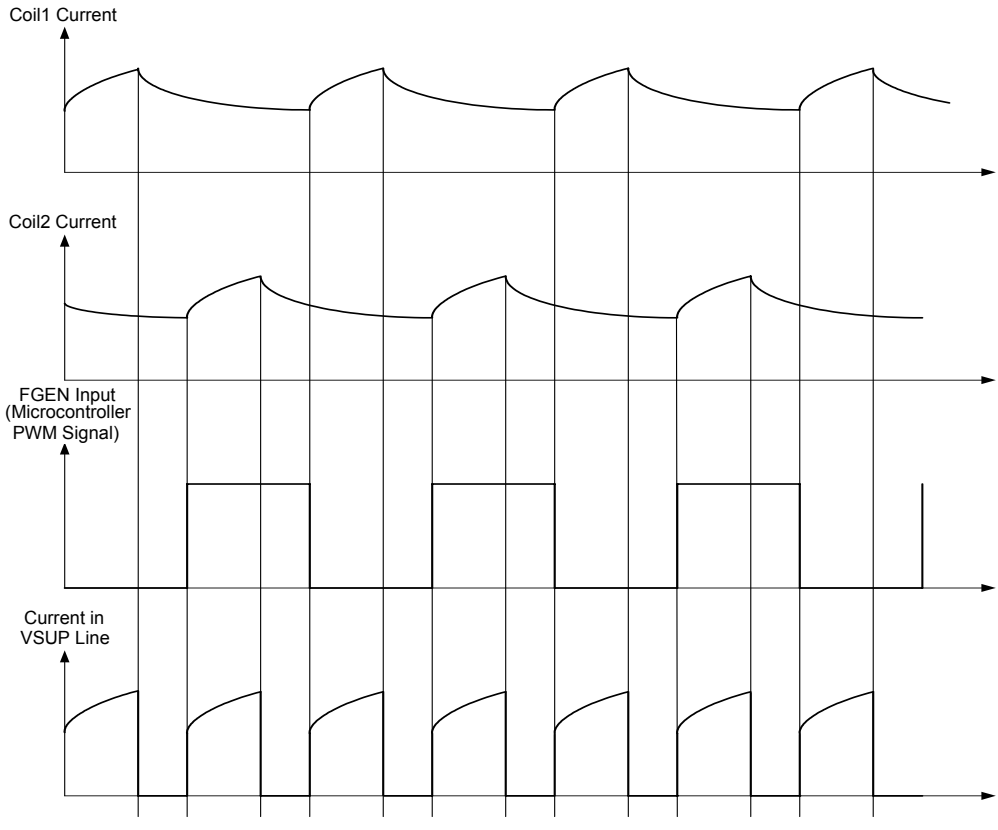


Figure 19. Offset Chopping for Stepper Motor Control

Half-Bridge Current Recopy

Each low-side FET has an additional sense output to allow a current recopy feature. This sense source is internally connected to a shunt resistor. The drop voltage is amplified and switched to the Analog Multiplexer.

The factor for the Current Sense amplification can be selected via bit CSA in the System Control Register.

- CSA = 1: Low resolution selected (500 mA measurement range).
- CSA = 0: High resolution selected (2.5 A measurement range).

Half-Bridge BEMF Generation

The BEMF output is set to one if in any half-bridge a recirculation current is detected. This recirculation current will flow via the two free wheel diodes of the power transistors. The BEMF circuitry will detect that and generate a high on the BEMF output as long as a recirculation current is detected. This signal provides a flexible and reliable detection of stall in stepper motor applications. For this the BEMF circuitry will take advantage of the instability of the electrical and mechanical behavior of a stepper motor when blocked. In addition the signal can be used for open load detection (absence of this signal) (see Figure 20, page 31).

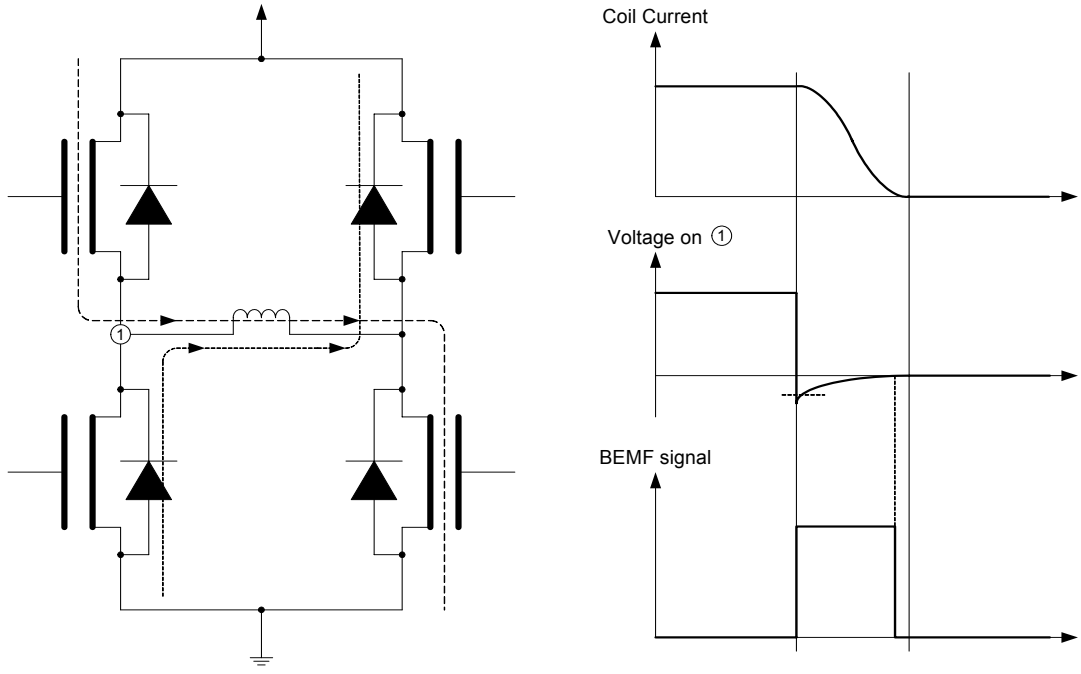


Figure 20. BEMF Signal Generation

Half-Bridge Overtemperature Protection

The outputs provide an overtemperature pre-warning with the HTF in the Interrupt Status Register. In order to protected the outputs against overtemperature, the High-Temperature Reset has to be enabled. If this value is reached, the part will generate a reset and disable all power outputs.

Half-Bridge Overcurrent Protection

The half-bridges are protected against short to GND, VSUP, and load shorts. The high-side protection is done by a real current measurement, the low-side FET just by monitoring VDS voltage.

In case a overcurrent on the high side is detected, the high-side FETs on all HB high-side FETs are switched off automatically. In case an overcurrent on the low side is detected all HB low-side FETs will be switched off automatically. In both cases the overcurrent status flag HB_OCF in the System Status Register is set.

The overcurrent status flag is cleared (and the outputs re-enabled) by writing a logic [1] to the HB_OCF flag in the System Status Register or by RESET.

Half-Bridge Overvoltage/Undervoltage

The half-bridge outputs are protected against undervoltage and overvoltage conditions. This protection is done by the low- and high-voltage interrupt circuitry. If one of these flags (LVF, HVF) is set, the outputs are automatically disabled.

The overvoltage/undervoltage status flags are cleared (and the outputs re-enabled) by writing a logic [1] to the LVF/HVF flags in the Interrupt Flag Register or by RESET. Clearing this flag is useless as long as a high- or low-voltage condition is present.

Half-Bridge Control Register (HBCTL)

Register Name and Address: HBCTL - $02

	Bit7	6	5	4	3	2	1	Bit0
Read	OFC_EN	CSA	0	0	0	CLS2	CLS1	CLS0
Write								
Reset	0	0	0	0	0	0	0	0

OFC_EN—H-Bridge Offset Chopping Enable Bit

This read/write bit enables offset chopping. Reset clears the OFC_EN bit.

- 1 = Offset chopping enabled.
- 0 = Offset chopping disabled.

CSA—H-Bridges Current Sense Amplification Select Bit

This read/write bit selects the current sense amplification of the H-Bridges. Reset clears the CSA bit.

- 1 = Current sense amplification set for measuring 0.5 A.
- 0 = Current sense amplification set for measuring 2.5 A.

CLS2, CLS1, and CLS0—H-Bridge Current Limitation Selection Bits

These read/write bits select the current limitation value according to Table 5. Reset clears the CLS2, CLS1, and CLS0 bits.

Table 5. H-Bridge Current Limitation Value Selection Bits

CLS2	CLS1	CLS0	Current Limit
0	0	0	No Limit
0	0	1	No Limit
0	1	0	No Limit
0	1	1	55 mA (typ)
1	0	0	275 mA (typ)
1	0	1	370 mA (typ)
1	1	0	550 mA (typ)
1	1	1	740 mA (typ)

High-Side Driver

The high-side output is a low resistive high-side switch, targeted for driving lamps. The high side is protected against overtemperature. To limit the high inrush current of bulbs the overcurrent protection circuitry will be used to limit the current. The output is enable with bit PSON in the System Control Register and can be switched on/off with bit HS_ON in the Power Output Register. See Figure 21 for high-side switch circuitry and connection to external lamp.

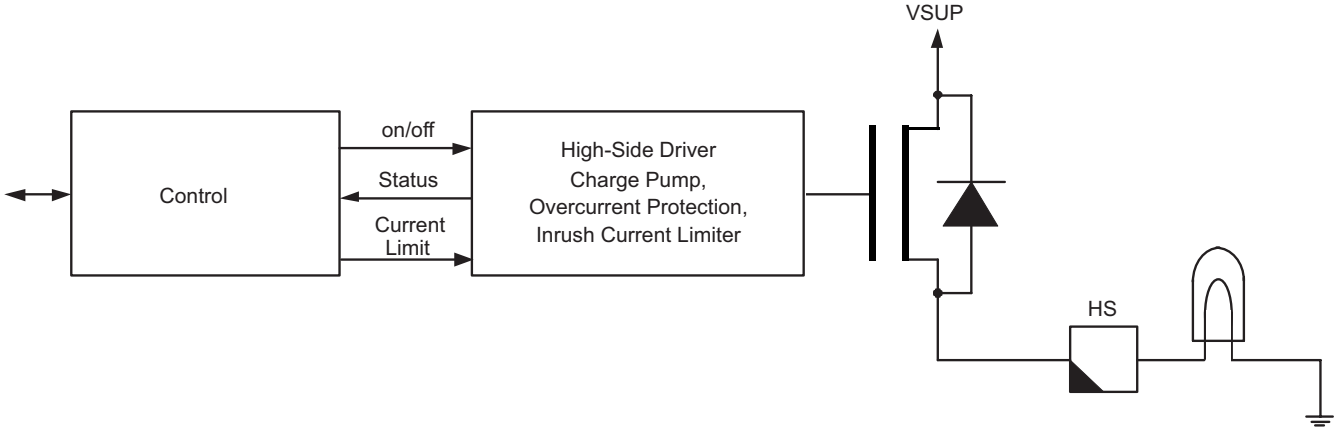


Figure 21. High-Side Circuitry

High-Side Overvoltage/Undervoltage Protection

The output is protected against undervoltage/overvoltage conditions. This protection is done by the low- and high-voltage interrupt circuitry. If one of these flags (LVF, HVF) is set, the output is disabled.

The overvoltage/undervoltage status flags are cleared (and the output re-enabled) by writing a logic [1] to the LVF/HVF flags in the Interrupt Flag Register or by RESET. Clearing this flag is useless as long as a high- or low-voltage condition is present.

High-Side Overtemperature Protection

The high-side output provides an overtemperature pre-warning with the HTF in the Interrupt Status Register. In order to protected the output against overtemperature the High-Temperature Reset has to be enabled. If this value is reached, the part will generate a reset and disable all power outputs.

High-Side Overcurrent Protection

The high-side output is protected against overcurrent. In case the overcurrent limit is or was reached, the output will be automatically switched off and the overcurrent flag is set.

Due to the high inrush current of bulbs, a special feature was implemented to avoid a overcurrent shutdown during this inrush current. If an PWM frequency will be supplied to the FGEN output during the switch on of a bulb the inrush current will be limited to the overcurrent shutdown limit. This means if the current reaches the overcurrent shutdown, the high side will be switched off, but each rising edge on the FGEN input will enable the driver again.

In order to be able to distinguish between a shutdown due to an inrush current or a real shutdown, the software has to check if the overcurrent status flag (HS_OCF) in the System Status Register is set beyond a certain period of time.

The overcurrent status flag is cleared by writing a logic [1] to the HS_OCF in the System Status Register (see Figure 22).

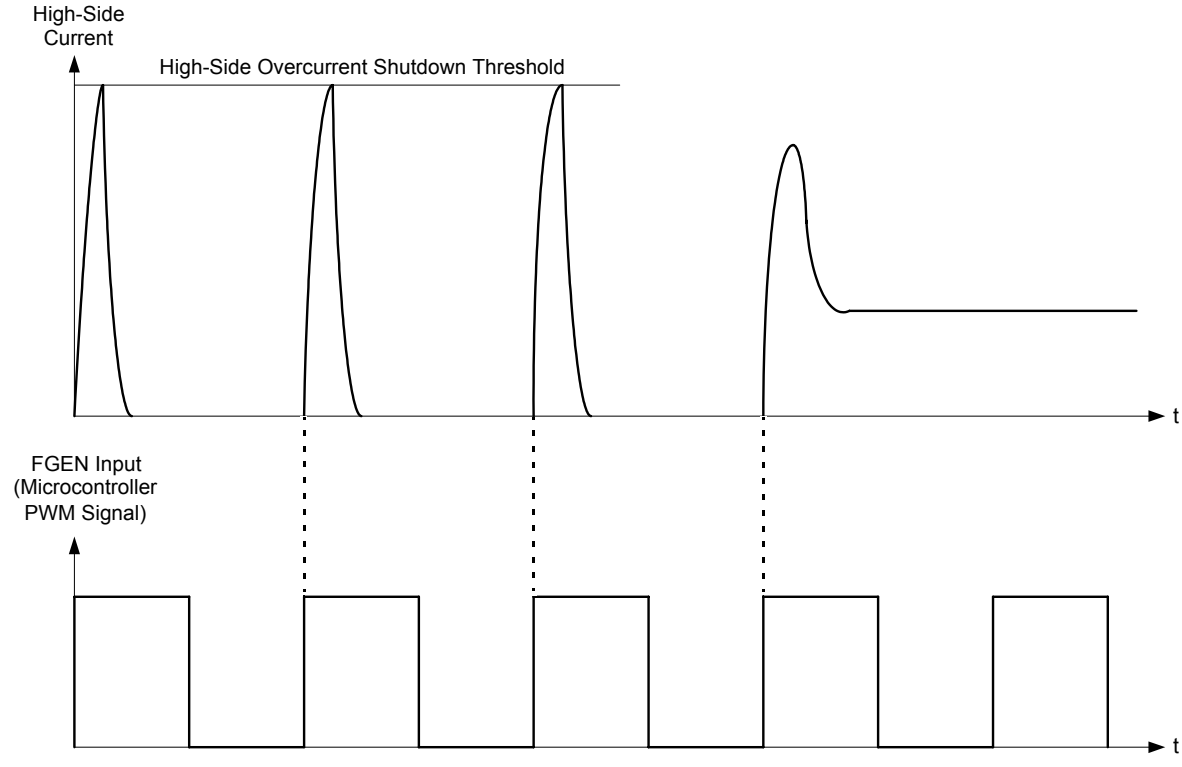


Figure 22. Inrush Current Limit on High-Side Output

Switchable VDD Outputs

The HVDD terminal is a switchable VDD output terminal. It can be used for driving external circuitry which requires a VDD voltage. The output is enable with bit PSON in the System Control Register and can be switched on/off with bit HVDD_ON in the Power Output Register. Low- or high-voltage conditions (LVI/HVI) will have no influence on this circuitry.

HVDD Overtemperature Protection

The overtemperature protection is enabled if the high-temperature reset is enabled.

HVDD Overcurrent Protection

The HVDD output is protected against overcurrent. In case the overcurrent limit is or was reached, the output will be automatically switched off and the HVDD overcurrent flag in the System Status Register is set.

System Control Register (SYSCTL)

Register Name and Address: SYSCTL - $03

	Bit7	6	5	4	3	2	1	Bit0
Read	PSON	SRS1	SRS0	0	0	0	0	0
Write								GS
Reset	0	0	0	0	0	0	0	0

PSON—Power Stages On Bit

This read/write bit enables the power stages (half-bridges, high side, LIN transmitter, Port A Current Sources, and HVDD output). Reset clears the PSON bit.

- 1 = Power stages enabled.
- 0 = Power stages disabled.

SRS0–SRS1—LIN Slew Rate Selection Bits

This read/write bits enables the user to select the appropriate LIN slew rate for different baud rate configurations as shown in Table 6.

Table 6. LIN Slew Rate Selection Bits

SRS1	SRS0	Current Source Enable
0	0	Initial SR
0	1	0.5 x initial SR
1	0	16 x initial SR
1	0	8 x initial SR

GS—Go to STOP Mode Bit

This read/write bit instructs the chip to power down and go into STOP mode. Reset or CPU interrupt requests clears the GS bit.

- 1 = Power down and go to STOP mode.
- 0 = Not in STOP mode.

System Control Register (SYSSTAT)

Register Name and Address: SYSSTAT - $0c

	Bit7	6	5	4	3	2	1	Bit0
Read	HP_ OCF	SICL	HVDD _OCF	HS_ OCF	LVF	HVF	HB_ OCF	HTF
Write								
Reset	0	0	0	0	0	0	0	0

HP_OCF—Hall-Effect Sensor Input Terminal Overcurrent Flag Bit

This read/write flag is set on overcurrent condition at one of the Hall-effect sensor input terminals. Clear HP_OCF and enable the output by writing a logic [1] to the HP_OCF Flag. Reset clears the HP_OCF bit. Writing a logic [0] to HP_OCF has no effect.

- 1 = Overcurrent condition on Hall-effect sensor input terminal has occurred.
- 0 = No overcurrent condition on Hall-effect sensor input terminal has occurred.

SICL — Serial Input Current Limitation Bit

This read only bit is set if the ISO9141 transmitter operates in current limitation region. Due to excessive power dissipation in the transmitter, software is advised to turn the transmitter off immediately.

- 1 = Transmitter operating in current limitation region.
- 0 = Transmitter not operating in current limitation region.

HVDD_OCF—HVDD Output Overcurrent Flag Bit

This read/write flag is set on overcurrent condition at HVDD terminal. Clear HVDD_OCF and enable the output by writing a logic [1] to the HVDD_OCF Flag. Reset clears the HVDD_OCF bit. Writing a logic [0] to HVDD_OCF has no effect.

- 1 = Overcurrent condition on VDD has occurred.
- 0 = No overcurrent condition on VDD has occurred.

HS_OCF—High-Side Overcurrent Flag Bit

This read/write flag is set on overcurrent condition at high-side driver. Clear HS_OCF and enable HS Driver by writing a logic [1] to HS_OCF. Reset clears the HS_OCF bit. Writing a logic [0] to HS_OCF has no effect.

- 1 = Overcurrent condition on high-side drivers has occurred.
- 0 = No overcurrent condition on high-side drivers has occurred.

LVF—H-Bridge Low-Voltage Bit

This read only bit is a copy of the LVF bit in the Interrupt Flag Register.

- 1 = Low-voltage condition on H-Bridges.
- 0 = No low-voltage condition on H-Bridges.

HVF—H-Bridge High-Voltage Sensor Bit

This read only bit is a copy of the HVF bit in the Interrupt Flag Register.

- 1 = High-voltage condition on H-Bridges.
- 0 = No high-voltage condition on H-Bridges.

HB_OCF—H-Bridge Overcurrent Flag Bit

This read / write flag is set on overcurrent condition at the H-Bridges. Clear HB_OCF and enable Half-Bridge driver by writing a logic [1] to HB_OCF. Reset clears the HB_OCF bit. Writing a logic [0] to HB_OCF has no effect.

- 1 = Overcurrent condition on H-Bridges has occurred.
- 0 = No overcurrent condition on H-Bridges has occurred.

HTF—Overtemperature Status Bit

This read only bit is a copy of the HTF bit in the Interrupt Flag Register.

- 1 = Overtemperature condition on H-Bridges.
- 0 = No overtemperature condition on H-Bridges.

Autonomous Watchdog (AWD)

The Autonomous Watchdog module comprises three functions:

- Periodic interrupt function
- Watchdog function for the CPU in RUN mode
- Cyclic wake-up function

The AWD is enabled if AWDIE or AWDRE or AWDCC in the AWDCTL Register is set. If these bits are cleared, the AWD oscillator is disabled and the watchdog is switched off.

Periodic Interrupt

The periodic interrupt is available in STOP mode. It will be enabled by setting the AWDIE bit in the AWDCTL Register. If AWDIE is set, the AWD will wake up the system after a fixed period of time. This time period can be selected with bit AWDR in the AWD Control Register.

Watchdog

The watchdog function is only available in RUN mode. On setting the AWDRE bit, the watchdog functionality in RUN mode is activated. Once this function is enabled, it is not possible to disable it via software.

If the timer reaches end value and AWDRE is set, a system reset will be initiated. Operations of the watchdog function are ceased in STOP mode. Normal operation will be continued when the system is back to RUN mode.

To prevent a watchdog reset the watchdog time-out counter has to be reset before it reaches the end value. This is done by a write to the AWDRST bit in the AWDCTL Register.

Cyclic Wake-Up

The cyclic wake-up feature is available in STOP mode. If this feature is enabled, the selected Hall-effect sensor input terminals are switched on and sensed. If a “1” is detected on one of these inputs and the interrupt for the Hall-effect sensors is enabled, a system wake-up will be performed. (Switch on main voltage regulator and assert IRQ to the microcontroller).

Autonomous Watchdog Control Register (AWDCTL)

Register Name and Address: AWDCTL - $0b

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0		AWDRE	AWDIE	AWDCC	AWDF	AWDR
Write			AWDRST					
Reset	0	0	0	0	0	0	0	0

AWDRST—Autonomous Watchdog Reset Bit

This write only bit resets the Autonomous Watchdog time-out period. AWDRST always reads zero. Reset clears AWDRST bit.

- 1 = Reset AWD and restart time-out period.
- 0 = No effect.

AWDRE—Autonomous Watchdog Reset Enable Bit

This read/write bit enables resets on AWD time-outs. RST will only be asserted when the device is in RUN mode. AWDRE is one-time setable after each reset. Reset clears the AWDRE bit.

- 1 = Autonomous watchdog enabled.
- 0 = Autonomous watchdog disabled.

AWDIE—Autonomous Watchdog Interrupt Enable Bit

This read/write bit enables CPU interrupts by the Autonomous Watchdog time-out flag, AWFD. IRQ will only be asserted when the device is in STOP mode. Reset clears the AWDIE bit.

- 1 = CPU interrupt requests from AWDF enabled.
- 0 = CPU interrupt requests from AWDF disabled.

AWDCC—Autonomous Watchdog Cyclic Check

This read/write bit enables the cyclic check of the two-terminal Hall-effect sensor and the analog inputs. Reset clears the AWDCC bit.

- 1 = Cyclic check of the Hall-effect sensor and analog port.
- 0 = No cyclic check of the Hall-effect sensor and analog port.

AWDF—Autonomous Watchdog Time-Out Flag Bit

This read/write flag is set when the Autonomous Watchdog has timed out. Clear AWDF by writing a logic [1] to AWDF. Clearing AWDF also resets the AWD counter and starts a new time-out period. Reset clears the AWDF bit. Writing a logic [0] to AWDF has no effect.

- 1 = AWD has timed out.
- 0 = AWD has not yet timed out.

AWDR—Autonomous Watchdog Rate Bit

This read/write bit select the clock rate of the Autonomous Watchdog. Reset clears the AWDR bit.

- 1 = Fast rate selected (10 ms).
- 0 = Slow rate selected (20 ms).

Voltage Regulator

The 908E625 chip contains a low-power, low-drop voltage regulator to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main regulator and the low-voltage reset circuit.

The VDD regulator accepts a unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD terminal to provide the 5.0 V to the microcontroller.

RUN Mode

During RUN mode the main voltage regulator is on. It will provide a regulated supply to all digital sections.

STOP Mode

During STOP mode, the STOP mode regulator will take care of suppling a regulated output voltage. The STOP mode regulator has a very limited output current capability. The output voltage will be lower as the output voltage of the main voltage regulator.

PACKAGE THERMAL PERFORMANCE

Figure 23 shows a thermal response curve for a package mounted onto a thermally enhanced PCB.

Note PCB board is a multi-layer with two inner copper planes (2s2p). The board conforms to JEDEC EIA/JESD 51-5 and JESD51-7. Substrate thickness is 1.60 mm. Top and bottom copper trace layers are 0.7 mm thick, with two inner copper planes of 0.35 mm thickness. Thermal vias have 0.35 mm thick plating.

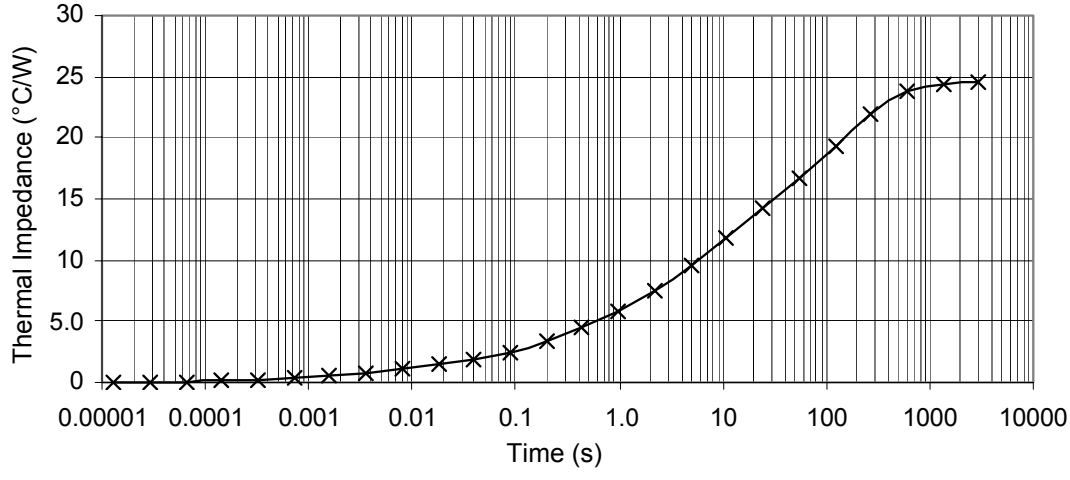
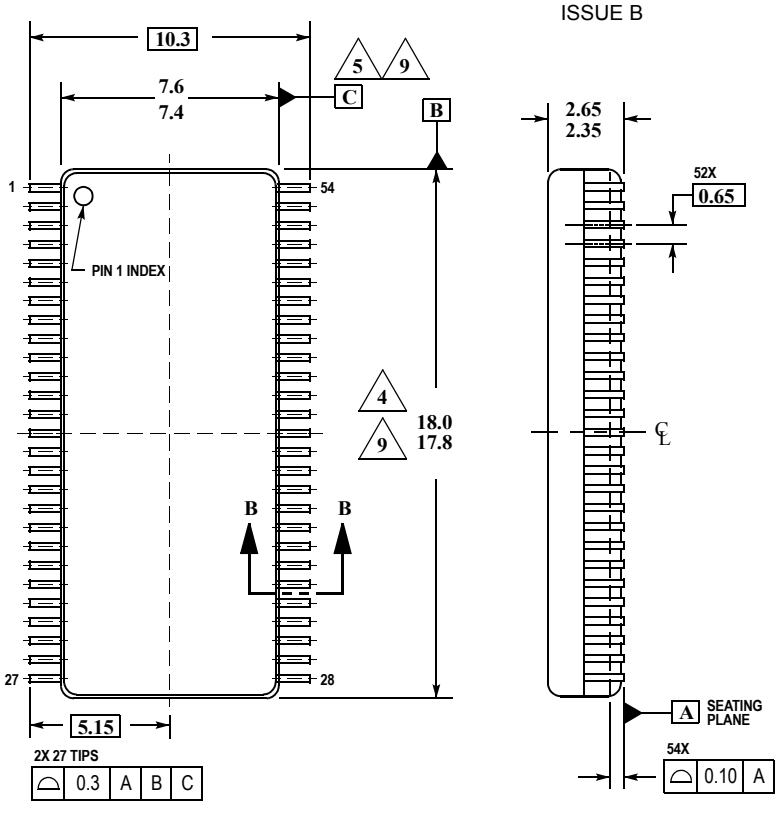


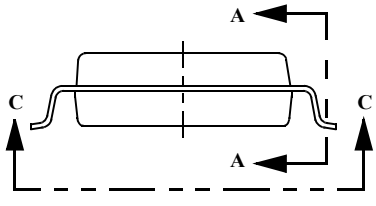
Figure 23. Thermal Response of H-Bridge Driver with Package Soldered to a JEDEC PCB Board

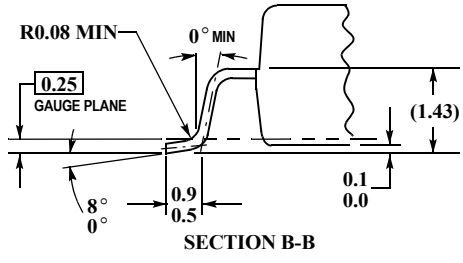
PACKAGE DIMENSIONS

DWB SUFFIX
54-TERMINAL SOIC WIDE BODY EXPOSED PAD
PLASTIC PACKAGE
CASE 1400-01
ISSUE B

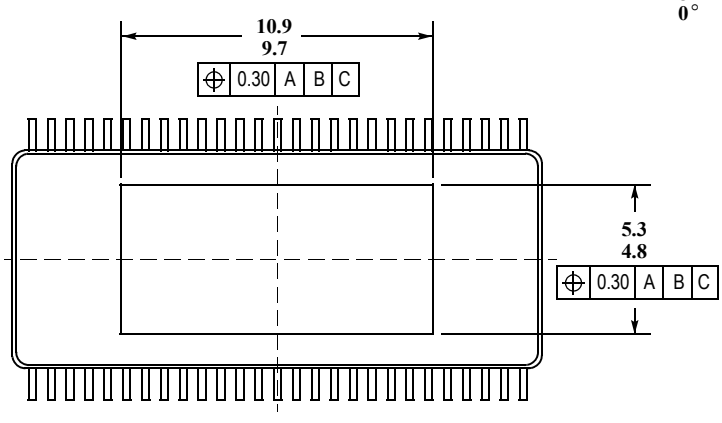


NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

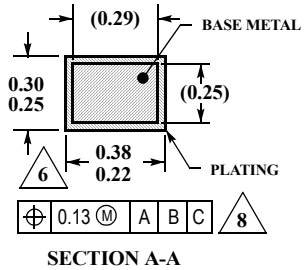




SECTION B-B



VIEW C-C



SECTION A-A
ROTATED 90° CLOCKWISE

NOTES

NOTES

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