# NCP1411

# Sync-Rect PFM Step-Up DC-DC Converter with Low-Battery Detector and Ring-Killer

NCP1411 is a monolithic micropower high frequency Boost (step−up) voltage switching converter IC specially designed for battery operated hand−held electronic products up to 250 mA loading. It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode. High switching frequency (up to 600 kHz) allows low profile inductor and output capacitor being used. Low−Battery Detector, Logic−Controlled Shutdown and Cycle−by−Cycle Current Limit provide value−added features for various battery−operated applications. The innovative Ring−Killer circuitry guarantees quiet operation in discontinuous conduction mode. With all these functions ON, the device quiescent supply current is only 9.0 μA typical. This device is available in the space saving compact Micro8™ package.

## Features

- Pb−Free Package is Available
- High Efficiency, up to 92%
- Very Low Device Quiescent Supply Current of 9.0 μA Typical
- Built−in Synchronous Rectifier (P−FET) Eliminates One External Schottky Diode
- High Switching Frequency (up to 600 kHz) Allows use of Small Size Inductor
- High Accuracy Reference Output, 1.19 V ± 0.6% @ 25°C, can supply more than 2.5 mA when $V_{OUT} \geq 3.3$ V
- Ring−Killer for Quiet Operation in Discontinuous Conduction Mode
- 1.0 V Startup at No Load Guaranteed
- Output Voltage from 1.5 V to 5.5 V Adjustable
- Output Current up to 250 mA @ $V_{IN}$ = 2.5 V, $V_{OUT}$ = 3.3 V
- Logic−Controlled Shutdown
- Open Drain Low−Battery Detector Output
- 1.0 A Cycle by Cycle Current Limit
- Low Profile and Minimum External Parts
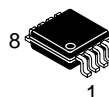- Compact Micro8 Package

## Typical Applications

- Personal Digital Assistant (PDA)
- Handheld Digital Audio Product
- Camcorder and Digital Still Camera
- Handheld Instrument
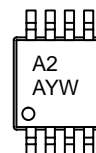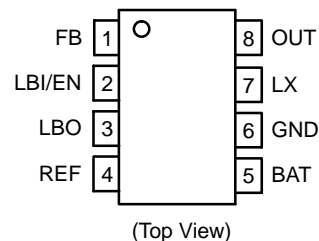- Conversion from One or Two NiMH or NiCd, or One Li−ion Cell to 3.3 V/5.0 V

**MARKING DIAGRAM**

8

Micro8
DM SUFFIX
CASE 846A

1

A2
AYW
○

A2 = Device Marking
A = Assembly Location
Y = Year
W = Work Week

**PIN CONNECTIONS**

| | |
|---|---|
| FB 1 ○ | 8 OUT |
| LBI/EN 2 | 7 LX |
| LBO 3 | 6 GND |
| REF 4 | 5 BAT |

(Top View)

# NCP1411
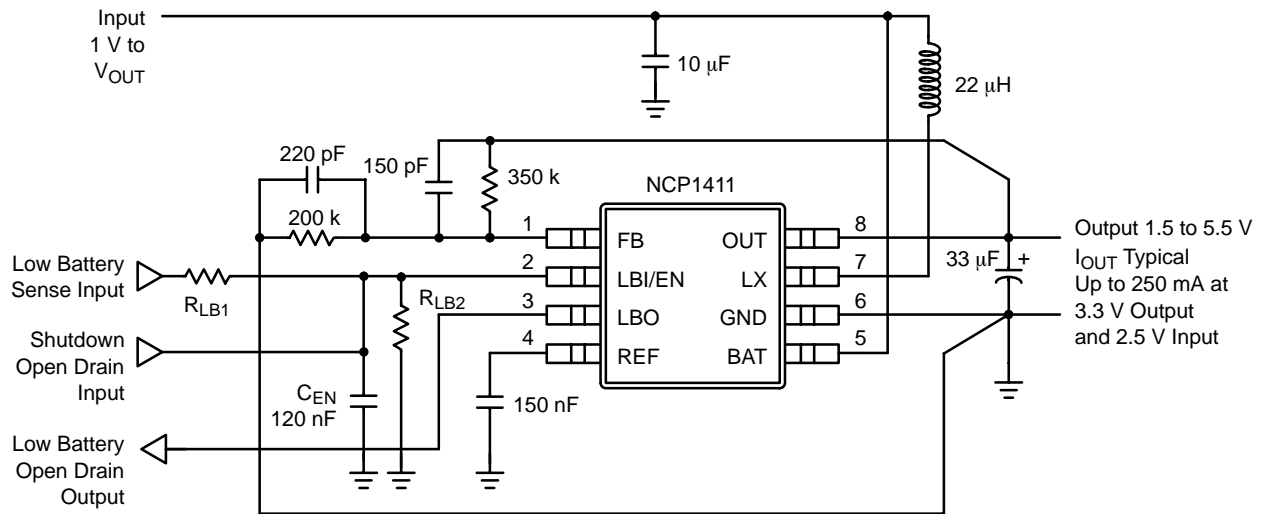


**Figure 1. Typical Operating Circuit**

## PIN FUNCTION DESCRIPTION

| Pin # | Symbol | Pin Description |
|-------|--------|-----------------|
| 1 | FB | Output Voltage Feedback Input. |
| 2 | LBI/EN | Low−Battery Detector Input and IC Enable. |
| 3 | LBO | Open−Drain Low−Battery Detector Output. Output is LOW when $V_{LBI}$ is < 1.178 V. LBO is high impedance during shutdown. |
| 4 | REF | 1.190 V Reference Voltage Output, bypassing with 150 nF capacitor if this pin is not loaded, bypassing with 1.0 μF if this pin is loaded up to 2.5 mA @ $V_{OUT}$ = 3.3 V. |
| 5 | BAT | Battery input connection for internal Ring−Killer. |
| 6 | GND | Ground. |
| 7 | LX | N−Channel and P−Channel Power MOSFET Drain Connection. |
| 8 | OUT | Power Output. OUT also provides bootstrapped power to the device. |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--------|--------|-------|------|
| Device Power Supply (Pin 8) | $V_{OUT}$ | −0.3 to 6.0 | V |
| Input/Output Pins (Pins 1−5, Pin 7) | $V_{IO}$ | −0.3 to 6.0 | V |
| Thermal Characteristics − Micro8 Plastic Package<br>  Maximum Power Dissipation @ $T_A$ = 25°C<br>  Thermal Resistance, Junction−to−Air | $P_D$<br>$R_{\theta JA}$ | 520<br>240 | mW<br>°C/W |
| Operating Junction Temperature Range | $T_J$ | −40 to +150 | °C |
| Operating Ambient Temperature Range | $T_A$ | −40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
1. This device contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

3. Latchup Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.
4. Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J−STD−020A.

**ELECTRICAL CHARACTERISTICS** ($V_{OUT}$ = 3.3 V, $T_A$ = 25°C for typical value, −40°C ≤ $T_A$ ≤ 85°C for min/max values unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Input Voltage | $V_{IN}$ | 1.0 | – | 5.5 | V |
| Output Voltage Range (Adjusted by external feedback) | $V_{OUT}$ | $V_{IN}$ | – | 5.5 | V |
| Reference Voltage ($C_{REF}$ = 150 nF, under no loading, $T_A$ = 25°C) | $V_{REF\_NL}$ | 1.183 | 1.190 | 1.197 | V |
| Reference Voltage <br> ($C_{REF}$ = 150 nF, under no loading, −40°C ≤ $T_A$ ≤ 85°C) | $V_{REF\_NL\_A}$ | 1.178 | – | 1.202 | V |
| Reference Voltage Temperature Coefficient | $TC_{VREF}$ | – | 0.03 | – | mV/°C |
| Reference Voltage Load Current <br> ($V_{OUT}$ = 3.3 V, $V_{REF}$ = $V_{REF\_NL}$ ±1.5%, $C_{REF}$ = 1.0 μF) (Note 5) | $I_{REF}$ | 2.5 | – | – | mA |
| Reference Voltage Load Regulation <br> ($V_{OUT}$ = 3.3 V, $I_{LOAD}$ = 0 to 100 μA, $C_{REF}$ = 1.0 μF) | $V_{REF\_LOAD}$ | – | 0.015 | 1.0 | mV |
| Reference Voltage Line Regulation <br> ($V_{OUT}$ from 1.5 V to 5.5 V, $C_{REF}$ = 1.0 μF) | $V_{REF\_LINE}$ | – | 0.03 | 1.0 | mV/V |
| FB, LBI Input Threshold ($I_{LOAD}$ = 0 mA) | $V_{FB}$, $V_{LBI}$ | 1.174 | 1.190 | 1.200 | V |
| N−FET ON Resistance | $R_{DS(ON)-N}$ | – | 0.6 | – | Ω |
| P−FET ON Resistance | $R_{DS(ON)-P}$ | – | 0.9 | – | Ω |
| LX Switch Current Limit (N−FET) | $I_{LIM}$ | – | 1.0 | – | A |
| Operating Current into OUT <br> ($V_{FB}$ = 1.4 V, i.e. no switching, $V_{OUT}$ = 3.3 V) | $I_Q$ | – | 9.0 | 14 | μA |
| Shutdown Current into OUT (LBI/EN = GND) | $I_{SD}$ | – | 0.05 | 1.0 | μA |
| LX Switch MAX. ON−Time ($V_{FB}$ = 1.0 V, $V_{OUT}$ = 3.3 V) | $t_{ON}$ | 1.2 | 1.4 | 1.8 | μS |
| LX Switch MIN. OFF−Time ($V_{FB}$ = 1.0 V, $V_{OUT}$ = 3.3 V) | $t_{OFF}$ | 0.25 | 0.31 | 0.37 | μS |
| FB Input Current | $I_{FB}$ | – | 1.5 | 9.0 | nA |
| Shutdown Current into BAT (LBI/EN = 0 V, $V_{OUT}$ = $V_{BAT}$ = 3.0 V) | $I_{LBT}$ | – | 50 | – | nA |
| BAT to LX resistance ($V_{FB}$ = 1.4 V, $V_{OUT}$ = 3.3 V) | $R_{LBT\_LX}$ | – | 100 | – | Ω |
| LBI/EN Input Current | $I_{LBI/EN}$ | – | 1.5 | 8.0 | nA |
| LBO Low Output Voltage ($V_{LBI}$ = 0 V, $I_{SINK}$ = 1.0 mA) | $V_{LBO\_L}$ | – | – | 0.05 | V |
| ENABLE (Pin 2) Input threshold, Low | $V_{EN}$ | – | – | 0.3 | V |
| ENABLE (Pin 2) Input threshold, High | $V_{EN}$ | 0.6 | – | – | V |

5. Loading capability increases with $V_{OUT}$.

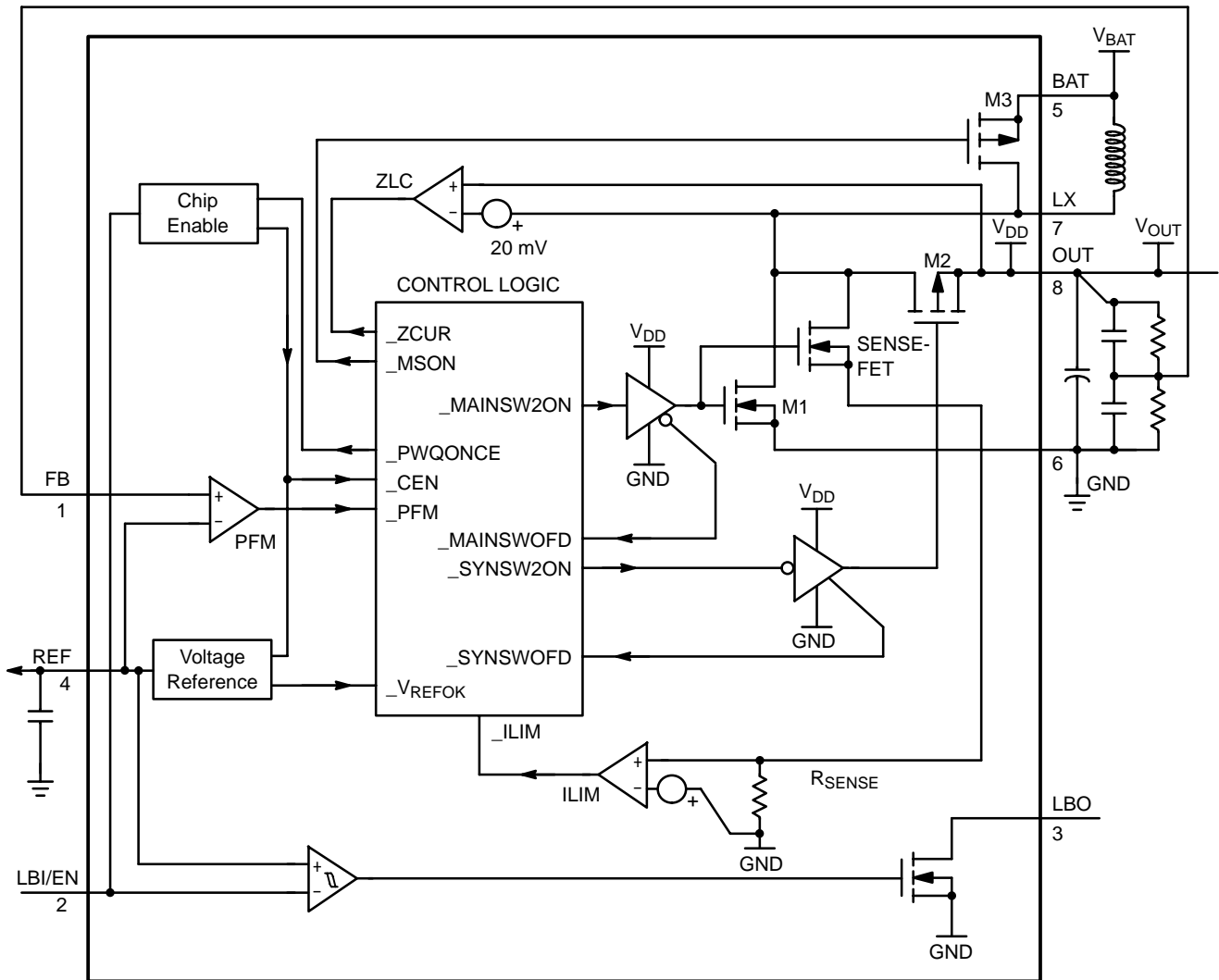**Figure 2. Simplified Functional Diagram**
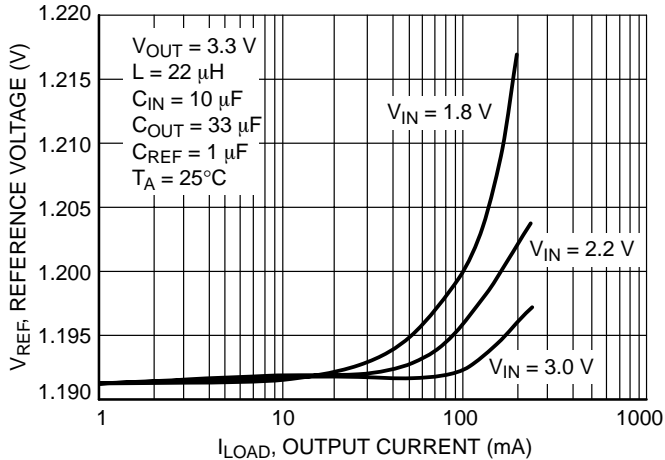
## TYPICAL OPERATING CHARACTERISTICS

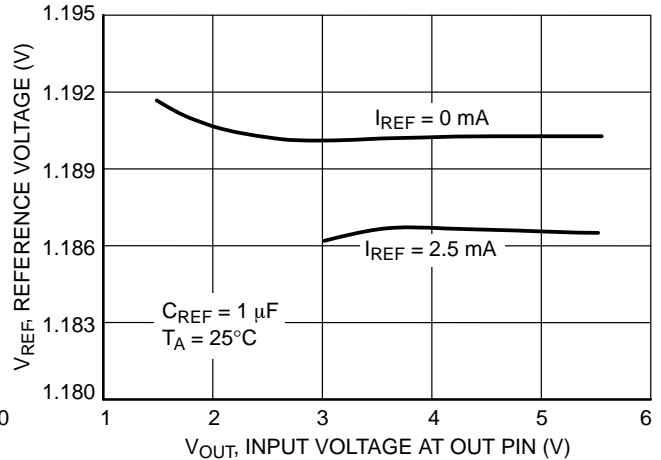**Figure 3. Reference Voltage versus Output
Current**

$V_{OUT} = 3.3$ V
$L = 22$ µH
$C_{IN} = 10$ µF
$C_{OUT} = 33$ µF
$C_{REF} = 1$ µF
$T_A = 25°C$

$V_{IN} = 1.8$ V
$V_{IN} = 2.2$ V
$V_{IN} = 3.0$ V

$I_{LOAD}$, OUTPUT CURRENT (mA)
$V_{REF}$, REFERENCE VOLTAGE (V)

**Figure 4. Reference Voltage versus Input
Voltage at OUT Pin**

$I_{REF} = 0$ mA
$I_{REF} = 2.5$ mA

$C_{REF} = 1$ µF
$T_A = 25°C$

$V_{OUT}$, INPUT VOLTAGE AT OUT PIN (V)
$V_{REF}$, REFERENCE VOLTAGE (V)
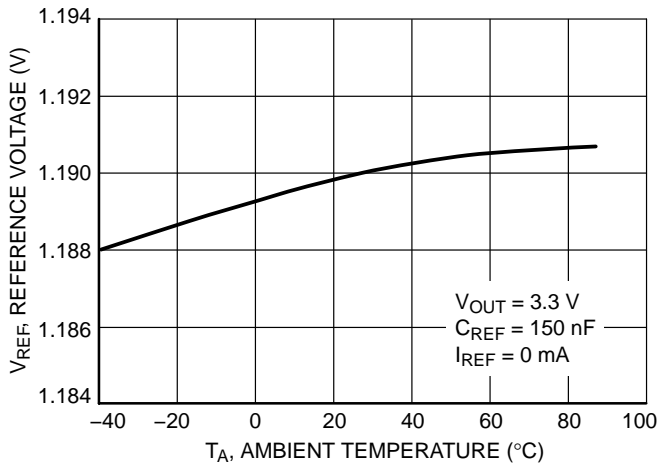
**Figure 5. Reference Voltage versus
Temperature**

$V_{OUT} = 3.3$ V
$C_{REF} = 150$ nF
$I_{REF} = 0$ mA

$T_A$, AMBIENT TEMPERATURE (°C)
$V_{REF}$, REFERENCE VOLTAGE (V)
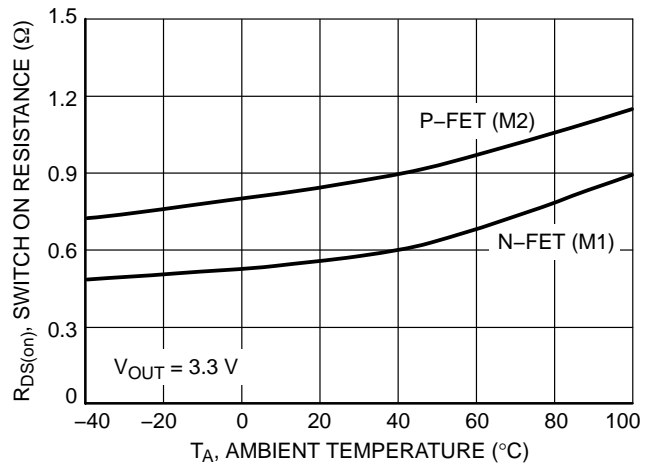
**Figure 6. Switch ON Resistance versus
Temperature**

P–FET (M2)
N–FET (M1)

$V_{OUT} = 3.3$ V

$T_A$, AMBIENT TEMPERATURE (°C)
$R_{DS(on)}$, SWITCH ON RESISTANCE (Ω)
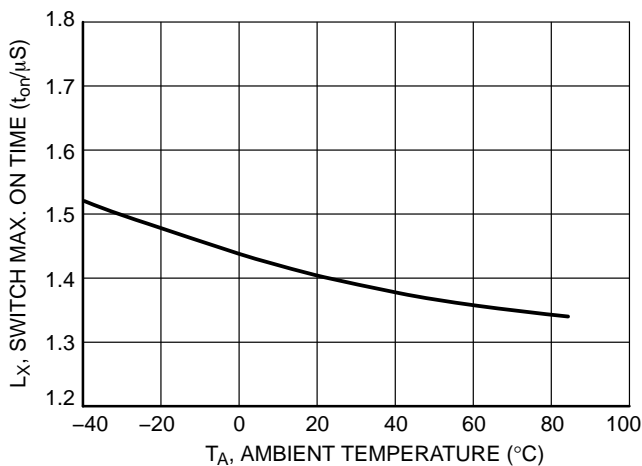
**Figure 7. $L_X$ Switch Max. ON Time versus
Temperature**

$T_A$, AMBIENT TEMPERATURE (°C)
$L_X$, SWITCH MAX. ON TIME ($t_{on}$/µS)
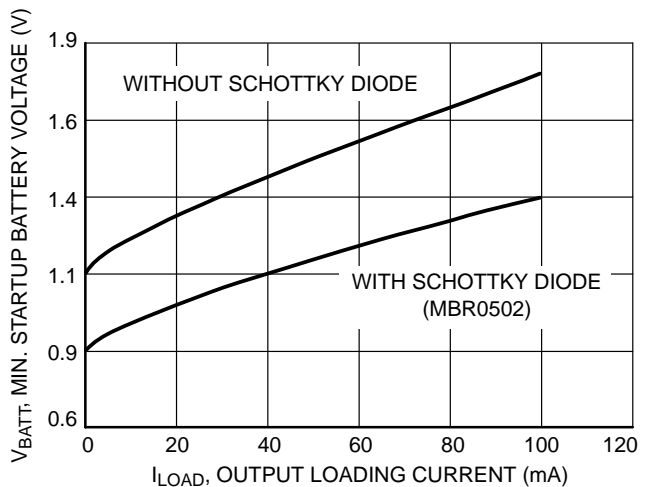
**Figure 8. Min. Startup Battery Voltage versus
Loading Current**

WITHOUT SCHOTTKY DIODE
WITH SCHOTTKY DIODE
(MBR0502)

$I_{LOAD}$, OUTPUT LOADING CURRENT (mA)
$V_{BATT}$, MIN. STARTUP BATTERY VOLTAGE (V)
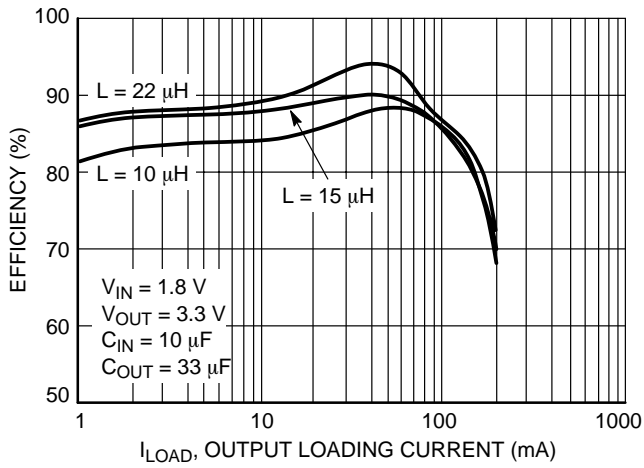
**Figure 9. Efficiency versus Load Current**

V$_{IN}$ = 1.8 V
V$_{OUT}$ = 3.3 V
C$_{IN}$ = 10 μF
C$_{OUT}$ = 33 μF

L = 22 μH
L = 10 μH
L = 15 μH
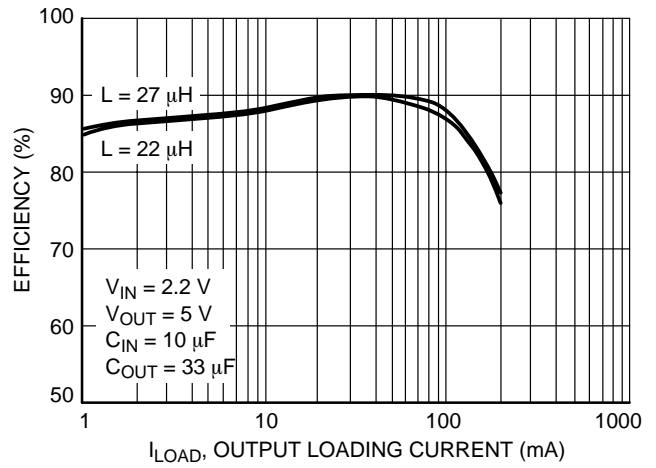


**Figure 10. Efficiency versus Load Current**

V$_{IN}$ = 2.2 V
V$_{OUT}$ = 5 V
C$_{IN}$ = 10 μF
C$_{OUT}$ = 33 μF

L = 27 μH
L = 22 μH
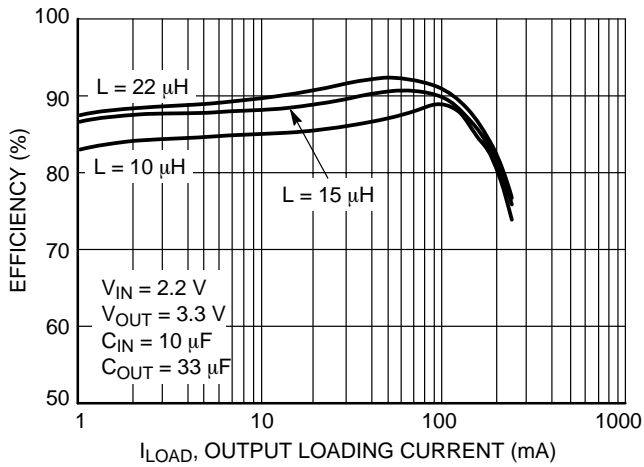


**Figure 11. Efficiency versus Load Current**

V$_{IN}$ = 2.2 V
V$_{OUT}$ = 3.3 V
C$_{IN}$ = 10 μF
C$_{OUT}$ = 33 μF

L = 22 μH
L = 10 μH
L = 15 μH
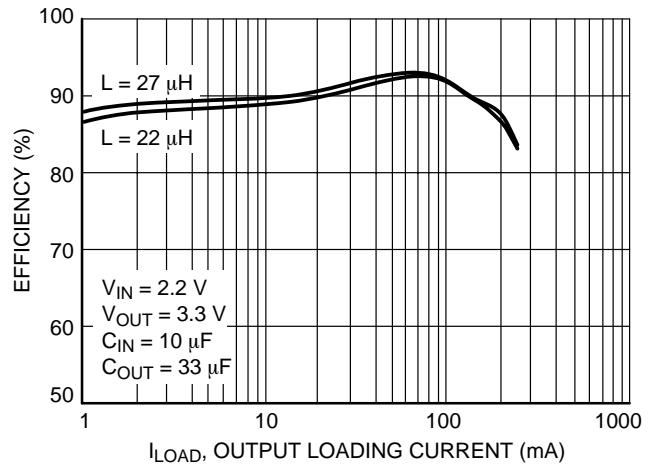


**Figure 12. Efficiency versus Load Current**

V$_{IN}$ = 2.2 V
V$_{OUT}$ = 3.3 V
C$_{IN}$ = 10 μF
C$_{OUT}$ = 33 μF

L = 27 μH
L = 22 μH
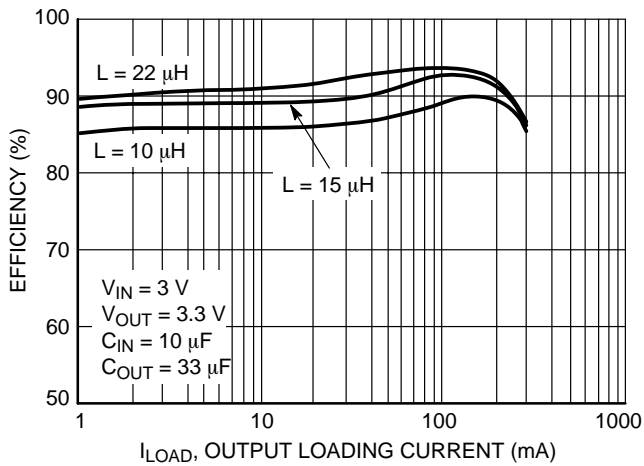


**Figure 13. Efficiency versus Load Current**

V$_{IN}$ = 3 V
V$_{OUT}$ = 3.3 V
C$_{IN}$ = 10 μF
C$_{OUT}$ = 33 μF

L = 22 μH
L = 10 μH
L = 15 μH
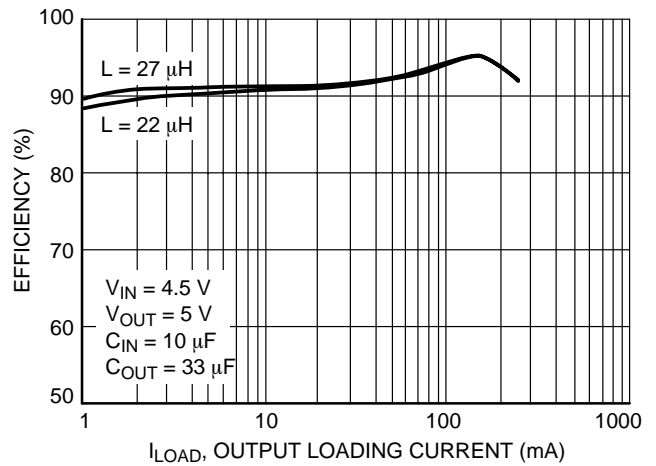


**Figure 14. Efficiency versus Load Current**

V$_{IN}$ = 4.5 V
V$_{OUT}$ = 5 V
C$_{IN}$ = 10 μF
C$_{OUT}$ = 33 μF

L = 27 μH
L = 22 μH

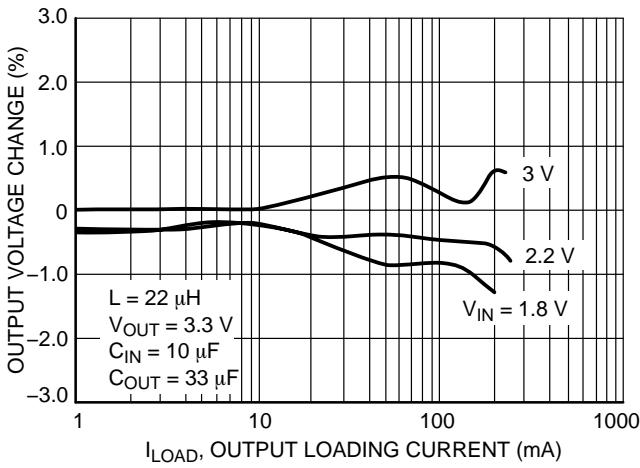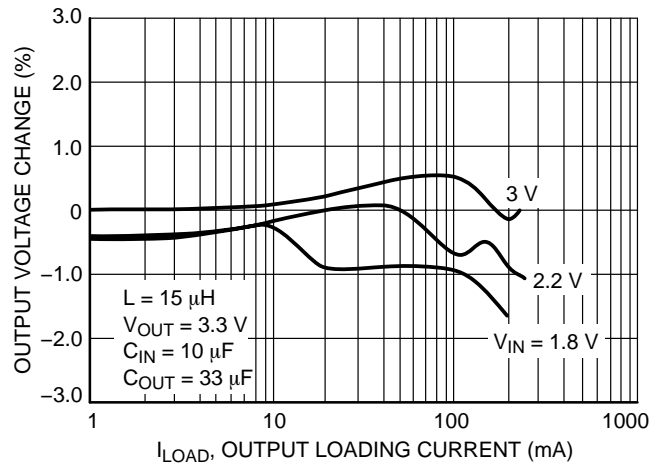**Figure 15. Output Voltage Change versus Load Current**



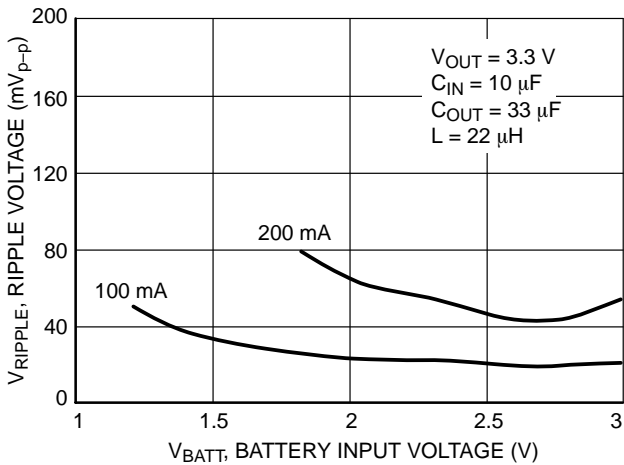**Figure 16. Output Voltage Change versus Load Current**
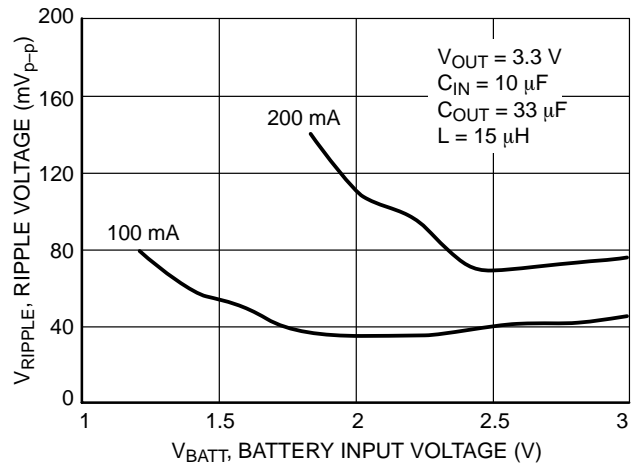


**Figure 17. Battery Input Voltage versus Output Ripple Voltage**



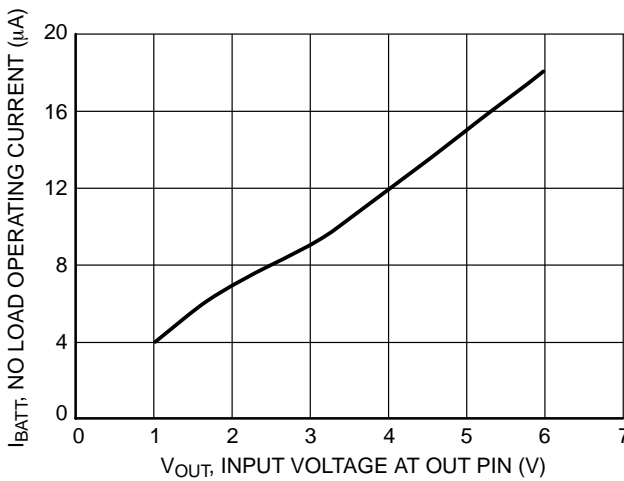**Figure 18. Battery Input Voltage versus Output Ripple Voltage**



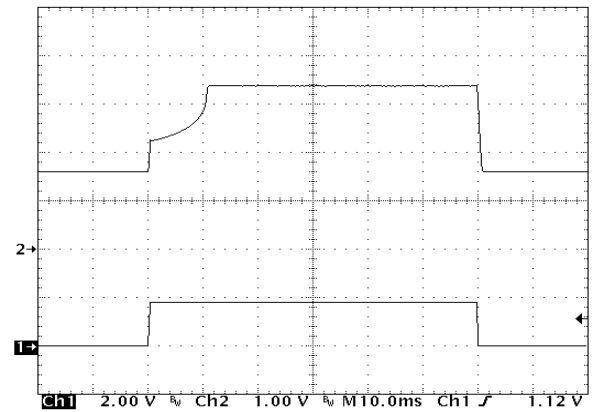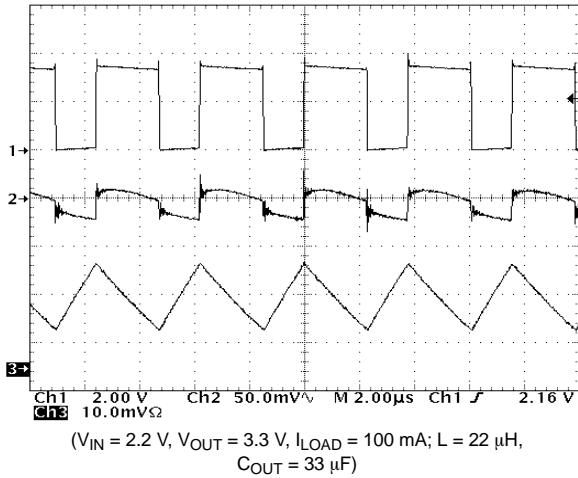**Figure 19. No Load Operating Current versus Input Voltage at OUT Pin**



($V_{IN}$ = 2.2 V, $V_{OUT}$ = 3.3 V, $I_{LOAD}$ = 100 mA; L = 22 μH, $C_{OUT}$ = 33 μF)
Upper Trace: Output Voltage Waveform, 2.0 V/Division
Lower Trace: Shutdown Pin Waveform, 1.0 V/Division

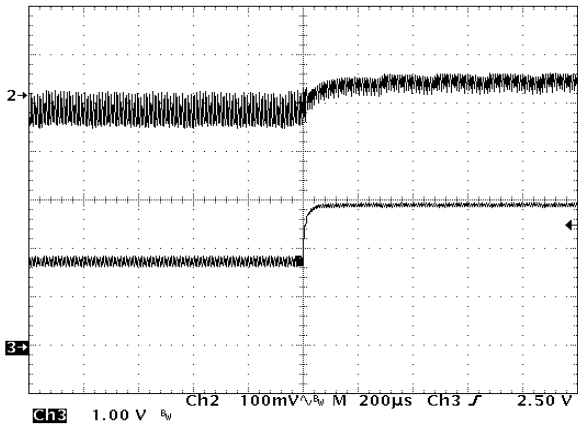**Figure 20. Startup Transient Response**

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($V_{IN}$ = 2.2 V, $V_{OUT}$ = 3.3 V, $I_{LOAD}$ = 100 mA; L = 22 μH, $C_{OUT}$ = 33 μF)
Upper Trace: Voltage at $L_X$ pin, 2.0 V/Division
MiddleTrace: Output Voltage Ripple, 50 mV/Division
Lower Trace: Inductor Current, $I_L$, 100 mA/Division

**Figure 21. Continuous Conduction Mode Switching Waveform**
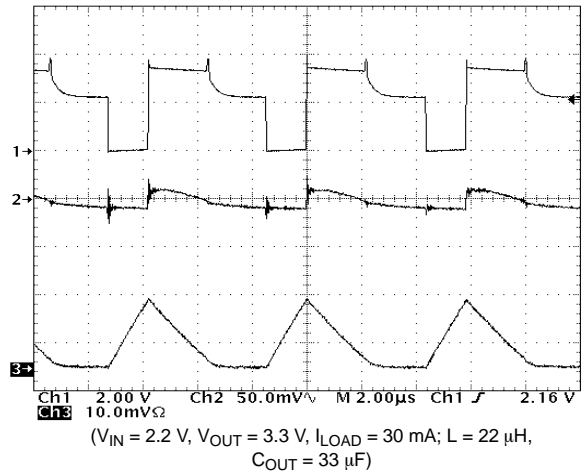


($V_{IN}$ = 2.2 V, $V_{OUT}$ = 3.3 V, $I_{LOAD}$ = 30 mA; L = 22 μH, $C_{OUT}$ = 33 μF)
Upper Trace: Voltage at $L_X$ pin, 2.0 V/Division
MiddleTrace: Output Voltage Ripple, 50 mV/Division
Lower Trace: Inductor Current, $I_L$, 100 mA/Division

**Figure 22. Discontinuous Conduction Mode Switching Waveform**



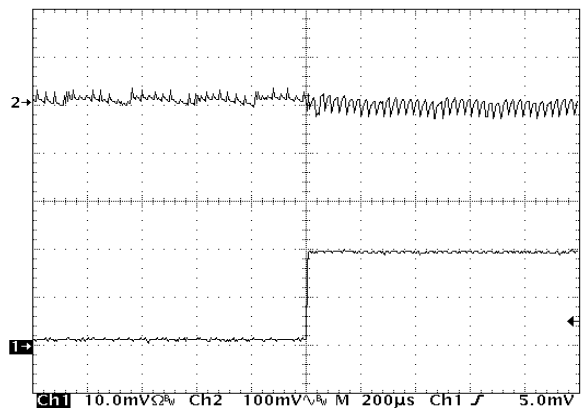($V_{IN}$ = 1.8 V to 3.0 V, L = 22 μH, $C_{OUT}$ = 33 μF)
Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Battery Voltage, $V_{IN}$, 1.0 V/Division

**Figure 23. Line Transient Response for $V_{OUT}$ = 3.3 V**
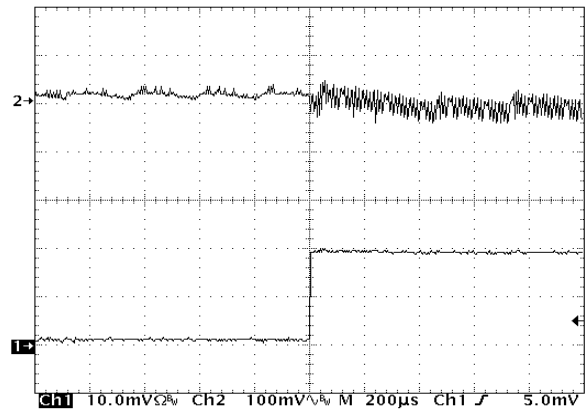


($V_{OUT}$ = 3.3 V, $I_{LOAD}$ = 10 mA to 100 mA; L = 22 μH, $C_{OUT}$ = 33 μF)
Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, $I_{LOAD}$, 50 mA/Division

**Figure 24. Load Transient Response for $V_{IN}$ = 1.8 V**



($V_{OUT}$ = 3.3 V, $I_{LOAD}$ = 10 mA to 100 mA; L = 22 μH, $C_{OUT}$ = 33 μF)
Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, $I_{LOAD}$, 50 mA/Division

**Figure 25. Load Transient Response for $V_{IN}$ = 2.4 V**



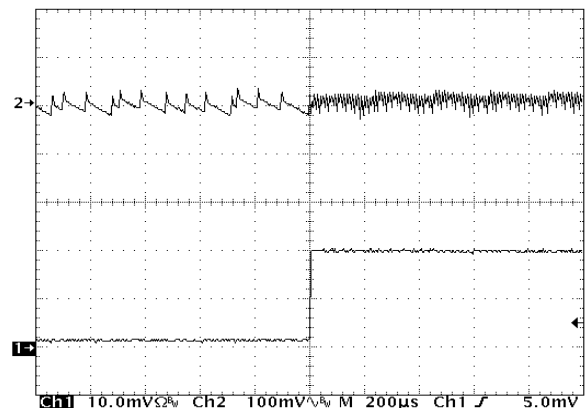($V_{OUT}$ = 3.3 V, $I_{LOAD}$ = 10 mA to 100 mA; L = 22 μH, $C_{OUT}$ = 33 μF)
Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, $I_{LOAD}$, 50 mA/Division

**Figure 26. Load Transient Response for $V_{IN}$ = 3.3 V**

## DETAILED OPERATION DESCRIPTIONS

NCP1411 is a monolithic micropower high frequency step−up voltage switching converter IC specially designed for battery operated hand−held electronic products up to 250 mA loading. It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode. High switching frequency (up to 600 kHz) allows low profile inductor and output capacitor being used. Low−Battery Detector, Logic−Controlled Shutdown and Cycle−by−Cycle Current Limit provide value−added features for various battery−operated application. With all these functions ON, the quiescent supply current is only 9.0 μA typical. This device is available in a compact Micro8 package.

### PFM Regulation Scheme

From the simplified Functional Diagram (Figure 2), the output voltage is divided down and fed back to pin 1 (FB). This voltage goes to the non−inverting input of the PFM comparator whereas the comparator's inverting input is connected to REF. A switching cycle is initiated by the falling edge of the comparator, at the moment, the main switch (M1) is turned ON. After the maximum ON−time (typical 1.4 μS) elapses or the current limit is reached, M1 is turned OFF, and the synchronous switch (M2) is turned ON. The M1 OFF time is not less than the minimum OFF−time (typical 0.31 μS), this is to ensure energy transfer from the inductor to the output capacitor. If the regulator is operating at Continuous Conduction Mode (CCM), M2 is turned OFF just before M1 is supposed to be ON again. If the regulator is operating at Discontinuous Conduction Mode (DCM), which means the coil current will decrease to zero before the next cycle, M1 is turned OFF as the coil current is almost reaching zero. The comparator (ZLC) with fixed offset is dedicated to sense the voltage drop across M2 as it is conducting, when the voltage drop is below the offset, the ZLC comparator output goes HIGH, and M2 is turned OFF. Negative feedback of closed loop operation regulates voltage at pin 1 (FB) equal to the internal voltage reference (1.190 V).

### Synchronous Rectification

Synchronous Rectifier is used to replace Schottky Diode for eliminating the conduction loss contributed by forward voltage of the latter. Synchronous Rectifier is normally realized by powerFET with gate control circuitry which, however, involved relative complicated timing concerns.

As main switch M1 is being turned OFF, if the synchronous switch M2 is just turned ON with M1 not being completed turned OFF, current will be shunt from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency. So a certain amount of dead time is introduced to make sure M1 is completely OFF before M2 is being turned ON.

When the main regulator is operating in CCM, as M2 is being turned OFF, and M1 is just turned ON with M2 not being completely turned OFF, the above mentioned situation will occur. So dead time is introduced to make sure M2 is completely turned OFF before M1 is being turned ON.

When the regulator is operating in DCM, as coil current is dropped to zero, M2 is supposed to be OFF. Fail to do so, reverse current will flow from the output bulk capacitor through M2 and then the inductor to the battery input. It causes damage to the battery. So the ZLC comparator comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 is switch OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss. Therefore, determination on the offset voltage is essential for optimum performance.

With the implementation of synchronous rectification, efficiency can be as high as 92%. For single cell input voltage, use an external Schottky diode such as MBR0520 connected from pin 7 to pin 8 to ensure quick startup.

### Ring−Killer

When the device entered Discontinuous Conduction Mode operation, a typical ringing at LX pin will start while the inductor current just ceased. This ringing is caused primarily by the capacitance and inductance at LX node and the result can produce unwanted EMI problem to the system. In order to eliminate this ringing, an internal damping switch (M3) is implemented to provide a low impedance path to dissipate the residue energy stored in the inductor once the operation entered the Discontinuous Conduction Mode. This feature can improve the EMI problem. The performance of the Ring−Killer switch is shown in Figure 22.

### Cycle−by−Cycle Current Limit

From Figure 2, SENSEFET is applied to sample the coil current as M1 is ON. With that sample current flowing through a sense resistor, sense−voltage is developed. Threshold detector (ILIM) detects whether the sense−voltage is higher than preset level. If it happens, detector output signifies the CONTROL LOGIC to switch OFF M1, and M1 can only be switched ON as next cycle starts after the minimum OFF−time (typical 0.31 μS). With properly sizing of SENSEFET and sense resistor, the peak coil current limit is set at 1.0 A typically.

### Voltage Reference

The voltage at REF is set typically at +1.190 V. It can deliver up to 2.5 mA with load regulation ±1.5%, at $V_{OUT}$ equal to 3.3 V. If $V_{OUT}$ is increased, the REF load capability can also be increased. A bypass capacitor of 0.15 μF is required for proper operation when REF is not loaded. If REF is loaded, 1.0 μF capacitor at REF is needed.

### Shutdown

The IC will shutdown when the voltage at pin 2 (LBI/EN) is pulled lower than 0.3 V. During shutdown, M1 and M2 are both switched OFF, however, the body diode of M2 allows current flow from battery to the output, the IC internal circuit will consume less than 0.05 μA current typically. If the

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pin 1 voltage raised higher than 0.6 V, the IC will be enabled. The internal circuit will only consume 9.0 μA current typically from the OUT pin. In order to ensure proper startup, a timing capacitor $C_{EN}$ as shown in Figure 1 is required to provide the reset pulse during batteries are plugged in. The product of $R_{LB1}$ and $C_{EN}$ must be larger than 28 msec.

**Low−Battery Detection**

A comparator with 30 mV hysteresis is applied to perform the low−battery detection function. When pin 2 (LBI/EN) is at a voltage, which can be defined by a resistor divider from the battery voltage, lower than the internal reference voltage, 1.190 V, the comparator output will cause a 50 Ohm low side switch to be turned ON. It will pull down the voltage at pin 3 (LBO) which has a hundreds kilo−Ohm of pull−high resistance. If the pin 2 voltage is higher than 1.190 V +30 mV, the comparator output will cause the 50 Ohm low side switch to be turned OFF, pin 3 will become high impedance, and its voltage will be pulled high.

## APPLICATIONS INFORMATION

**Output Voltage Setting**

The output voltage of the converter is determined by the external feedback network comprised of $R_{FB1}$ and $R_{FB2}$ and the relationship is given by:

$$V_{OUT} = 1.190\ V \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where $R_{FB1}$ and $R_{FB2}$ are the upper and lower feedback resistors respectively.

**Low Battery Detect Level Setting**

The Low Battery Detect Voltage of the converter is determined by the external divider network comprised of $R_{LB1}$ and $R_{LB2}$ and the relationship is given by:

$$V_{LB} = 1.190\ V \times \left(1 + \frac{R_{LB1}}{R_{LB2}}\right)$$

where $R_{LB1}$ and $R_{LB2}$ are the upper and lower divider resistors respectively.

**Inductor Selection**

The NCP1411 is tested to produce optimum performance with a 22 μH inductor at $V_{IN}$ = 3.0 V, $V_{OUT}$ = 3.3 V supplying output current up to 250 mA. For other input/output requirements, inductance in the range 10 μH to 47 μH can be used according to end application specifications. Selecting an inductor is a compromise between output current capability and tolerable output voltage ripple. Of course, the first thing we need to obey is to keep the peak inductor current below its saturation limit at maximum current and the $I_{LIM}$ of the device. In NCP1411, $I_{LIM}$ is set at 1.0 A. As a rule of thumb, low inductance values supply higher output current, but also increase the ripple at output and reducing efficiency, on the other hand, high inductance values can improve output ripple and efficiency, however it also limit the output current capability at the same

time. One other parameter of the inductor is its DC resistance, this resistance can introduce unwanted power loss and hence reduce overall efficiency, the basic rule is selecting an inductor with lowest DC resistance within the board space limitation of the end application.

**Capacitors Selection**

In all switching mode boost converter applications, both the input and output terminals sees impulsive voltage/current waveforms. The currents flowing into and out of the capacitors multiplying with the Equivalent Series Resistance (ESR) of the capacitor producing ripple voltage at the terminals. During the syn−rect switch off cycle, the charges stored in the output capacitor is used to sustain the output load current. Load current at this period and the ESR combined and reflected as ripple at the output terminal. For all cases, the lower the capacitor ESR, the lower the ripple voltage at output. As a general guide line, low ESR capacitors should be used. Ceramic capacitors have the lowest ESR, but low ESR tantalum capacitors can also be used as a cost effective substitute.

**Optional Startup Schottky Diode for Low Battery Voltage**

In general operation, no external schottky diode is required, however, in case you are intended to operate the device close to 1.0 V level, a schottky diode connected between the LX and OUT pins as shown in Figure 27 can help during startup of the converter. The effect of the additional schottky was shown in Figure 8.
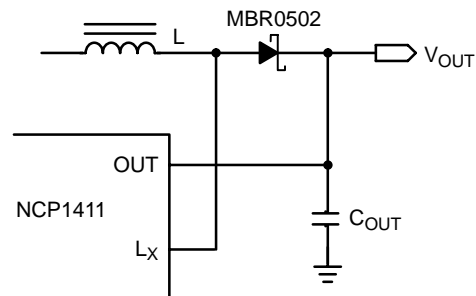


**Figure 27. PCB Layout Recommendations**

**PCB Layout Recommendations**

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedback that can affect the performance of the converter. Hints suggested in below can be used as a guide line in most situations.

**Grounding**

Star−ground connection should be used to connect the output power return ground, the input power return ground and the device power ground together at one point. All high current running paths must be thick enough for current flowing through and producing insignificant voltage drop

along the path. Feedback signal path must be separated with the main current path and sensing directly at the anode of the output capacitor.

kept away from the feedback (FB, pin 1) terminal to avoid unwanted injection of noise into the feedback path.

**Components Placement**

Power components, i.e. input capacitor, inductor and output capacitor, must be placed as close together as possible. All connecting traces must be short, direct and thick. High current flowing and switching paths must be

**Feedback Network**

Feedback of the output voltage must be a separate trace detached from the power path. External feedback network must be placed very close to the feedback (FB, pin 1) pin and sensing the output voltage directly at the anode of the output capacitor.
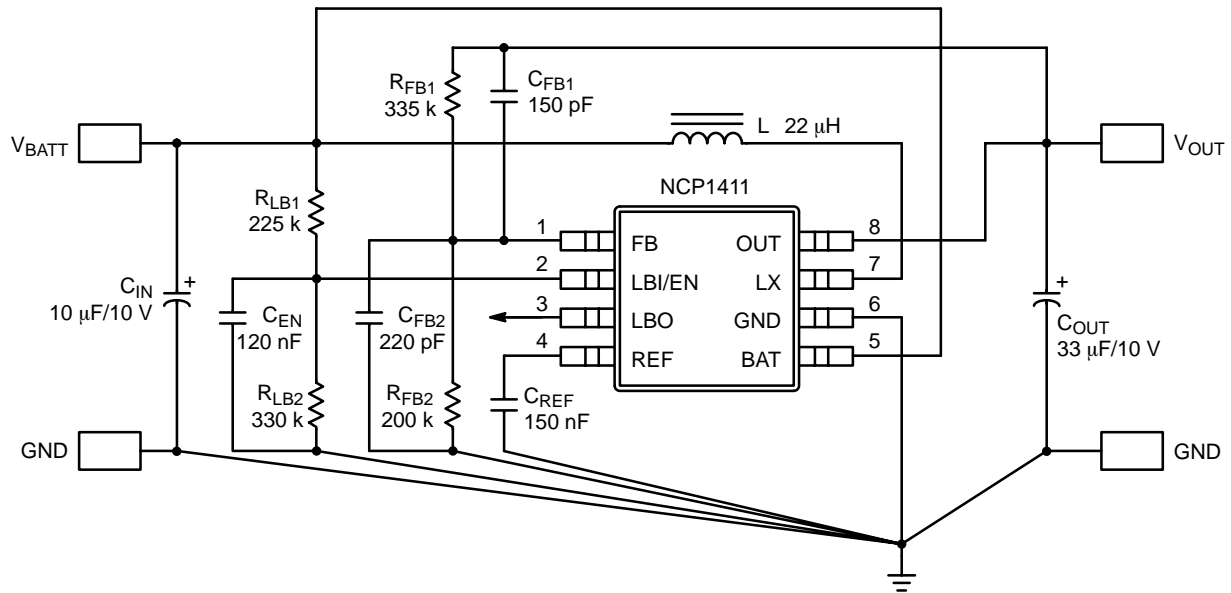
**Figure 28. Typical Application Schematic for 2 Alkaline Cells Supply**

## **GENERAL DESIGN PROCEDURES**

Switching mode converter design is considered as black magic to most engineers, some complicate empirical formulae are available for reference usage. Those formulae are derived from the assumption that the key components, i.e. power inductor and capacitors are available with no tolerance. Practically, its not true, the result is not a matter of how accurate the equations you are using to calculate the component values, the outcome is still somehow away from the optimum point. In below a simple method base on the most basic first order equations to estimate the inductor and capacitor values for NCP1411 operate in Continuous Conduction Mode is introduced. The component value set can be used as a starting point to fine tune the circuit operation. By all means, detail bench testing is needed to get the best performance out of the circuit.

Design Parameters:

$V_{IN}$ = 1.8 V to 3.0 V, Typical 2.4 V
$V_{OUT}$ = 3.3 V
$I_{OUT}$ = 200 mA (250 mA max)
$V_{LB}$ = 2.0 V
$V_{OUT-RIPPLE}$ = 40 m$V_{P-P}$ at $I_{OUT}$ = 250 mA

Calculate the feedback network:

Select $R_{FB2}$ = 200 K

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

$$R_{FB1} = 200\,K\left(\frac{3.3\,V}{1.19\,V} - 1\right) = 355\,K$$

With the feedback resistor divider, additional small capacitor, $C_{FB1}$ in parallel with $R_{FB1}$ is required to ensure stability. The value can be in between 68 pF to 220 pF, the rule is to select the lowest capacitance to ensure stability. Also a small capacitor, $C_{FB2}$ in parallel with $R_{FB2}$ may also be needed to lower the feedback ripple hence improve output regulation. The use of $C_{FB2}$ is a compromise between output ripple level and regulation, so careful selection of the value according to end application requirement is needed. In this example, values for $C_{FB1}$ and $C_{FB2}$ are 150 pF and 220 pF respectively.

Calculate the Low Battery Detect divider:

$V_{LB}$ = 2.0 V
Select $R_{LB2}$ = 330 K

$$R_{LB1} = R_{LB2}\left(\frac{V_{LB}}{V_{REF}} - 1\right)$$

$$R_{LB1} = 330\,K\left(\frac{2.0\,V}{1.19\,V} - 1\right) = 225\,K$$

$$C_{EN} = \frac{28\,msec}{225\,K} = 120\,nF$$

Determine the Steady State Duty Ratio, D for typical $V_{IN}$, operation will be optimized around this point:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 1 - \frac{2.4\,V}{3.3\,V} = 0.273$$

Determine the average inductor current, $I_{LAVG}$ at maximum $I_{OUT}$:

$$I_{LAVG} = \frac{I_{OUT}}{1-D} = \frac{250\,mA}{1-0.273} = 344\,mA$$

Determine the peak inductor ripple current, $I_{RIPPLE-P}$ and calculate the inductor value:

Assume $I_{RIPPLE-P}$ is 20% of $I_{LAVG}$, the inductance of the power inductor can be calculated as in below:

$I_{RIPPLE-P}$ = 0.20 x 344 mA = 68.8 mA

$$L = \frac{V_{IN} \times t_{ON}}{2I_{RIPPLE-P}} = \frac{2.4\,V \times 1.4\,\mu S}{2(68.8\,mA)} = 24.4\,\mu H$$

Standard value of 22 μH is selected for initial trial.

Determine the output voltage ripple, $V_{OUT-RIPPLE}$ and calculate the output capacitor value:

$V_{OUT-RIPPLE}$ = 40 m$V_{P-P}$ at $I_{OUT}$ = 250 mA

$$C_{OUT} \geq \frac{I_{OUT} \times t_{ON}}{V_{OUT-RIPPLE} - I_{OUT} \times ESR_{COUT}}$$

where $t_{ON}$ = 1.4 μS and $ESR_{COUT}$ = 0.1 Ω,

$$C_{OUT} \geq \frac{250\,mA \times 1.4\,\mu S}{40\,mV - 250\,mA \times 0.1\,\Omega} = 23.33\,\mu F$$

From above calculation, we need at least 23.33 μF in order to achieve the specified ripple level at conditions stated. Practically, a one level larger capacitor will be used to accommodate factors not take into account in the calculation. So a capacitor value of 33 μF is selected.

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## PACKAGE DIMENSIONS

**Micro8**
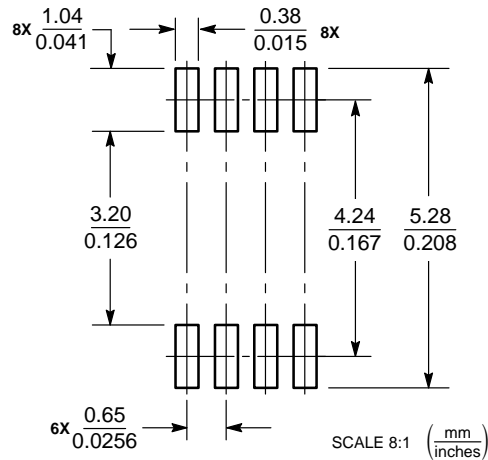**DM SUFFIX**
CASE 846A–02
ISSUE F
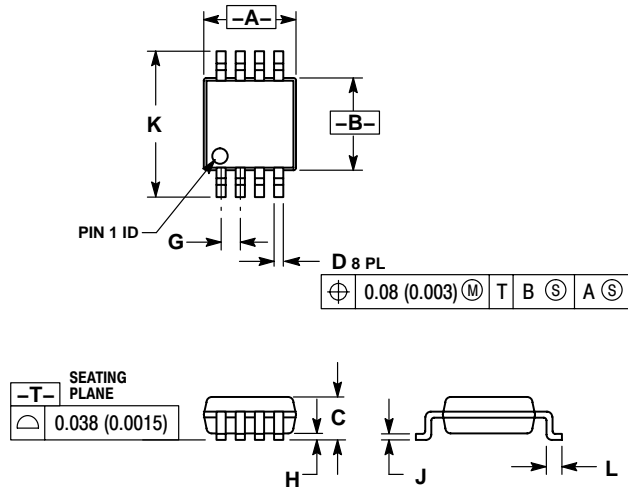
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A–01 OBSOLETE, NEW STANDARD 846A–02.

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
|  | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | --- | 1.10 | --- | 0.043 |
| D | 0.25 | 0.40 | 0.010 | 0.016 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.05 | 0.15 | 0.002 | 0.006 |
| J | 0.13 | 0.23 | 0.005 | 0.009 |
| K | 4.75 | 5.05 | 0.187 | 0.199 |
| L | 0.40 | 0.70 | 0.016 | 0.028 |

$\oplus$ | 0.08 (0.003) Ⓜ | T | B Ⓢ | A Ⓢ

−A−
−B−
K
PIN 1 ID
G
D 8 PL

−T−
SEATING PLANE
△ 0.038 (0.0015)
C
H
J
L

## SOLDERING FOOTPRINT*

8X $\frac{1.04}{0.041}$   $\frac{0.38}{0.015}$ 8X

$\frac{3.20}{0.126}$   $\frac{4.24}{0.167}$   $\frac{5.28}{0.208}$

6X $\frac{0.65}{0.0256}$

SCALE 8:1  $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Micro8 is a trademark of International Rectifier.