

#### **BROADBAND HIGH LINEARITY AMPLIFIER**

## **Pb-Free Product**

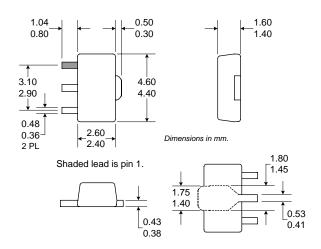
## **Typical Applications**

- Basestation Applications
- Cellular and PCS Systems

- WLL, W-CDMA Systems
- Final PA for Low-Power Applications

## **Product Description**

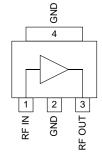
The RF3315 is a high-efficiency GaAs Heterojunction Bipolar Transistor (HBT) amplifier packaged in a low-cost surface-mount package. This amplifier is ideal for use in applications requiring high-linearity and low noise figure over the 300MHz to 3GHz frequency range. The RF3315 operates from a single 5V power supply.



#### **Optimum Technology Matching® Applied**

- ☐ Si BJT ☐ Si Bi-CMOS ☐
- GaAs HBT
- ☐ GaAs MESFET ☐ Si CMOS

- ☐ InGaP/HBT
- ☐ GaN HEMT
- ☐ SiGe Bi-CMOS



#### **Functional Block Diagram**

### Package Style: SOT89

#### **Features**

- 300MHz to 3GHz
- +40dBm Output IP3
- 12.5dB Gain at 2.0GHz
- +23dBm P1dB
- 3.0dB Typical Noise Figure at 2.0GHz
- Single 5V Power Supply

#### Ordering Information

RF3315 Broadband High Linearity Amplifier
RF3315PCBA-410 Fully Assembled Evaluation Board (2GHz)
RF3315PCBA-411 Fully Assembled Evaluation Board (900MHz)

RF Micro Devices, Inc. 7628 Thorndike Road Greensboro, NC 27409, USA Tel (336) 664 1233 Fax (336) 664 0454 http://www.rfmd.com

## **Absolute Maximum Ratings**

Parameter	Rating	Unit			
RF Input Power	+20	dBm			
Device Voltage	-0.5 to +6.0	V			
Device Current	250	mA			
Operating Temperature	-40 to +85	°C			
Storage Temperature	-40 to +150	°C			



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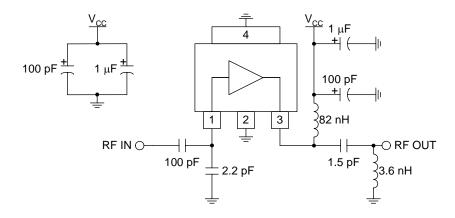
Donomotor	Specification		l lmi4	Condition		
Parameter	Min.	Тур.	Max.	Unit	Condition	
Overall						
AC Specifications (2GHz)					V <sub>CC</sub> =5V, RF <sub>IN</sub> =-10dBm, Freq=2.0GHz, with 2GHz application schematic.	
Frequency	300		3000	MHz		
Gain (Small Signal)	11.0	12.5		dB	F=2GHz	
Input Return Loss		15		dB	F=2GHz	
Output Return Loss		15		dB	F=2GHz	
Output IP3	+36	+40.0		dBm	$F_1 = 1.99 \text{ GHz}, F_2 = 2.00 \text{ GHz}, P_{IN} = -5 \text{ dBm}$	
Output P1dB	+21	+23.0		dBm		
Noise Figure		3.0	4.0	dB		
AC Specifications (900MHz)					V <sub>CC</sub> =5V, RF <sub>IN</sub> =-10dBm, Freq=900MHz, with 900MHz application schematic.	
Frequency	300		3000	MHz		
Gain (Small Signal)	16	18		dB		
Input Return Loss		20		dB		
Output Return Loss		20		dB		
Output IP3	+36	+41		dBm	$F_1 = 900 MHz, F_2 = 901 MHz, P_{IN} = -10 dBm$	
Output P1dB	+23	+25		dBm		
Noise Figure		2.5	3.5	dB		
Thermal					I <sub>CC</sub> =150mA, P <sub>DISS</sub> =770mW. (See Note.)	
Theta <sub>JC</sub>		88		°C/W		
Maximum Measured Junction Temperature at DC Bias Con- ditions		154		°C	T <sub>CASE</sub> =+85°C	
Mean Time To Failure		370		years	T <sub>CASE</sub> =+85°C	
DC Specifications						
Device Voltage	4.5	5.0	5.5	V	I <sub>CC</sub> =150mA	
Operating Current Range	100	150	170	mA	V <sub>CC</sub> =5V	

Note: The RF3315 must be operated at or below 170mA to ensure the highest possible reliability and electrical performance.

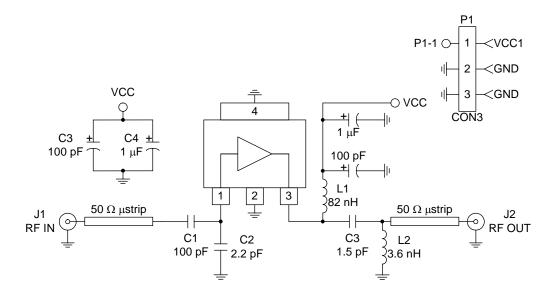
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Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is <u>not</u> internally DC-blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications.	VCC PRF IN O
2	GND	Ground connection.	
3	RF OUT	RF output and bias pin. For biasing, an RF choke is needed. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. See application schematic for configuration and value.	VCC ORF OUT
4	GND	Ground connection.	
Pkg Base	GND	Ground connection.	

## **Typical Application Schematic for 2GHz**

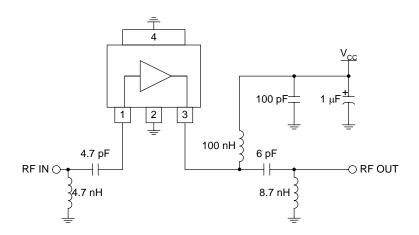


## **Evaluation Board Schematic for 2GHz**

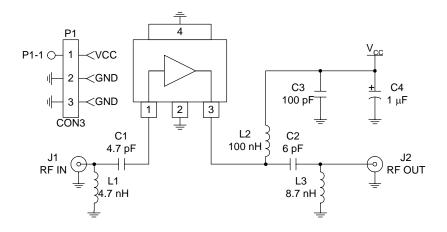


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## **Typical Application Schematic for 900 MHz**



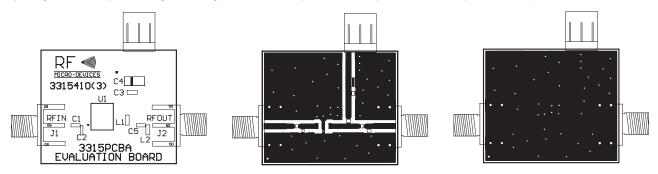
## **Evaluation Board Schematic for 900 MHz**



## Evaluation Board Layout for 1.9GHz Board Size 1.195" x 1.000"

Board Thickness 0.033", Board Material FR-4

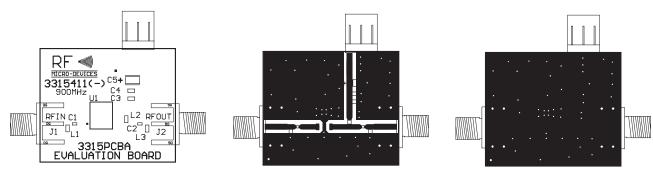
**Note:** A small amount of ground inductance is required to achieve datasheet performance. The necessary inductance may be generated by ensuring that no ground vias are placed directly below the footprint of the part.



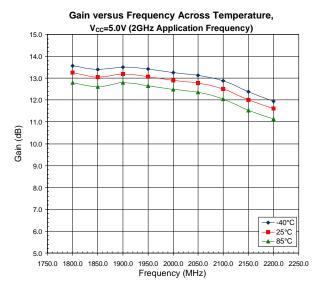
## Evaluation Board Layout for 900 MHz Board Size 1.195" x 1.000"

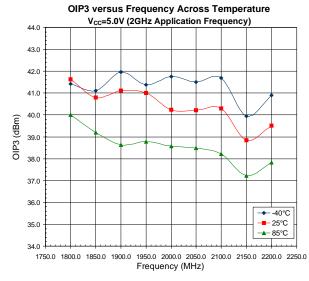
Board Thickness 0.033", Board Material FR-4

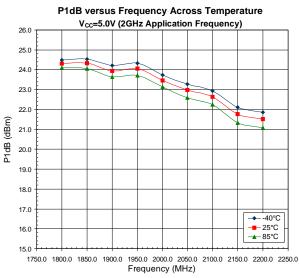
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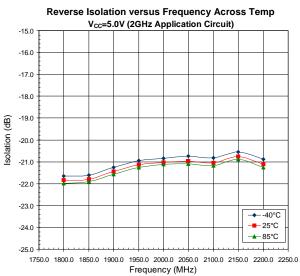


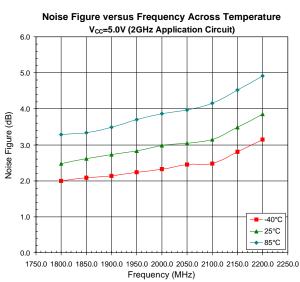
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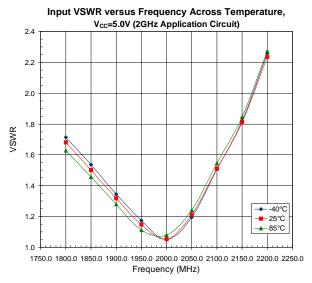


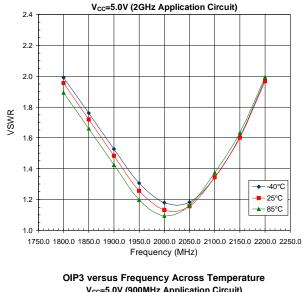




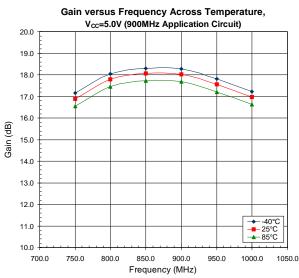


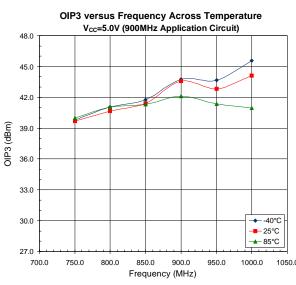


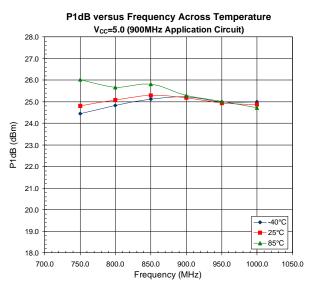


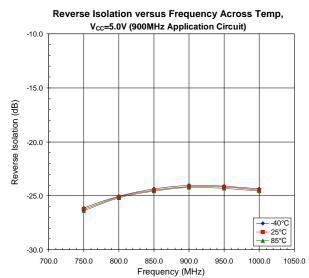


Output VSWR versus Frequency Across Temperature,

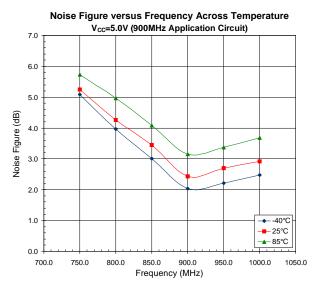


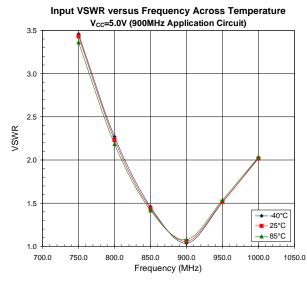


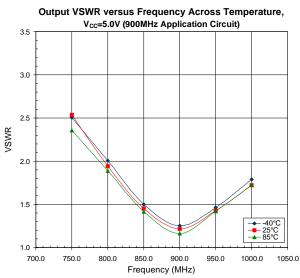


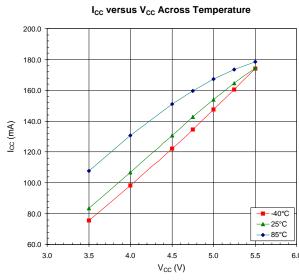


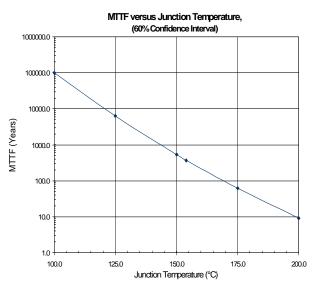
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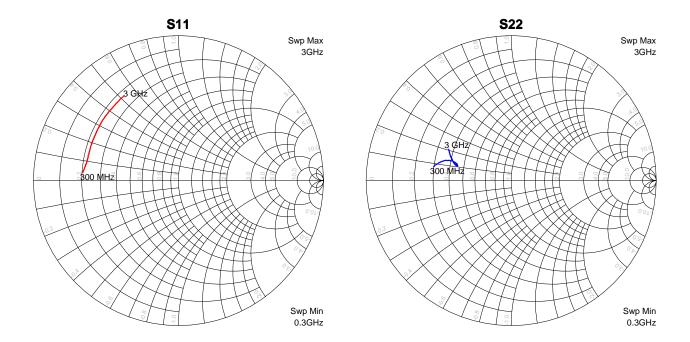












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## **PCB Design Requirements**

#### **PCB Surface Finish**

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

#### **PCB Land Pattern Recommendation**

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

#### **PCB Metal Land Pattern**

 $A = 1.27 \times 0.86 \text{ (mm) Typ.}$ 

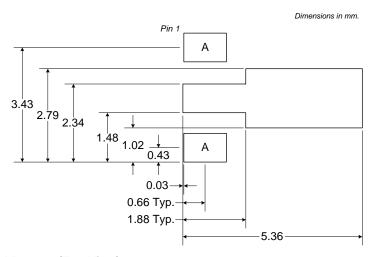


Figure 1. PCB Metal Land Pattern (Top View)

#### **PCB Solder Mask Pattern**

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

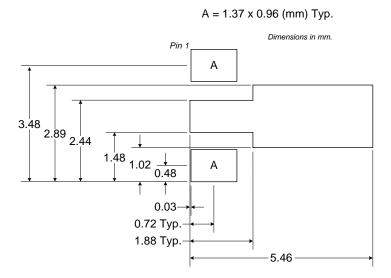


Figure 2. PCB Solder Mask Pattern (Top View)

#### Thermal Pad and Via Design

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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