

MOS INTEGRATED CIRCUIT

μ PD6121

MULTI-PURPOSE REMOTE CONTROL TRANSMITTER IC

CMOS LSI

DESCRIPTION

The μ PD6121 is an infrared remote control transmitter LSI for TV, VCR, stereo components, cassette decks, air conditioners, and other appliances. The 65 536 number customer codes (MAX.) are available by setting external diodes, resistors, and internal MASK ROM.

The transmission code consists of "leader pulse", "16 bit customer code", and "16 bit data code". Using micro-processors for decoder, various applications can be realized.

FEATURES

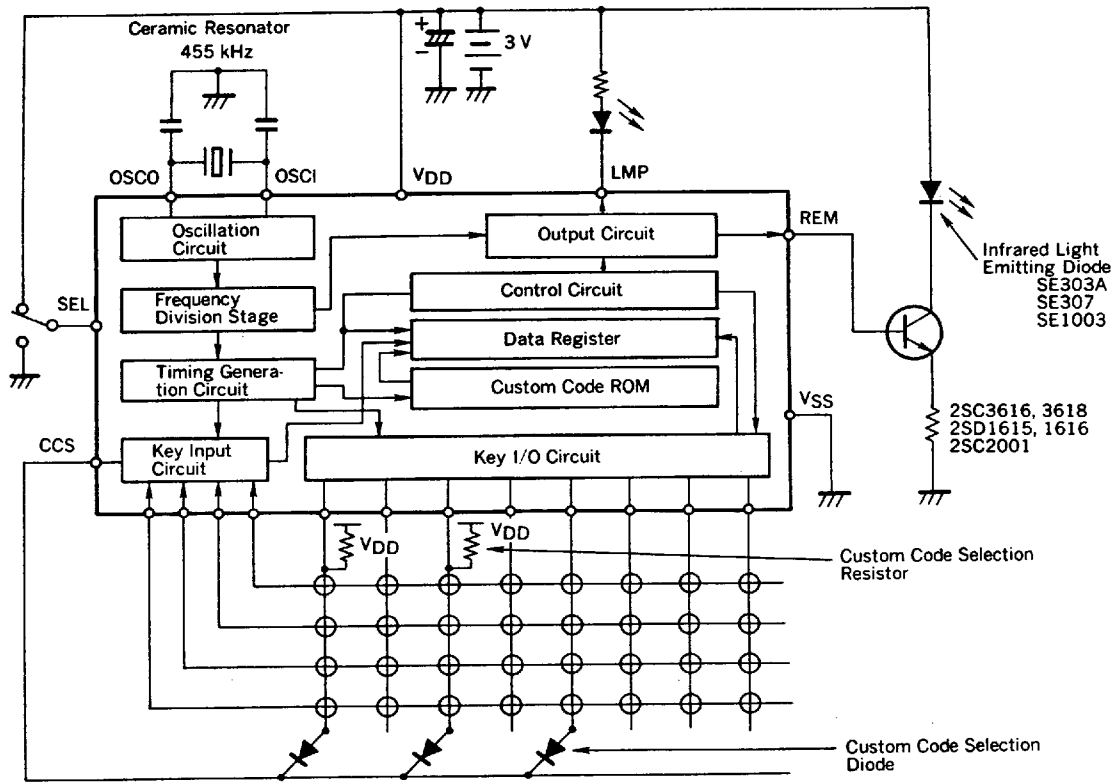
- Low voltage operation $V_{DD} = 2.0$ to 3.3 V
- Low power consumption $I_{DD} < 1 \mu A$ at standby mode
- 32 function keys and 3 double action keys
- 64 + 6 function codes are available. (Using SEL terminal)
- 65 536 customer codes can be selected. (Using external R, Di or internal MASK ROM)
- The transmission format is compatible with μ PD1913, μ PD1943, μ PD6102, μ PD6120, μ PD6122.
- Pin compatible with the μ PD1943.
- NEC standard μ PD6121G-001 (μ PD1943 compatible), μ PD6121G-002 (Built-in customer code ROM)

ORDERING INFORMATION

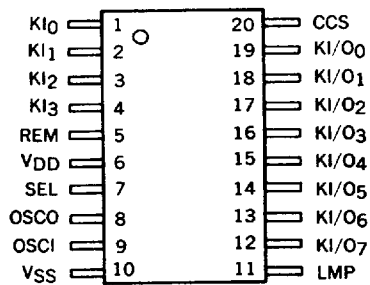
Order Code	Package	Features
μ PD6121G-001	20 pin Plastic SOP (375 mil)	μ PD1943G compatible
μ PD6121G-002	20 pin Plastic SOP (375 mil)	Built-in customer code ROM
μ PD6121G-xxx	20 pin Plastic SOP (375 mil)	Custom

In addition to the above standard products, the μ PD6121G can also be ordered as a custom product with custom codes in mask ROM. Incorporating custom codes in mask ROM reduces the number of external parts required.

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Terminal

1	KI ₀	Key Input 0
2	KI ₁	Key Input 1
3	KI ₂	Key Input 2
4	KI ₃	Key Input 3
5	REM	Remote Output
6	V _{DD}	3 V
7	SEL	Data Select
8	OSCO	Oscillator Output
9	OSCI	Oscillator Input
10	V _{SS}	
11	LMP	Lamp Output
12	KI/O ₇	Key I/O 7
13	KI/O ₆	Key I/O 6
14	KI/O ₅	Key I/O 5
15	KI/O ₄	Key I/O 4
16	KI/O ₃	Key I/O 3
17	KI/O ₂	Key I/O 2
18	KI/O ₁	Key I/O 1
19	KI/O ₀	Key I/O 0
20	CCS	Customer Code Select Input

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PIN DESCRIPTION

(1) Key input and key output pins KI_0 to KI_3 , KI/O_0 to KI/O_7

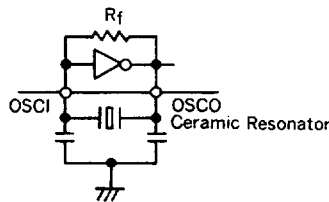
A pull-down resistor is inserted between the key input pins and the V_{SS} pin. If two or more keys are depressed simultaneously, transmission is disabled by the multi-depression prevention circuit. As regards the key transmission priority in the case of two depressions, with simultaneous depressions (± 36 ms) transmission is disabled, and first depression, later remainder priority is used.

When a key is depressed, reading of the custom code and key data code is started, and REM output begins 36 ms later, so that if the key is being depressed during this 36 ms interval one transmission is performed. If a key is held down for 108 ms or longer, consecutive transmissions of the leader code only are performed while the key is depressed. As a key interruption operation can handle an interval of up to 126 ms (from ON to ON). It is possible to configure a system with an extremely fast response time.

(2) Oscillation pins OSC1, OSC0

The oscillation circuit starts to operate when a key is depressed.

Use of a ceramic resonator with a 400 to 500 kHz oscillation is designed for non-adjustment operation.



(3) Power supply pin

The power supply voltage is provided by two 3 V batteries, and covers a wide operating supply voltage range of 2.0 to 3.3 V. Also, as oscillation is stopped except during a key operation, the power supply current is 1 μ A or less.

(4) REM pin

Outputs the transmission code consisting of the leader code, custom code (16 bits) and data code (16 bits) see "Transmission Code" on page 4).

(5) SEL pin

Data code D_7 can be controlled by this pin, allowing 64 kinds of data to be transmitted.

D_7 is set to "0" by connecting the SEL pin to V_{DD} , and to "1" by connecting the SEL pin to V_{SS} .

As the input of this pin is high-impedance, it must be connected to either V_{DD} or V_{SS} .

(6) CCS pin

The custom code can be set by the diodes connected to the CCS pin and the KI/O pins. Connecting the CCS pin and KI/O pins via diodes gives a corresponding custom code of "1", while no connection gives "0".

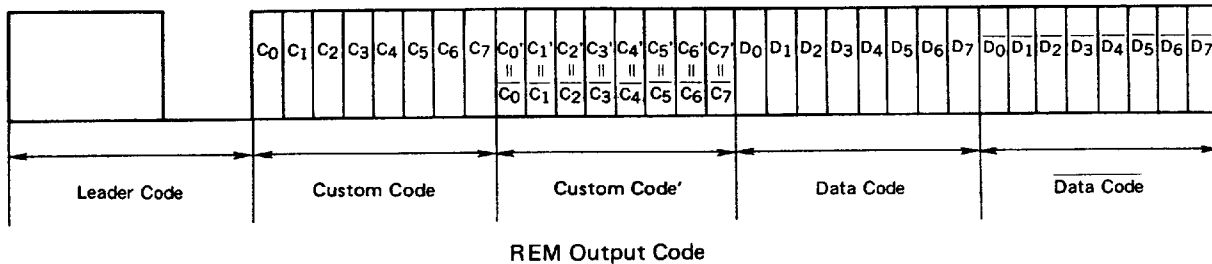
(7) LMP pin

Outputs "L" while the REM pin is outputting a transmission code.

TRANSMISSION CODE

(1) REM output

The transmission code consists of a leader code, 16-bit custom code, and 8-bit data code. The inverse code of the data code is also sent simultaneously, giving a total configuration of 32 bits per transmission.



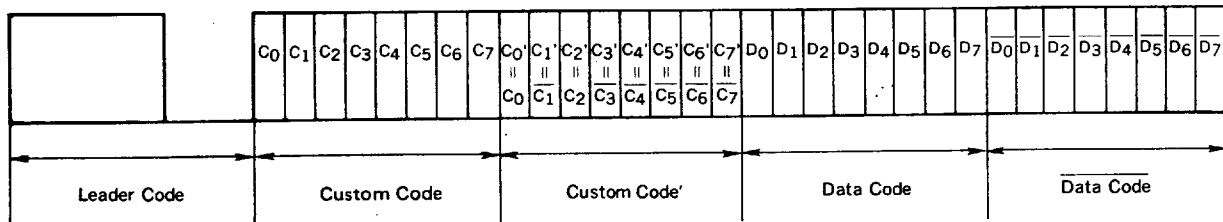
The leader code consists of a 9 ms carrier waveform plus a 4.5 ms OFF waveform, and is used as the leader for the following code. Thus when reception is configured by a microcomputer, the time relationship between reception detection and other processing can be managed efficiently. The code uses the PPM (Pulse Position Modulation) method, with "1" and "0" differentiated by the time between pulses. Each code consists of 8 bits, and simultaneous transmission of the inverse code allows configuration of a system with an extremely low error rate.

(2) Custom code extension

As with the μ PD1943G, the above output codes can be obtained by custom code selection using diodes only.

To further extend the number of custom codes, 200 k Ω pull-up resistors are added to pins KI/O₀ through KI/O₇, and the bit corresponding to a pin from among the custom code' outputs is output without being inverted.

By encoding the custom code' part, 256 times the number of μ PD1943G custom codes, i.e. 65 536, can be selected.



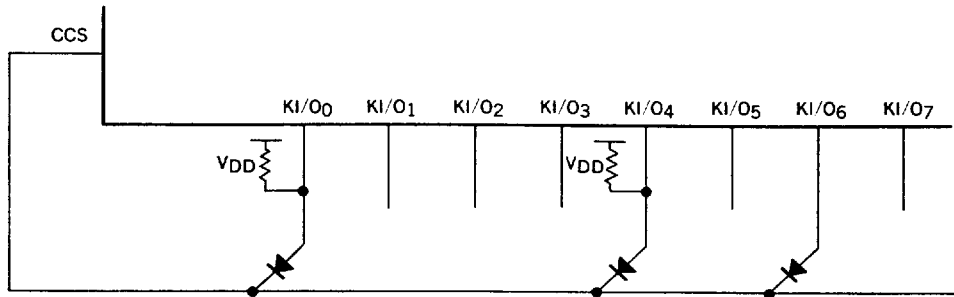
*: Pull-up resistor added to pins KI/O₀ and KI/O₂.
C₀ and C₂ output without inversion (non-inverted bits).

(3) Custom code

The REM output custom code can be set in any of 65 536 ways by means of the diodes attached to the CCS (Custom Code Select) pin and the KI/O pins and the pull-up resistors attached to the KI/O pins. When a code other than code 00000000 (no diode connection) is used, please contact NEC since custom codes are managed by NEC to prevent errors between various systems.

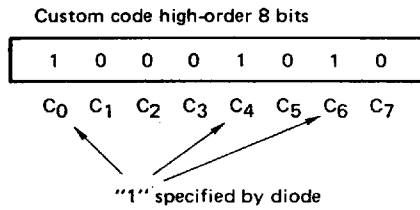
Setting Example

(Configuration example)



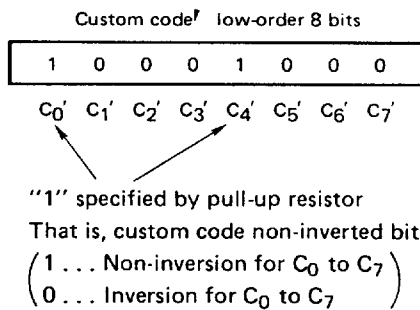
The custom code high-order 8 bits are determined by the diode attached to the CCS pin and KI/O pins.

Set custom code



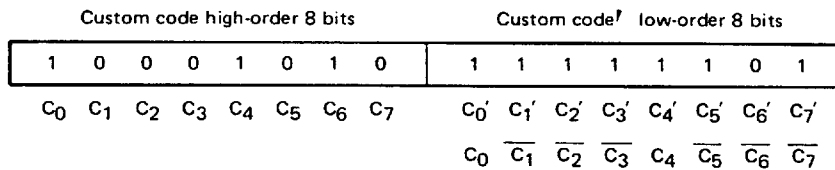
The custom code^l low-order 8 bits are determined by the pull-up resistor attached to the KI/O pins.

Set custom code



When the above setting is made, the output custom code is as follows:

Custom code



(4) Custom code mask ROM specification

The custom code can also be set by mask ROM. When the mask ROM specification is used the custom code can be set without the connection of external diodes and resistors, and by combining external diodes and resistors with mask ROM it is possible to output a code with different contents from those set by the mask ROM. When mask ROM specification is used, (Ver. I) or (Ver. II) can be selected.

	Custom Code High-Order 8 Bits	Custom Code' Low-Order 8 Bits
Ver. I	Determined by logical OR of internal ROM1 and external diode positions.	Determined by logical OR of internal ROM2 and external pull-up resistor positions
Ver. II	C ₀ , C ₁ , C ₂ : Determined by wiring one of pins KI/O ₀ thru KI/O ₇ to CCS pin. C ₃ thru C ₇ : Determined by internal ROM3 and absence/presence of KI/O ₆ & KI/O ₇ external pull-up resistors.	Determined by logical OR of internal ROM2 and external pull-up resistor (KI/O ₀ thru KI/O ₅) positions.

* Standard product μ PD6121G-001 uses the Ver. I specification, and is pin-compatible with the μ PD1943G. When using this as pin-compatible with the μ PD1943G, the following points should be noted:

- (1) The SEL pin (pin 7) should be connected to V_{DD}.
- (2) The capacity of the capacitor connected to the oscillation pins (OSCO pin 8, and OSC1 pin 9) should be changed. (See page 18.)

Internal ROM is set as follows:

ROM1								ROM2							
Custom code high-order 8 bits								Custom code' low-order 8 bits							
0 0 0 0 0 0 0 0								0 0 0 0 0 0 0 0							
C ₀	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇	C ₀ '	C ₁ '	C ₂ '	C ₃ '	C ₄ '	C ₅ '	C ₆ '	C ₇ '

* Standard product μ PD6121G-002 uses the Ver. II specification.

Internal ROM is set as follows:

ROM3

C₇, C₆, C₅, C₄, C₃ of Custom Code High-Order 8 Bits

Pull-Up Resistor

ROM3	C ₇	C ₆	C ₅	C ₄	C ₃	KI/O ₆	KI/O ₇
ROM3 to ROM0	0	0	0	0	0	No	No
ROM3 to ROM1	1	0	0	1	1	No	Yes
ROM3 & ROM2	1	0	0	0	0	Yes	No
ROM3 & ROM3	1	1	1	0	1	Yes	Yes

ROM2

Custom code¹ low-order 8 bits

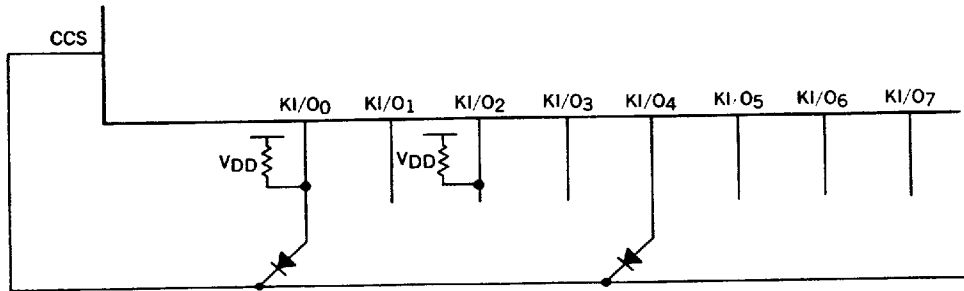
0	0	0	0	0	0	0	0
C ₀	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇

(Ver. II)

Internal custom code ROM1 and ROM2 (total 16 bits) are effective, with 8 bits being the part (ROM1) corresponding to the external diodes, and 8 bits the part (ROM2) corresponding to the external pull-up resistors.

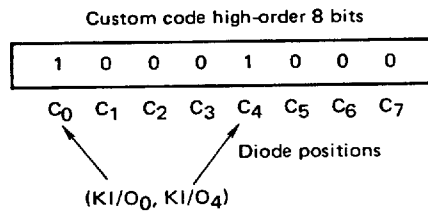
Setting Example

Configuration example

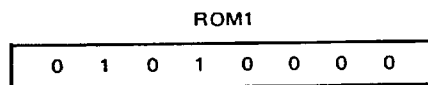


The custom code high-order 8 bits are determined by the logical OR of the external diode positions and internal ROM1.

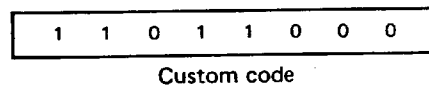
External setting (see above figure)



Internal ROM1 (setting example)

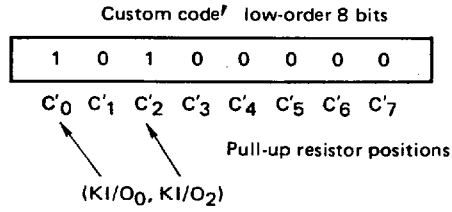


External setting V Internal ROM1

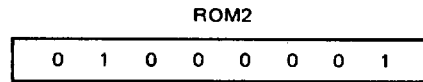


The custom code' low-order 8 bits are determined by the logical OR of the external pull-up resistor positions and internal ROM2.

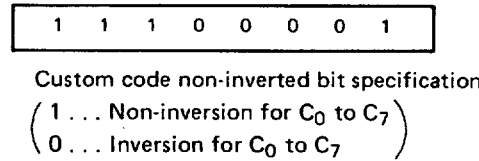
External setting (see above figure)



Internal ROM2 (setting example)

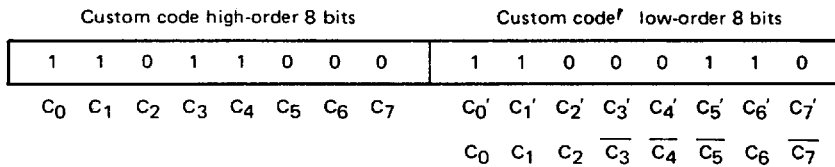


External setting V Internal ROM2



When pull-up resistors, diodes and ROM1/ROM2 and set, as mentioned before, the output custom code is as follows :

Custom code



*: The code to be transmitted is output LSB-first.

(Ver. II)

With Ver. II, the CCS pin does not have the function of reading the external diodes.

Internal custom code ROM2 and ROM3 (total 28 bits) are effective, with 20 bits being the part (ROM3) for setting the 4 channels of custom code C_7 , C_6 , C_5 , C_4 and C_3 as 5 bits each, and 8 bits being the part (ROM2) corresponding to the external pull-up resistors (excluding KI/O_6 and KI/O_7).

With Ver. II, 0/1 allocation to C_2 , C_1 and C_0 of the custom code high-order bits is set as shown in the following table according to the pin connection status of KI/O_0 through KI/O_7 .

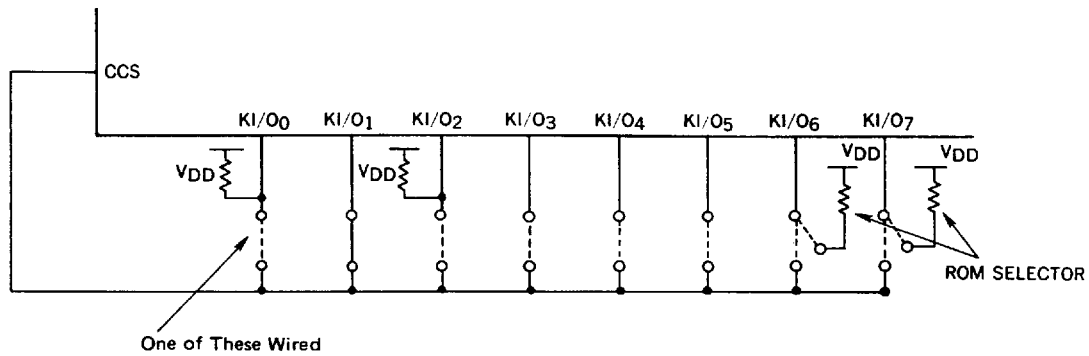
CCS-	C_2	C_1	C_0
KI/O_0	0	0	0
KI/O_1	0	0	1
KI/O_2	0	1	0
KI/O_3	0	1	1
KI/O_4	1	0	0
KI/O_5	1	0	1
KI/O_6	1	1	0
KI/O_7	1	1	1

When CCS pin is open

$(C_2 C_1 C_0) = (0, 0, 0)$

Setting Example

Configuration example



Bits C_2, C_1, C_0 of the custom code high-order 8 bits are determined by wiring between the CCS pin and pins KI/O₀ thru KI/O₇, and thus in the above figure is:

1	0	0
C_0	C_1	C_2

Bits C_7, C_6, C_5, C_4, C_3 of the custom code high-order 8 bits are determined by selection by the pull-up resistors added to KI/O₆ & KI/O₇ among the 4 channels of internal ROM3.

Pull-Up Resistors

KI/O ₆	KI/O ₇	ROM3	C ₇	C ₆	C ₅	C ₄	C ₃
No	No	ROM3 to ROM0	1	0	1	1	0
No	Yes	ROM3 to ROM1	0	0	1	1	1
Yes	No	ROM3 & ROM2	1	1	0	1	1
Yes	Yes	ROM3 & ROM3	1	1	1	1	1

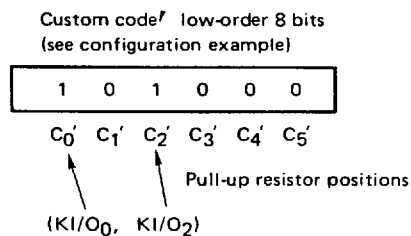
(Setting example)

In the above figure, C_3 thru C_7 of the custom code high-order 8 bits are:

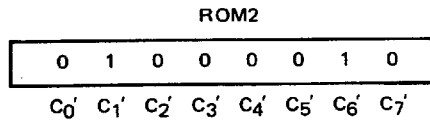
1	1	0	1	1
C_3	C_4	C_5	C_6	C_7

The custom code⁷ low-order 8 bits are determined by the logical OR of the KI/O₀ thru KI/O₅ external pull-up resistor positions and internal ROM2.

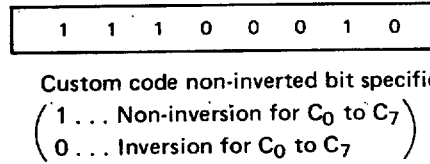
External setting



Internal ROM2 (setting example)

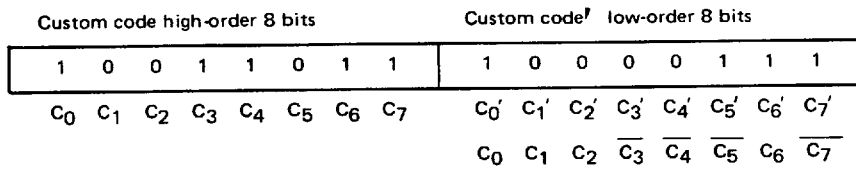


External setting V Internal ROM2



When pull-up resistors, wiring and ROM2, ROM3 are set, as mentioned before, the output custom code is as follows:

Custom code



* : The code to be transmitted is output LSB-first.

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Key Data Code

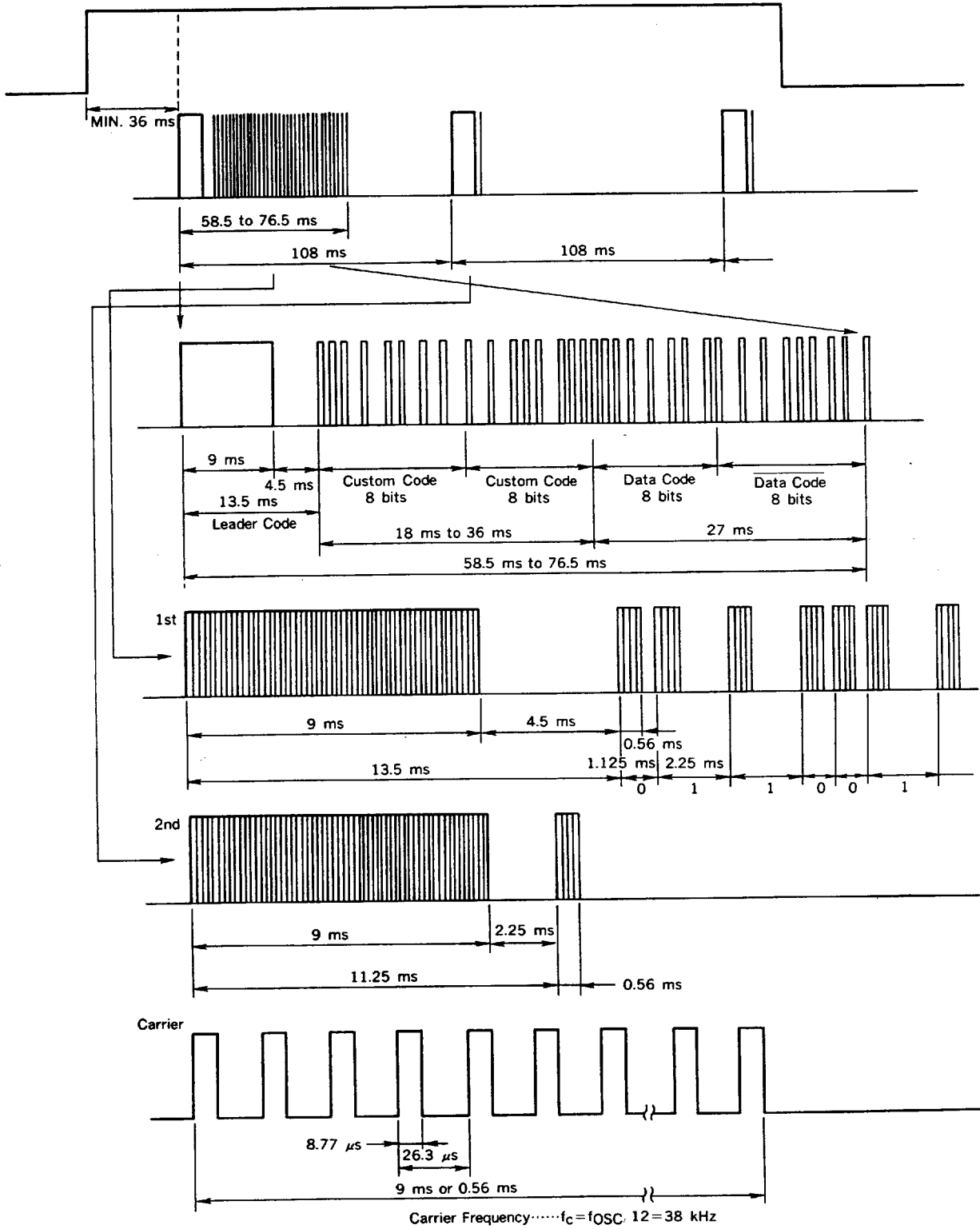
KEY	CONNECTION					DATA CODE								NOTES
	KI ₀	KI ₁	KI ₂	KI ₃	KI/O	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	
K 1	*				KI/O ₀	0	0	0	0	0	0	0	0/1	
K 2		*				1	0	0	0	0	0	0	0/1	
K 3			*			0	1	0	0	0	0	0	0/1	
K 4				*		1	1	0	0	0	0	0	0/1	
K 5	*				KI/O ₁	0	0	1	0	0	0	0	0/1	N/A for μ PD1913C μ PD6120C
K 6		*				1	0	1	0	0	0	0	0/1	
K 7			*			0	1	1	0	0	0	0	0/1	
K 8				*		1	1	1	0	0	0	0	0/1	
K 9	*				KI/O ₂	0	0	0	1	0	0	0	0/1	
K10		*				1	0	0	1	0	0	0	0/1	
K11			*			0	1	0	1	0	0	0	0/1	
K12				*		1	1	0	1	0	0	0	0/1	
K13	*				KI/O ₃	0	0	1	1	0	0	0	0/1	N/A for μ PD1913C μ PD6120C
K14		*				1	0	1	1	0	0	0	0/1	
K15			*			0	1	1	1	0	0	0	0/1	
K16				*		1	1	1	1	0	0	0	0/1	
K17	*				KI/O ₄	0	0	0	0	1	0	0	0/1	
K18		*				1	0	0	0	1	0	0	0/1	
K19			*			0	1	0	0	1	0	0	0/1	
K20				*		1	1	0	0	1	0	0	0/1	
K21	*				KI/O ₅	0	0	1	0	1	0	0	0/1	
K22		*				1	0	1	0	1	0	0	0/1	
K23			*			0	1	1	0	1	0	0	0/1	
K24				*		1	1	1	0	1	0	0	0/1	
K25	*				KI/O ₆	0	0	0	1	1	0	0	0/1	
K26		*				1	0	0	1	1	0	0	0/1	
K27			*			0	1	0	1	1	0	0	0/1	
K28				*		1	1	0	1	1	0	0	0/1	
K29	*				KI/O ₇	0	0	1	1	1	0	0	0/1	N/A for μ PD1913C μ PD6120C
K30		*				1	0	1	1	1	0	0	0/1	
K31			*			0	1	1	1	1	0	0	0/1	
K32				*		1	1	1	1	1	0	0	0/1	

N/A = Not Available

Remote Output Waveforms

KEY Input

Ex. $f_{OSC} = 455 \text{ kHz}$



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9. Double Key Operation

When more than two keys except K21 + K22, K21 + K23 and K21 + K24 are depressed at the same time, the transmission output stops.

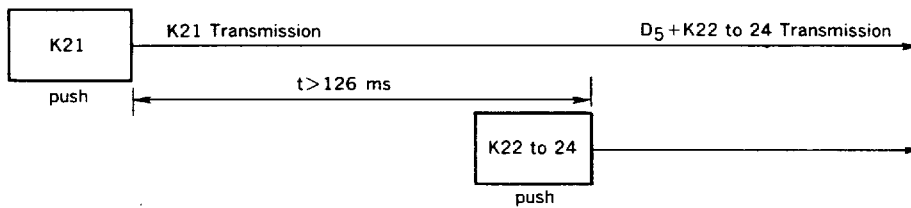
Double key operation is useful for tape deck recording operation.

Double key operation form are following.

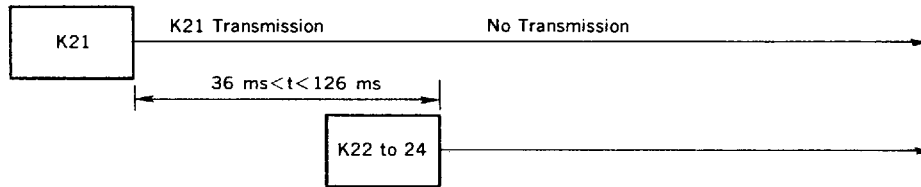
Double Key Operation

KEY	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
K21 + K22	1	0	1	0	1	1	0	0/1
K21 + K23	0	1	1	0	1	1	0	0/1
K21 + K24	1	1	1	0	1	1	0	0/1

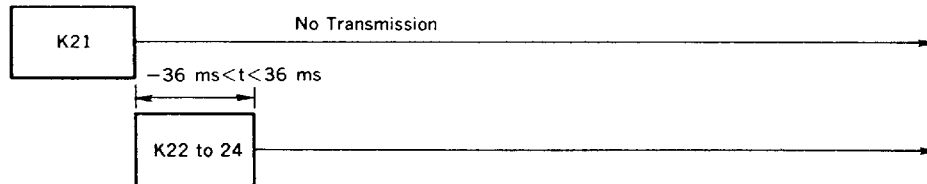
(a) Operation



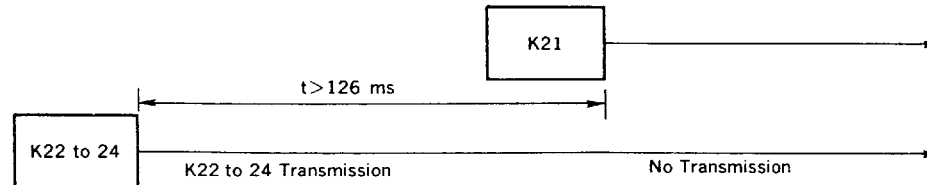
(b) No operaiton



(c) No operation



(d) No operation



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10. Customer Code ROM Format

This LSI has customer code table ROM on the chip. So users can generate customer codes without external parts. The customer code ROM format is following.

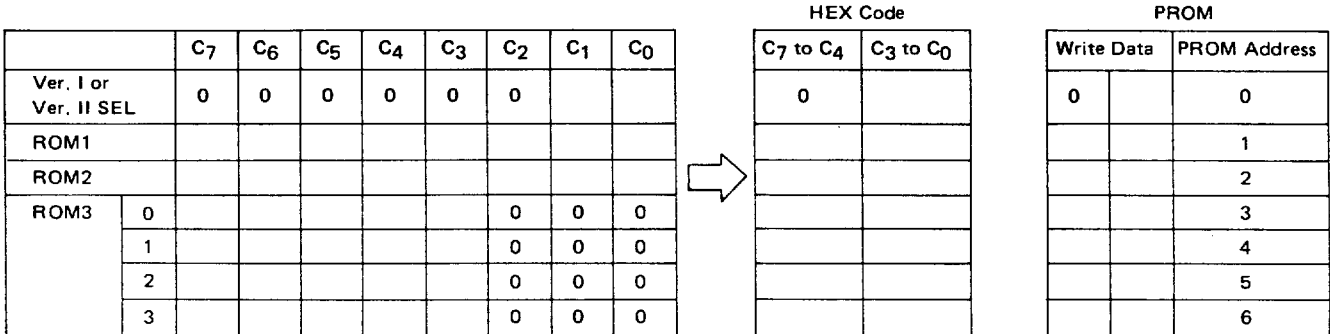
		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
Ver. 1 or 2 SEL		0	0	0	0	0	0	1/0	1/0		
ROM1		1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	ROM PULL	SEL UP
ROM2		1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	KI/O ₆	KI/O ₇
ROM3	0	1/0	1/0	1/0	1/0	1/0	0	0	0	NO	NO
	1	1/0	1/0	1/0	1/0	1/0	0	0	0	NO	YES
	2	1/0	1/0	1/0	1/0	1/0	0	0	0	YES	NO
	3	1/0	1/0	1/0	1/0	1/0	0	0	0	YES	YES

- 1) Ver. 1 or Ver. 2 selection Ver. 1 = 01_H, Ver. 2 = 02_H
- 2) When a user selects Ver. 1, ROM1 is available for the customer code (C₇ to C₀) selection.
- 3) ROM2 is available for the customer code' (C₇' to C₀') selection.
- 4) When a user selects Ver. 2, ROM3 is available for the customer code (C₇ to C₃) selection. And a user can select ROM3 -0, ROM3-1, ROM3-2 or ROM3-3 by the KI/O₆ and KI/O₇ pull up resistances.

Mask ROM Ordering Procedure

The ordering medium for custom code mask ROM is PROM.

- Ordering medium PROM
(μ PD2716, μ PD2732A, μ PD2764, μ PD27128, μ PD27256 and equivalent products)
- Quantity 3
- Data storage method ① Ver. I or Ver. II selection is stored in PROM address 0.
 ② ROM1 data is stored in PROM address 1.
 ③ ROM2 data is stored in PROM address 2.
 ④ ROM3 data is stored in PROM address 3 to 6.



- NOTE 1:** When Ver. I is selected, ROM1 and ROM2 data is stored in PROM address 1 and address 2, and 00H is stored as ROM3 data (addresses 3 to 6).
- 2:** When Ver. II is selected, ROM2 and ROM3 to 6, and 00H is stored as ROM1 data (address 1).

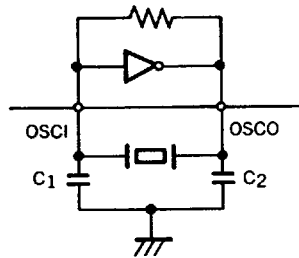
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The μ PD6121G oscillation circuit is designed for use of a 400 kHz or 500 kHz ceramic resonator, but there may be mutual influence between variations in the IC and the ceramic resonator resulting in abnormal oscillation.

The following table shows the recommended values of C_1 and C_2 when using the μ PD6121G. These recommended values have been obtained through the cooperation of the ceramic resonator manufacturers.

Recommended Ceramic Resonators

Manufacturer	Product	External Capacitance (pF)		Oscillation Voltage Range (V)	
		C_1	C_2	MIN.	MAX.
Murata Mfg. Co., Ltd.	CSB455E	220	220	2.0	3.3
	CSB480E	220	220	2.0	3.3
Toko, Inc.	P46CRK455-M11	120	300	2.0	3.3
Kyocera Corp.	KBR-455BTLR	220	220	2.0	3.3

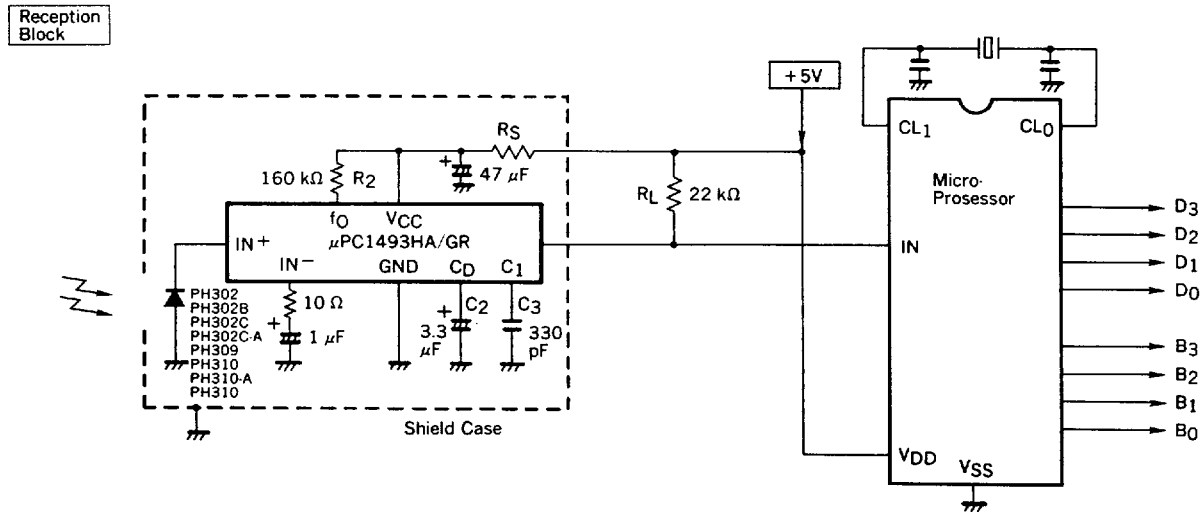
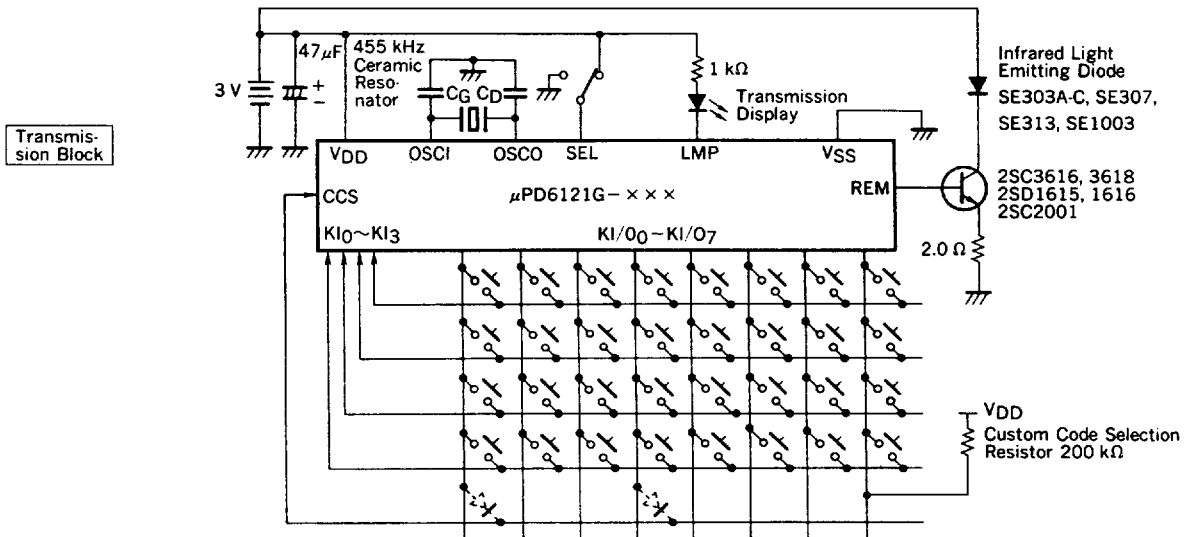


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Sample Application Circuit

In this example a 4-bit single-chip microcomputer is used for reception. The microcomputer is not used exclusively for reception; this can be included among other functions.



The application circuits and circuit constants shown in this document are not designed for volume production with parts variance and temperature characteristics taken into consideration. NEC Corporation cannot accept liability for patent infringements in connection with these circuits.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Supply Voltage	V_{DD}	6.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD}	V
Power Dissipation	P_d	250	mW
Operating Temperature	T_{opt}	-20 to +75	$^\circ\text{C}$
Storage Temperature	T_{stg}	-40 to +125	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	2.0	3.0	3.3	V
Oscillation Frequency	f_{osc}	400	455	500	kHz
Input Voltage	V_{IN}	0		V_{DD}	V
Custom code select Pull up Resistance	R_{up}	160	200	240	k Ω

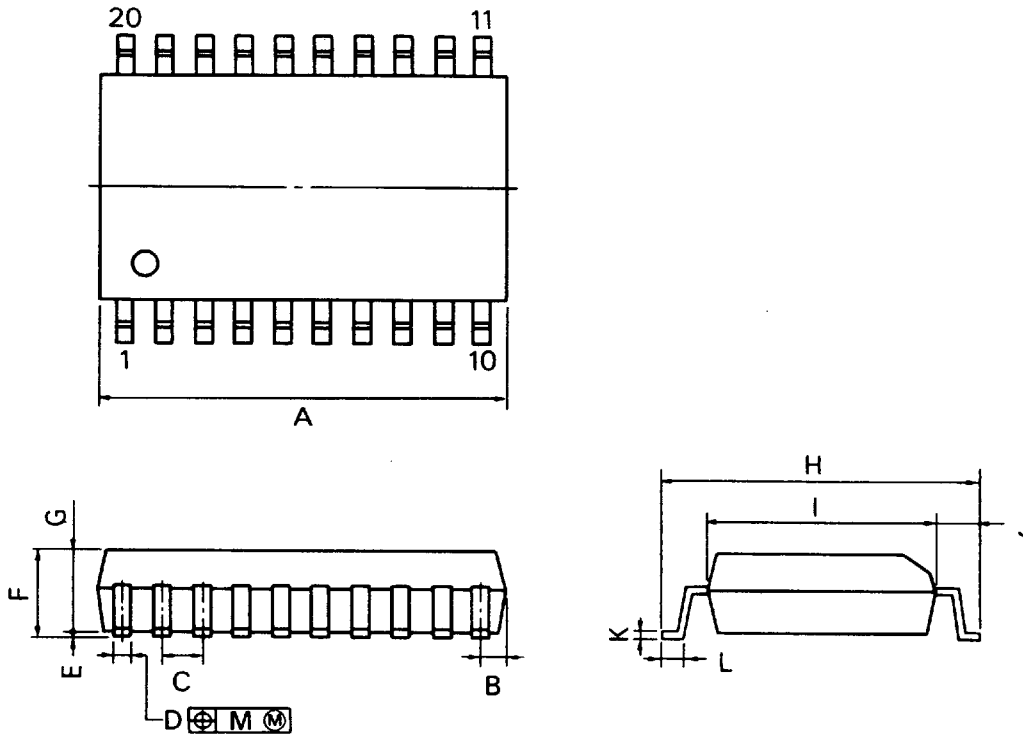
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	V_{DD}	2.0	3.0	3.3	V	
Current Consumption 1	I_{DD1}		0.1	1.0	mA	$f_{osc} = 455\text{ kHz}$
Current Consumption 2	I_{DD2}			1.0	μA	$f_{osc} = \text{STOP}$
REM High Level Output Current	I_{OH1}	-5.0	-8.0		mA	$V_o = 1.5\text{ V}$
REM Low Level Output Current	I_{OL1}	15	30		μA	$V_o = 0.3\text{ V}$
LMP High Level Output Current	I_{OH2}	-15	-30		μA	$V_o = 2.7\text{ V}$
LMP Low Level Output Current	I_{OL2}	1	1.5		mA	$V_o = 0.3\text{ V}$
KI High Level Input Current	I_{IH1}	10		30	μA	$V_{IN} = 3.0\text{ V}$
KI Low Level Input Current	I_{IL1}			-0.2	μA	$V_{IN} = 0\text{ V}$
KI High Level Input Voltage	V_{IH1}	$0.7 V_{DD}$		V_{DD}	V	
KI Low Level Input Voltage	V_{IL1}	0		$0.3 V_{DD}$	V	
KI/O High Level Input Voltage	V_{IH2}	1.3		V_{DD}	V	
KI/O Low Level Input Voltage	V_{IL2}	0		0.4	V	
KI/O High Level Input Current	I_{IH2}	2		7	μA	$V_{IN} = 3.0\text{ V}$
KI/O Low Level Input Current	I_{IL2}			-0.2	μA	$V_{IN} = 0\text{ V}$
KI/O High Level Output Current	I_{OH3}	1.0		2.5	mA	$V_o = 2.5\text{ V}$
KI/O Low Level Output Current	I_{OL3}	35		100	μA	$V_o = 1.7\text{ V}$
CCS High Level Input Voltage	V_{IH3}	1.1			V	
CCS High Level Input Current	I_{IH3}			0.2	μA	Pull up $V_{IN} = 3.0\text{ V}$
CCS Low Level Input Current	I_{IL3}	-3		-8	μA	Pull up $V_{IN} = 0\text{ V}$
CCS High Level Input Current	I_{IH4}	10		30	μA	Pull down $V_{IN} = 3.0\text{ V}$
CCS Low Level Input Current	I_{IL4}			-0.2	μA	Pull down $V_{IN} = 0\text{ V}$

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20PIN PLASTIC SOP (375 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P20GM-50-375B-1

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{+0.10} _{-0.06}	0.016 ^{+0.004} _{-0.003}
E	0.1 ^{+0.2} _{-0.1}	0.004 ^{+0.008} _{-0.004}
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ^{+0.3}	0.406 ^{+0.012} _{-0.013}
I	7.2	0.283
J	1.6	0.063
K	0.15 ^{+0.10} _{-0.06}	0.006 ^{+0.004} _{-0.002}
L	0.8 ^{+0.2}	0.031 ^{+0.008} _{-0.006}
M	0.12	0.005

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RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD6121G

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature : 230 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow process : 1, Exposure limit* : None	IR30-00
VPS	Peak package's surface temperature : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow process : 1, Exposure limit* : None	VP15-00
Wave soldering	Solder temperature : 260 °C or below. Flow time : 10 seconds or below. Number of flow process : 1, Exposure limit* : None	WS60-00
Partial heating method	Terminal temperature : 300 °C or below, Flow time : 10 seconds or below. Exposure limit* : None	

* : Exposure limit before soldering after dry-pack package is opened.
Storage conditions : 25 °C and relative humidity at 65 % less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

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