



Weltrend Semiconductor, Inc.
WT8801T Specification

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Ver. 1.0
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1. Features

Digital Input Support

- 24 bit RGB input
- 8/16 bit YUV 4:2:2 Video input support
- Built-in YUV to RGB color space converter
- DDWG/DVI1.0 compliant

High Quality Scaling Engine

- Fully programmable zoom ratios
- Independent Horizontal/Vertical scale
- High quality scaling down capability, for 1152 & 1280 to 1024 down scale
- Advanced de-interlacing algorithm for digital YUV video
- Enhanced sharpness filter for better text support
- Spatial color dithering algorithm (random mode or fuzzy mode) to 16.7 million color
- Digital Brightness/Contrast adjustment

Output Panel Support

- Single (18/24) or Dual (36/48) pixel output
- Support Multiple TFT LCD Panel
- Support VGA/SVGA/XGA/SXGA display resolution
- Programmable output driving capacity for 8mA/16mA/24mA

Build-in Programmable Panel Timing Controller (TCON)

- Direct connect to commercial row/column driver IC
- Support dual bus dual port, single bus single/dual port configurations
- Independent data swapping of even/odd pixels, red and blue pixels, and MSB and LSB

OSD and Gamma Correction Support

- Fully programmable OSD Engine
- Downloadable font storage for internal OSD
- Support 384 plus 128 Multi-Color fonts
- User programmable 10-bit Gamma table
- Support sRGB for color management

On-chip Micro-controller

- Requires no external micro-controller
- 12 general purpose inputs/outputs (GPIO) available
- Build in IR control registers for IR function.
- Build in 64k flash memory for program and 32k flash memory for OSD font



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- In System Programming (ISP)

Display Synchronization

- Advanced Input mode detection
- Automatic Input Edge Adjustment
- Automatic Input Phase Calibration

Low System Cost Solution

- Plug and Display, support VGA mode up to 1280x1024 @ 75Hz
- 2-wire I²C serial interface for EEPROM and Micro-controller
- Glue less interface to external TMDS chip
- Power Management support

Electrical/Physical Specification

- 3.3V pad power supply with 5V I/O tolerant, 2.5V core power supply
- 160 pin PQFP Package



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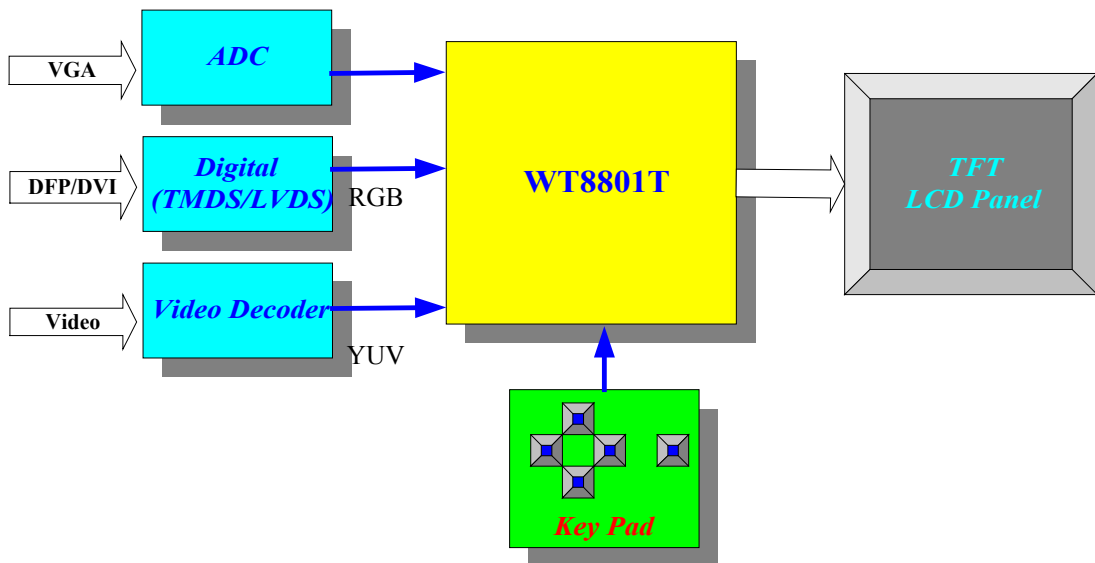
2. Overview

The WT8801T LCD (Liquid Crystal Display) Monitor Controller is an input format converter for the TFT-LCD Panels or LCD-TV applications. It accepts analog RGB signals from PC, YUV from digital video decoder or digital RGB graphics from PanelLink TMDS receiver and transforms these signals to TFT-LCD panel to display. The WT8801T performs image scaling on 24bit RGB or YUV data stream and feeds these scaled pixels to the output LCD panel. When displaying the image, instead of using external memory chips for scaling and temporary storage, the chip is using embedded line buffers. This chip also embedded MCU and flash memory such that the total system cost can be kept to minimum.

In order to provide the plug-n-display, the chip also performs functions like automatic input mode detection and automatic phase calibration. This is designed to keep the sampling clock of ADC is synchronized with the incoming data so that the final image in the LCD panel is free of distortion. The chip also provides the circuitry for contrast / brightness adjustment and gamma tables for intensity correction.

Figure 1 shows a system configuration for the chip.

WT8801T System Block Diagram





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3. Signal Definitions

3.1 Pin Listing & Description

Symbol	Pin No	I/O	Description
GND	1	G	System Ground
RESETB	2	I	System Reset signal (Active Low)
OVR	3	I	External OSD Red signal
OVG	4	I	External OSD Green signal
OVB	5	I	External OSD Blue signal
OVI	6	I	External OSD Intensity signal
OVFB	7	I	Overlay enable from external OSD chip
TMS0	8	I	Test Mode Selection 0, N/C in Normal Mode
GND	9	G	System Ground
N/C	10	N/C	No Connection
V25	11	P	+2.5V Power Supply
GND	12	G	System Ground
N/C	13	N/C	No Connection
V25	14	P	+2.5V Power Supply
GND	15	G	System Ground
N/C	16	N/C	No Connection
TMS1	17	I	Test Mode Selection 1, N/C in Normal Mode
PANEL_R0	18	O	Panel Red Output Data Bit 0
PANEL_R1	19	O	Panel Red Output Data Bit 1
PANEL_R2	20	O	Panel Red Output Data Bit 2
PANEL_R3	21	O	Panel Red Output Data Bit 3
PANEL_R4	22	O	Panel Red Output Data Bit 4
PANEL_R5	23	O	Panel Red Output Data Bit 5
V25	24	P	+2.5V Power Supply
V33	25	P	+3.3V Power Supply
PANEL_R6	26	O	Panel Red Output Data Bit 6
PANEL_R7	27	O	Panel Red Output Data Bit 7
PANEL_G0	28	O	Panel Green Output Data Bit 0
PANEL_G1	29	O	Panel Green Output Data Bit 1
PANEL_G2	30	O	Panel Green Output Data Bit 2
PANEL_G3	31	O	Panel Green Output Data Bit 3
PANEL_G4	32	O	Panel Green Output Data Bit 4
PANEL_G5	33	O	Panel Green Output Data Bit 5
SDA	34	I/O	I2C Bus Data Line
SCL	35	I	I2C Bus Clock Line
V25	36	P	+2.5V Power Supply
PANEL_G6	37	O	Panel Green Output Data Bit 6
V33	38	P	+3.3V Power Supply
PANEL_G7	39	O	Panel Green Output Data Bit 7
PANEL_B0	40	O	Panel Blue Output Data Bit 0



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Symbol	Pin No	I/O	Description
GND	41	G	System Ground
PANEL_B1	42	O	Panel Blue Output Data Bit 1
PANEL_B2	43	O	Panel Blue Output Data Bit 2
PANEL_B3	44	O	Panel Blue Output Data Bit 3
PANEL_B4	45	O	Panel Blue Output Data Bit 4
PANEL_B5	46	O	Panel Blue Output Data Bit 5
PANEL_B6	47	O	Panel Blue Output Data Bit 6
PANEL_B7	48	O	Panel Blue Output Data Bit 7
VGA_HS	49	I	VGA Horizontal Sync
V33	50	P	+3.3V Power Supply
PDE	51	O	Panel Data Enable
PVS	52	O	Panel Vertical Sync
PHS	53	O	Panel Horizontal Sync
PCK	54	O	Panel Clock
N/C	55	N/C	No Connection
PANEL_R8	56	O	Panel Red Output Data Bit 8
PANEL_R9	57	O	Panel Red Output Data Bit 9
PANEL_R10	58	O	Panel Red Output Data Bit 10
V25	59	P	+2.5V Power Supply
PANEL_R11	60	O	Panel Red Output Data Bit 11
PANEL_R12	61	O	Panel Red Output Data Bit 12
PANEL_R13	62	O	Panel Red Output Data Bit 13
V33	63	P	+3.3V Power Supply
PANEL_R14	64	O	Panel Red Output Data Bit 14
PANEL_R15	65	O	Panel Red Output Data Bit 15
PANEL_G8	66	O	Panel Green Output Data Bit 8
PANEL_G9	67	O	Panel Green Output Data Bit 9
PANEL_G10	68	O	Panel Green Output Data Bit 10
PANEL_G11	69	O	Panel Green Output Data Bit 11
PANEL_G12	70	O	Panel Green Output Data Bit 12
PANEL_G13	71	O	Panel Green Output Data Bit 13
PANEL_G14	72	O	Panel Green Output Data Bit 14
PANEL_G15	73	O	Panel Green Output Data Bit 15
V33	74	P	+3.3V Power Supply
PANEL_B8	75	O	Panel Blue Output Data Bit 8
PANEL_B9	76	O	Panel Blue Output Data Bit 9
PANEL_B10	77	O	Panel Blue Output Data Bit 10
PANEL_B11	78	O	Panel Blue Output Data Bit 11
PANEL_B12	79	O	Panel Blue Output Data Bit 12
PANEL_B13	80	O	Panel Blue Output Data Bit 13



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Symbol	Pin No	I/O	Description
GND	81	G	System Ground
PANEL_B14	82	O	Panel Blue Output Data Bit 14
PANEL_B15	83	O	Panel Blue Output Data Bit 15
V33	84	P	+3.3V Power Supply
INPUT_B7	85	I	Input Blue Data Bit 7
INPUT_B6	86	I	Input Blue Data Bit 6
INPUT_B5	87	I	Input Blue Data Bit 5
INPUT_B4	88	I	Input Blue Data Bit 4
INPUT_B3	89	I	Input Blue Data Bit 3
INPUT_B2	90	I	Input Blue Data Bit 2
INPUT_B1	91	I	Input Blue Data Bit 1
INPUT_B0	92	I	Input Blue Data Bit 0
V33	93	P	+3.3V Power Supply
TCON0	94	O	Timing Controller Output Bit 0
TCON1	95	O	Timing Controller Output Bit 1
TCON2	96	O	Timing Controller Output Bit 2
TCON3	97	O	Timing Controller Output Bit 3
TCON4	98	O	Timing Controller Output Bit 4
TCON5	99	O	Timing Controller Output Bit 5
TCON6	100	O	Timing Controller Output Bit 6
TCON7	101	O	Timing Controller Output Bit 7
TCON8	102	O	Timing Controller Output Bit 8
V33	103	P	+3.3V Power Supply
TCON9	104	O	Timing Controller Output Bit 9
TCON10	105	O	Timing Controller Output Bit 10
TCON11	106	O	Timing Controller Output Bit 11
TCON12	107	O	Timing Controller Output Bit 12
TCON13	108	O	Timing Controller Output Bit 13
TCON14	109	O	Timing Controller Output Bit 14
TCON15	110	O	Timing Controller Output Bit 15
PWM1	111	O	Pulse Width Modulation Output 1
V25	112	P	+2.5V Power Supply
INPUT_G7	113	I	Input Green Data Bit 7
INPUT_G6	114	I	Input Green Data Bit 6
INPUT_G5	115	I	Input Green Data Bit 5
INPUT_G4	116	I	Input Green Data Bit 4
INPUT_G3	117	I	Input Green Data Bit 3
INPUT_G2	118	I	Input Green Data Bit 2
INPUT_G1	119	I	Input Green Data Bit 1
INPUT_G0	120	I	Input Green Data Bit 0



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Symbol	Pin No	I/O	Description
GND	121	G	System Ground
V33	122	P	+3.3V Power Supply
INPUT_R7	123	I	Input Red Data Bit 7
INPUT_R6	124	I	Input Red Data Bit 6
INPUT_R5	125	I	Input Red Data Bit 5
INPUT_R4	126	I	Input Red Data Bit 4
INPUT_R3	127	I	Input Red Data Bit 3
INPUT_R2	128	I	Input Red Data Bit 2
INPUT_R1	129	I	Input Red Data Bit 1
INPUT_R0	130	I	Input Red Data Bit 0
PWM2	131	O	Pulse Width Modulation Output 2
GPIO0	132	I/O	General Purpose Input/Output Bit 0
GPIO1	133	I/O	General Purpose Input/Output Bit 1
GPIO2	134	I/O	General Purpose Input/Output Bit 2
GPIO3	135	I/O	General Purpose Input/Output Bit 3
GPIO4	136	I/O	General Purpose Input/Output Bit 4
GPIO5	137	I/O	General Purpose Input/Output Bit 5
V33	138	P	+3.3V Power Supply
GPIO6	139	I/O	General Purpose Input/Output Bit 6
GPIO7	140	I/O	General Purpose Input/Output Bit 7
GPIO8	141	I/O	General Purpose Input/Output Bit 8
GPIO9	142	I/O	General Purpose Input/Output Bit 9
GPIO10	143	I/O	General Purpose Input/Output Bit 10
GPIO11	144	I/O	General Purpose Input/Output Bit 11
VGA_CK	145	I	VGA Input Clock
D_HS	146	I	Digital Input Horizontal Sync
N/C	147	N/C	No Connection
DDC_SDA	148	I/O	DDC I2C Bus Data Output, also as ISP I2C Bus Data Input/Output
DDC_SCL	149	I	DDC I2C Bus Clock Input, also as ISP I2C Bus Clock Input
V33	150	P	+3.3V Power Supply
N/C	151	N/C	No Connection
OSC_IN	152	I	X'tal Osc Input
OSC_OUT	153	O	X'tal Osc Output
V25	154	P	+2.5V Power Supply
D_VS	155	I	Digital Input Vertical Sync
VGA_DE	156	I	VGA Input Data Enable
TV_CK	157	I	Video (TV) Input Clock
TV_HS	158	I	Video (TV) Input Horizontal Sync
TV_VS	159	I	Video (TV) Input Vertical Sync
VGA_VS	160	I	VGA Input Vertical Sync

Note: All input pins have internal pull down (100K)



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3.2 Pin Diagram

