ZMD31050

Advanced Differential Sensor Signal Conditioner

Datasheet PRELIMINARY

Features

- Digital compensation of sensor offset, sensitivity, temperature drift and non-linearity
- Accommodates nearly all bridge sensor types (signal spans from 1 up to 275mV/V processable)
- Digital one-shot calibration: quick and precise
- Selectable compensation temperature T1 source: bridge, thermistor, internal diode or external diode
- Output options: voltage (0...5V), current (4...20mA), PWM, I²C, SPI, ZACwire™ (one-wire-interface), alarm
- Adjustable output resolution (up to 15 bits) versus sampling rate (up to 3.9kHz)
- Selectable bridge excitation: ratiometric voltage, constant voltage or constant current
- Input channel for separate temperature sensor
- Sensor connection and common mode check (Sensor aging detection)
- Operation temperature, depending on product version, up to -40..+125°C (derated up to +150°C)
- Supply voltage +2.7V...+5.5V
- Available in SSOP16 or as die

Benefits

- No external trimming components required
- PC-controlled configuration and calibration via digital bus interface - simple, low cost
- High accuracy (±0.1% FSO @ -25...85°C; ±0.25% FSO @ -40...125°C)

Brief Description

ZMD31050 is a CMOS integrated circuit for highly-accurate amplification and sensor-specific correction of bridge sensor signals. The device provides digital compensation of sensor offset, sensitivity, temperature drift and non-linearity by a 16-bit RISC micro controller running a correction algorithm with correction coefficients stored in non-volatile EEPROM.

The ZMD31050 accommodates virtually any bridge sensor (e.g. piezo-resistive, ceramic-thickfilm or steel membrane based). In addition, the IC can interface a separate temperature sensor.

The bi-directional digital interfaces (I²C, SPI, ZACwire™) can be used for a simple PC-controlled one-shot calibration procedure, in order to program a set of calibration coefficients into an on-chip EEPROM. Thus a specific sensor and a ZMD31050 are mated digitally: fast, precise and without the cost overhead associated with laser trimming, or mechanical potentiometer methods.

- **Application kit available (SSOP16 samples, calibration PCB, calibration software, technical documentation)**
- **Support for industrial mass calibration available**
- **Quick circuit customization possible for large production volumes**

Application Circuit (Examples)

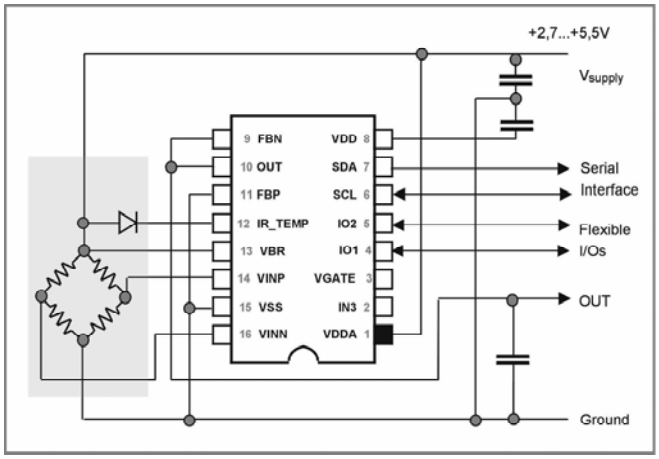

Fig.1: Ratiometric measurement with voltage output, temperature compensation via external diode

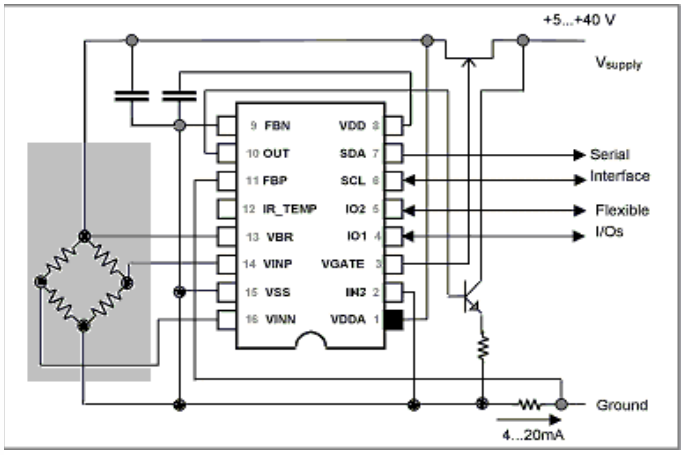

Fig.2: Two wire 4...20mA (5...40V) configuration, temperature compensation via internal diode

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Contents

1. Circuit Description

1.1 Signal Flow

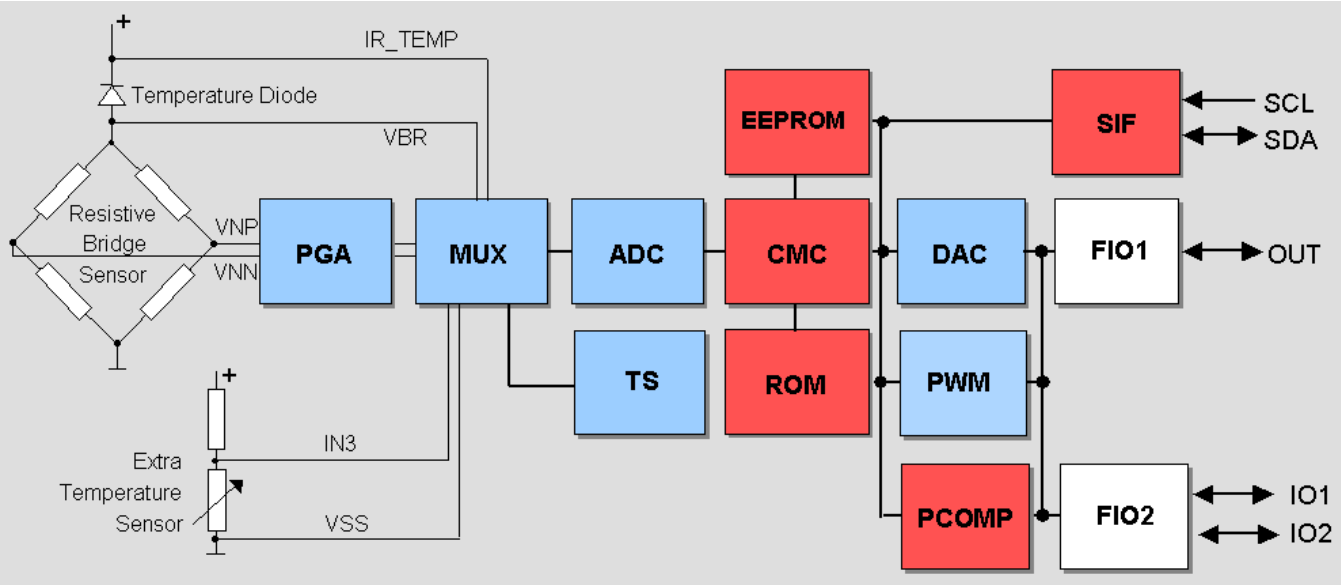


Fig.3: Block diagram of ZMD31050

PGA	programmable gain amplifier
MUX	multiplexer
ADC	analog-to-digital converter
CMC	calibration microcontroller
DAC	digital-to-analog converter
FIO1	flexible I/O 1: analog out (voltage/current), PWM2, ZACwire™ (one-wire-interface)
FIO2	flexible I/O 2: PWM1, SPI data out, SPI slave select, Alarm1, Alarm2SIF serial interface: I2C data I/O, SPI data in, clock
PCOMP	programmable comparator
EEPROM	for calibration parameters and configuration
TS	on-chip temperature sensor (pn-junction)
ROM	for correction formula and –algorithm
PWM	PWM module

The ZMD31050's signal path is partly analog (blue) and partly digital (red). The analog part is realized differential – this means internal is the differential bridge sensor signal also handled via two signal lines, which are rejected symmetrically around a common mode potential (analog ground = VDDA/2). Consequently it is possible to amplify positive and negative input signals, which are located in the common mode range of the signal input.
The differential signal from the bridge sensor is pre-amplified by the programmable gain amplifier (PGA). The Multiplexer (MUX) transmits the signals from bridge sensor, external diode or separate temperature sensor to the ADC in a certain sequence (instead of the temp. diode the internal pn-junction (TS) can be used optionally). Afterwards the ADC converts these signals into digital values.

The digital signal correction takes place in the calibration micro-controller (CMC). It is based on a special correction formula located in the ROM and on sensor-specific coefficients (stored into the EEPROM during calibration). Dependent on the programmed output configuration the corrected sensor signal is output as analog value, as PWM signal or in digital format (SPI, I^2C, ZACwire™). The output signal is provided at 2 flexible I/O modules (FIO) and at the serial interface (SIF). The configuration data and the correction parameters can be programmed into the EEPROM via the digital interfaces.
The modular circuit concept enables fast custom designs varying these blocks and, as a result, functionality and die size.

1.2 Application Modes

For each application a configuration set has to be established (generally prior to calibration) by programming the on-chip EEPROM regarding to the following modes:

- Sensor channel
  - **Sensor mode**: ratiometric voltage or current supply mode.
  - **Input range**: The gain of the analog front end has to be chosen with respect to the maximum sensor signal span and to this has also adjusted the zero point of the ADC
  - **Additional offset compensation**: The extended analog offset compensation has to be enabled if required, e.g. if the sensor offset voltage is near to or larger than the sensor span.
  - **Resolution/response time**: The A/D converter has to be configured for resolution and converting scheme (first or second order). These settings influence the sampling rate, signal integration time and this way the noise immunity. The **Sample Order** influences the response time too.
  - Ability to invert the sensor bridge inputs
- **Analog output**
  - Choice of output method (voltage value, current loop, PWM) for output register 1.
  - Optional choice of additional output register 2: PWM via IO1 or alarm out module via IO1/2.
- **Digital communication**: The preferred protocol and its parameter have to be set.
- **Temperature**
  - The **temperature measure source** for the temperature correction has to be chosen.
  - The temperature measure source T1 sensor type for the temperature correction has to be chosen (only T1 is usable for correction!!!)
  - Optional: the **temperature measure channel** as the second output has to be chosen.
- **Supply voltage** : For non-ratiometric output the voltage regulation has to be configured.

Note: *Not all possible combinations of settings are allowed (see section 1.5).*

The calibration procedure must include
  - the set of coefficients of calibration calculation

and, depending on configuration,
  - the adjustment of the extended offset compensation,
  - the zero compensation of temperature measurement,
  - the adjustment of the bridge current

and, if necessary,
  - the set of thresholds and delays for the alarms and the reference voltage.

1.3 Analog Front End (AFE)

The analog front end consists of the programmable gain amplifier (PGA), the multiplexer (MUX) and the analog-to-digital converter (ADC).

1.3.1. Programmable Gain Amplifier

The following tables show the adjustable gains, the processable sensor signal spans and the allowed common mode range.

No.	PGA Gain a_{IN}	Gain Amp1	Gain Amp2	Gain Amp3	Max. span V_{IN_SP} in mV/V	Input range V_{IN_CM} in % VDDA
1	420	30	7	2	2	43 - 57
2	280	30	4,66	2	3	38 - 62
3	210	15	7	2	4	43 - 57
4	140	15	4,66	2	6	40 - 59
5	105	15	3,5	2	8	38 - 62
6	70	7,5	4,66	2	12	40 - 59
7	52,5	7,5	3,5	2	16	38 - 62
8	35	3,75	4,66	2	24	40 - 59
9	26,3	3,75	3,5	2	32	38 - 62
10	14	1	7	2	50	43 - 57
11	9,3	1	4,66	2	80	40 - 59
12	7	1	3,5	2	100	38 - 62
13	2,8	1	1,4	2	280	21 - 76

Table 1: Adjustable gains, resulting sensor signal spans and common mode ranges

1.3.2. Analog Sensor Offset Compensation - **A**nalog **Z**ero Point **S**hift (AZS)

The ZMD31050 supports two methods of sensor offset cancellation (zero shift):

- digital offset correction
- analog cancellation for large offset values (up to approx 300% of span)

Digital sensor offset correction will be processed at the digital signal correction/conditioning by the CMC. Analog sensor offset pre-compensation will be needed for compensation of large offset values, which would be overdrive the analog signal path by uncompensated gaining. For analog sensor offset pre-compensation a compensation voltage will be added in the analog pre-gaining signal path (coarse offset removal). The analog offset compensation in the AFE can be adjusted by 6 EEPROM bits. It allows an Analog Zero Point Shift up to 300% of the processable signal span.

The zero point shift of the temperature measurements can also be adjusted by 6 EEPROM bits (Z_{AZS}= -25…+25) and is calculated by:

$$V_{AZS} / VDD_{BR} = k * Z_{AZS} / (20 * a_{IN})$$

PGA gain a_{IN}	Max. span V_{IN_SP} in mV/V	Calculation factor k	Offset shift per step in % full span	Approx. maximum offset shift in mV/V	Approx. maximum shift in [% V_{IN_SP}] (@ ± 25)
420	2	3,0	15%	+/- 9	450
280	3	1,833	9%	+/- 8	266
210	4	3,0	15%	+/- 18	450
140	6	1,833	9%	+/- 18	300
105	8	1,25	6%	+/- 15	187
70	12	1,833	9%	+/- 33	275
52,5	16	1,25	6%	+/- 44	275
35	24	1,833	9%	+/-66	275
26,3	32	1,25	6%	+/- 87	272
14	50	3,0	15%	+/- 270	540
9,3	80	1,833	9%	+/- 250	312
7	100	1,25	6%	+/- 225	225
2,8	280	0,2	1%	+/- 90	32

Table 2: Analog Zero Point Shift Ranges

1.3.3. Measurement Cycle realized by Multiplexer

The Multiplexer selects, depending on EEPROM settings, the following inputs in a certain sequence.

- Bridge temperature signal measured by external diode
- Bridge temperature signal measured by internal pn-junction
- Bridge temperature signal measured by bridge resistors
- Separate temperature signal measured by external thermistor
- Internal offset of the input channel measured by input short circuiting
- Pre-amplified bridge sensor signal

The complete measurement cycle is controlled by the CMC. The cycle diagram at the right shows its principle structure.

The EEPROM adjustable parameters are:

- Pressure measurement count, n=<1,2,4,8,16,32,64,128>
- Enable temperature measurement 2, e2=<0,1>

After Power ON the start routine is called. It contains the pressure and auto zero measurement. When enabled it measures the temperature and its auto zeros.

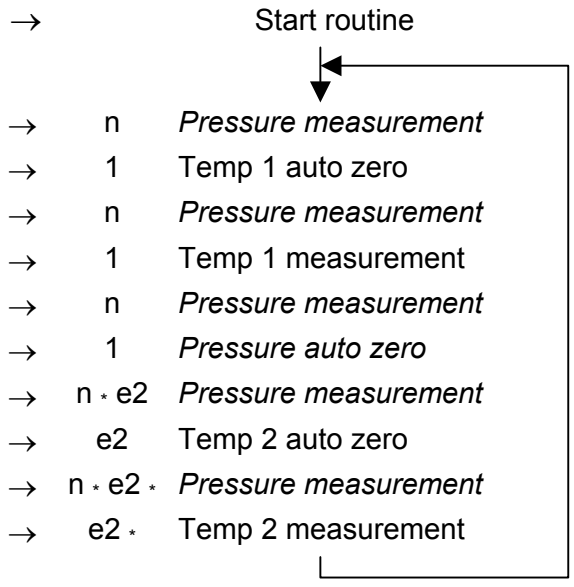


Fig. 4: Measurement cycle ZMD31050

1.3.4. Analog-to-Digital Converter

The ADC is a charge balancing converter in full differential switched capacitor technique. It can be used as first or second order converter:
In the **first order** mode it is inherently monotone and insensitive against short and long term instability of the clock frequency. The conversion cycle time depends on the desired resolution and can be roughly calculated by:

$$t_{CYC\_1} = 2^{r}\ \mu s$$

The available ADC-resolutions are r_{ADC}=<9,10,11,12,13,14,15>.

The result of the AD conversion is a relative counter result corresponding to the following equation:

$$V_{ADC\_DIFF} / V_{ADC\_REF} = Z_{ADC} / N - RS_{ADC}$$

ZOUT:	number of counts (result of the conversion)
N:	total number of counts (=2^{r})
V_{ADC_DIFF}:	differential input voltage of ADC
V_{ADC_REF}:	differential reference voltage of ADC
RS_{ADC}:	digital ADC Range Shift (RS_{ADC} = $^{1}/_{16}$, $^{1}/_{8}$, $^{1}/_{4}$, $^{1}/_{2}$, controlled by the EEPROM content)

With the RS_{ADC} value a sensor input signal can be shifted in the optimal input range of the ADC.

In the **second order** mode two conversions are stacked with the advantage of much shorter conversion cycle time and the drawback of a lower noise immunity caused by the shorter signal integration period. The conversion cycle time at this mode is roughly calculated by:

$$t_{CYC\_2} = 2^{(r+3)/2}\ \mu s$$

The available resolutions are r_{ADC}=<10,11,12,13,14,15>. The result of the AD conversion is a relative counter result corresponding to the following equations:

$$V_{ADC\_DIFF} / V_{ADC\_REF} = Z_{ADC} / N - RS_{ADC}$$
$$Z_{ADC} = Z1 * (N2/2) + Z2$$
$$N = N1 * 2^{(INT(r+2)/2)} + N2$$

Z1:	number of counts (result of the 1st conversion)
Z2:	number of counts (result of the 2nd conversion)
N1:	total number of counts 1st conversion (=$2^{(INT(r+2)/2)}$)
N2	total number of counts 2nd conversion (=$2^{(INT(r+1)/2)}$)
V_{ADC_DIFF}:	differential input voltage of ADC
V_{ADC_REF}:	differential reference voltage of ADC
RS_{ADC}:	digital ADC Range Shift (RS_{ADC} = $^{1}/_{16}$, $^{1}/_{8}$, $^{1}/_{4}$, $^{1}/_{2}$, controlled by the EEPROM content)

Note: The AD conversion time is only a part of a whole sample cycle. Thus the sample rate is lower then the AD conversion rate.

ADC Order	Maximum Output Resolution				Sample Rate	
	r_{ADC}*	Digital-OUT	Analog-OUT	r_{PWM}	f_{CLK}=2MHz	f_{CLK} =2.25MHz
O_{ADC}	Bit	Bit	Bit	Bit	Hz	Hz
1	9	9	9	9	1302	1465
	10	10	10	10	781	879
	11	11	11	11	434	488
	12	12	11	12	230	259
	13	13	11	12	115	129
	14	14	11	12	59	67
	15	15	11	12	30	34
2	10	10	10	10	3906	4395
	11	11	11	11	3906	4395
	12	12	11	12	3906	4395
	13	13	11	12	1953	2197
	14	14	11	12	1953	2197
	15	15	11	12	977	1099

Table 2: Output resolution versus sample rate

*ADC Resolution should be 1 or 2 Bits higher then applied Output Resolution

1.4 System Control

The system control has the following features:

- Control of the I/O relations and of the measurement cycle regarding to the EEPROM-stored configuration data
- 16 bit correction calculation for each measurement signal using the EEPROM stored calibration coefficients and ROM-based algorithms
- Started by internal POC, internal clock – generator or external clock
- For safety improvement the EEPROM data are proved with a signature within initialization procedure, the registers of the CMC are steadily observed with a parity check. Once an error is detected, the error flag of the CMC is set and the outputs are driven to a diagnostic value

Note: *The conditioning includes up to third order sensor input correction. The available adjustment ranges depend on the specific calibration parameters, a detailed description will be issued later. To give a rough idea: Offset compensation and linear correction are only limited by the loose of resolution it will cause, the second order correction is possible up to about 30% full scale difference to straight line, third order up to about 20% (ADC resolution = 13bit). The temperature calibration includes first and second order correction and should be fairly sufficient in all relevant cases. ADC resolution influences also calibration possibilities – 1 bit more resolution reduces calibration range by approximately 50%.*

1.5 Output Stage

	Used serial IF		Used I/O pins			
No.	I²C	SPI	OUT	IO1	IO2	SDA
1	X					Data I/O
2	X			ALARM1		Data I/O
3	X				ALARM2	Data I/O
4	X			ALARM1	ALARM2	Data I/O
5	X			PWM1		Data I/O
6	X			PWM1	ALARM2	Data I/O
7	X		Analog			Data I/O
8	X		Analog	ALARM1		Data I/O
9	X		Analog		ALARM2	Data I/O
10	X		Analog	ALARM1	ALARM2	Data I/O
11	X		Analog	PWM1		Data I/O
12	X		Analog	PWM1	ALARM2	Data I/O
13	X		PWM2			Data I/O
14	X		PWM2	ALARM1		Data I/O
15	X		PWM2		ALARM2	Data I/O
16	X		PWM2	ALARM1	ALARM2	Data I/O
17	X		PWM2	PWM1		Data I/O
18	X		PWM2	PWM1	ALARM2	Data I/O
19		X		Data out	Slave select	Data in
20		X		Data out ALARM1	Slave select -	Data in -
21		X		Data out PWM1	Slave select -	Data in -
22		X	Analog	Data out	Slave select	Data in
23		X	Analog	Data out ALARM1	Slave select -	Data in -
24		X	Analog	Data out PWM1	Slave select -	Data in -
25		X	PWM2	Data out	Slave select	Data in
26		X	PWM2	Data out ALARM1	Slave select -	Data in -
27		X	PWM2	Data out PWM1	Slave select -	Data in -

Table 3: Output configurations overview

The ZMD31050 provides the following I/O pins: OUT, IO1, IO2 and SDA.

Via these pins the following signal formats can be output: Analog (voltage/current), PWM, Data (SPI/I²C), Alarm.

The following values can be provided at the O/I pins: bridge sensor signal, temperature signal 1, temperature signal 2, alarm.

Note:
The Alarm signal only refers to the bridge sensor signal, but never to a temperature signal.

Due to the necessary pin sharing there are restrictions to the possible combinations of outputs and interface connections.
The table beside gives an overview about possible combinations.

Note:
In the SPI mode the pin IO2 is used as Slave select. Thus no Alarm 2 can be output in this mode.

1.5.1. Analog Output

For the analog output 3 registers of 12 bit depth are available, which can store the actual pressure and the results of temperature measurement 1 and 2. Each register can be independently switched to one of two output slots connected to the Pin OUT and IO1 respectively. In these output slots different output modules are available according to the following table:

Output slot:	OUT	IO1
Voltage	x	
PWM	x	x

Table 5:Analog output configuration

The Voltage module consists of an 11bit resistor string – DAC with buffered output and a subsequent inverting amplifier with class AB rail-to-rail OPAMP. The two feedback nets are connected to the Pins FBN and FBP. This structure offers wide flexibility for the output configuration, for example voltage output and 4 to 20 mA current loop output. To short circuit the analog output against VSS or VDDA does not damage the ZMD31050.

The PWM module provides pulse streams with signal dependent duty cycle. The PWM – frequency depends on resolution and clock divider. The maximum resolution is 12 bit, the maximum PWM – frequency is 4 kHz (9 bit). If both, second PWM and SPI protocol are activated, the output pin IO1 is shared between the PWM output and the SPI_SDO output of the serial interface (Interface communication interrupts the PWM output).

1.5.2. Comparator Module (ALARM Output)

The comparator module consists of two comparator channels connectable to IO1 and IO2 respectively. Each of them can be independently programmed referring to the parameters threshold, hysteresis, switching direction and on/off – delay, additional a window comparator mode is available.

1.5.3. Serial Digital Interface

The ZMD31050 includes a serial digital interface which is able to communicate in three different communication protocols – I^2C^{TM}, SPI^{TM} and ZACwire™ (one wire communication).
In the SPI mode the pin IO2 operates as slave select input, the pin IO1 as data output.

Initializing Communication

After power-on the interface is for about 20ms (start window) in the state ZACwire. During the start window it is possible to communicate via the one wire interface (pin OUT).
Detecting a proper request inside the start window the interface stays in the state ZACwire. This state can be left by certain commands or a new power-on.
If no request happens during the start window then the serial interface switches to I^2C or SPI mode (depending on EEPROM settings) and the OUT pin is used as analog output or as PWM output (also depending on EEPROM settings. The start window can generally be disabled (or enabled) by a special EEPROM setting.
For detailed description of the serial interfaces see “ZMD31050 Functional Description”.

1.6 Voltage Regulator

For ratiometric applications 3V to 5V (+/- 10%) the external supply voltage can be used for sensor element biasing. If an absolute analog output is desired then the internal voltage regulator with external power regulation element (FET) can be used. It is bandgap reference based and designed for an external supply range V_{SUPP} = (7 … 40) VDC. With the voltage regulator the internal supply and sensor bridge voltage can be varied between 3V and 5V.

1.7 Watchdog and Error Detection

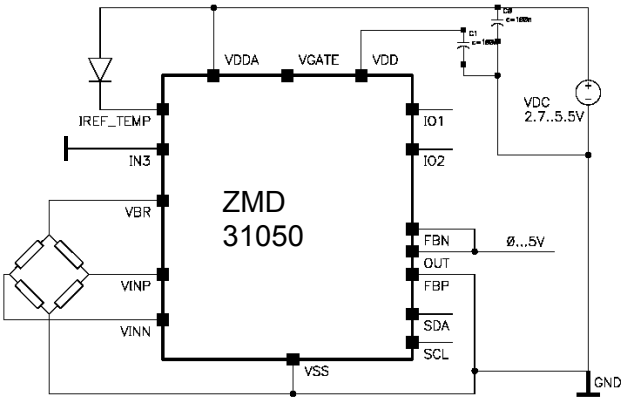
The ZMD31050 detects various possible errors. A detected error is signalized by changing in a diagnostic mode. In this case the analog output is set to High or Low (maximum or minimum possible output value) and the output registers of the digital serial interface are set to a significant error code.

A watchdog oversees the continuous working of the CMC and the running measurement loop.

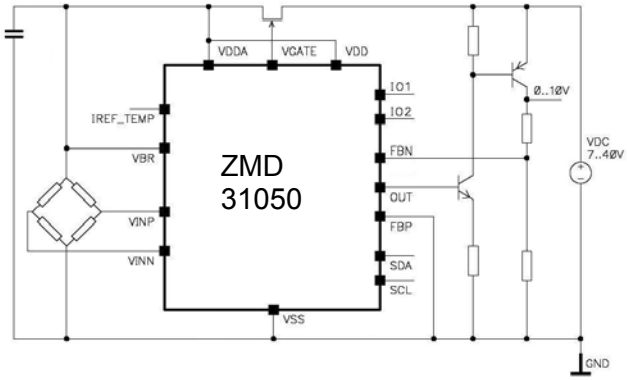
A check of the sensor bridge for broken wires which is done permanently by two comparators watching the input voltage of each input (between 0.5V … VDDA-0.5V). Add on the common mode voltage of the sensor is watched permanently (sensor aging).

Different functions and blocks in digital part are watched like RAM-, Rom,- EEPROM- and Register content continuously, the document “ZMD31050 Functional Description” contains in chapter 1.3.4 a detailed description of all watched block and methods of messaging of errors.

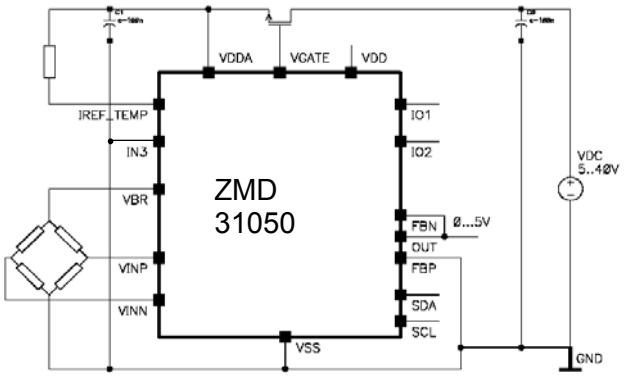
2. Application Circuit Examples



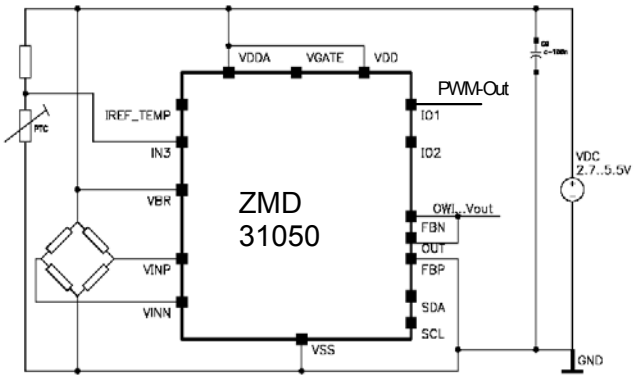
Example 1
Typical ratiometric measurement with voltage output, temperature compensation via external diode, internal VDD regulator and supply lost diagnosis (bridge must not be at VDDA) is used



Example 2
0-10V output configuration, supply regulator, temperature compensation via internal diode, internal VDD regulator and bridge in voltage mode



Example 3
Absolute voltage output, constant current biasing of the sensor bridge, temperature compensation by bridge voltage drop measurement, internal VDD regulator without ext. capacitor



Example 4
Ratiometric pressure measurement, 3–wire connection for end of line calibration, additional temperature measurement with external thermistor for PWM-output

Hint:
It is possible to combine or split connectivity of different application examples. For VDD generation ZMD recommends to use internal supply voltage regulator with external capacitor (refer to example 1).

3. ESD/Latch-Up-Protection

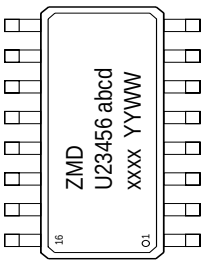
All pins have an ESD Protection of >2000V (except the Pins INN,INP,FBP with > 1200V) and a Latch-up protection of ±100mA or of +8V/ –4V (to VSS/VSSA) – refer chapter 4 for details and restrictions. ESD Protection referred to the human body model is tested with devices in SSOP16 packages during product qualification. The ESD test follows the human body model with 1.5kOhm/100pF based on MIL 883, Method 3015.7.

4. Pin Configuration and Package

Pin	Name	Description	Remarks	Latch-Up related Application Circuit Restrictions and/or Remarks
10	OUT	Analog output & PWM2 Output & one wire interface i/o	Analog OUT & dig. IO	free accessibility
11	FBP	Positive feedback connection output stage	Analog IO	free accessibility
9	FBN	Negative feedback connection output stage	Analog IO	free accessibility
1	VDDA	Positive analog supply voltage	Supply	
8	VDD	Positive digital supply voltage	Supply	only short to VDDA or capacitor to VSS allowed, otherwise no application access
15	VSS	Negative supply voltage	Ground	
6	SCL	I²C clock & SPI clock	Digital IN, pull-up	free accessibility
7	SDA	Data IO for I²C & data IN for SPI	Digital IO, pull-up	free accessibility
14	VINP	Positive input sensor bridge	Analog IN	free accessibility
16	VINN	Negative input sensor bridge	Analog IN	free accessibility
13	VBR	Bridge top sensing in bridge current out	Analog IO	only short to VDDA or connection to sensor bridge, otherwise no application access
2	IN3	Resistive temp sensor IN & external clock IN	Analog IN	free accessible (latch-up related)
12	IR_TEMP	Current source resistor i/o & temp. diode in	Analog IO	circuitry secures potential inside of VSS-VDDA range, otherwise no application access
3	VGATE	Gate voltage for external regulator FET	Analog OUT	only connection to external FET
4	IO1	SPI data out & ALARM1 & PWM1 Output	Digital IO	free accessibility
5	IO2	SPI chip select & ALARM2	Digital IO	free accessibility

The standard package of the ZMD31050 is a SSOP16 (5.3mm body width) with lead-pitch 0.65mm:

Pin-Nr	Pin-Name
9	FBN
10	OUT
11	FBP
12	IR_TEMP
13	VBR
14	VINP
15	VSS
16	VINN



Pin-Name	Pin-Nr
VDD	8
SDA	7
SCL	6
IO2	5
IO1	4
VGATE	3
IN3	2
VDDA	1

5. IC Characteristics

5.1 Absolute Maximum Ratings

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
5.1.1	Digital Supply Voltage	VDD_{AMR}	-0.3		6.5	V DC	to VSS
5.1.2	Analog Supply Voltage	$VDDA_{AMR}$	-0.3		6.5	V DC	to VSS
5.1.3	Voltage at all analog and digital I/O – Pins	$V_{A\_I/O}$, $V_{D\_I/O}$	-0.3		VDDA +0.3	V DC	Exception s. 5.1.4
5.1.4	Voltage at Pin FBP	V_{FBP_AMR}	-1.2		VDDA +0.3	V DC	4 .. 20mA – Interface
5.1.5	Storage temperature	T_{STG}	-45		150	°C	

5.2 Operating Conditions (Voltages related to VSS)

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
5.2.1	Ambient temperature	T_{AMB}	-40		125	°C	
5.2.2	Ambient temperature advanced performance	T_{AMB_ADV}	-25		85	°C	
5.2.3	Analog Supply Voltage	VDDA	2.7		5.5	V DC	ratiometric mode
5.2.4	Analog Supply Voltage advanced performance	$VDDA_{ADV}$	4.5		5.5	V DC	ratiometric mode
5.2.5	Digital Supply Voltage	VDD	- 2.7		1.05 -	VDDA V DC	external powered
5.2.6	External Supply Voltage	V_{SUPP}	VDDA + 2V		40	V DC	voltage regulator mode with ext. JFET
5.2.7	Common mode input range	V_{IN_CM}	0.25		0.65	VDDA	absolute ratings in temperature range[1]
5.2.8	Input Voltage Pin FBP	V_{IN_FBP}	-1		VDDA	V DC	
5.2.9	Sensor Bridge Resistance	R_{BR}	3.0 [2] 5.0		25.0 25.0	kΩ kΩ	full temperature range 4 .. 20mA – Interface

[1] See also chapter 1.3.1
[2] no limitations with an external connection between VDDA and VBR

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
5.2.10	Reference Resistor for Bridge Current Source	R_{BR_REF}	0.07			R_{BR}	(leads to $I_{BR} = V_{DDA} / (16 \cdot R_{Ref})$)
5.2.11	Stabilization Capacitor	C_{VDDA}	50	100	470	nF	between VDDA and VSS, extern
5.2.12	Optional Stabilization Capacitor	C_{VDD}	0 [3]	100	470	nF	between VDD and VSS, extern
5.2.13	Maximum allowed load capacitance at OUT[4]	C_{L_OUT}			50	nF	Output Voltage mode
5.2.14	Minimum allowed load resistance	R_{L_OUT}	2			kΩ	Output Voltage mode
5.2.15	Maximum allowed load capacitance at VGATE	C_{L_VGATE}			10	nF	summarized to all potentials

5.3 Build In Characteristics

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
5.3.1.	Selectable Input Span, Pressure Measurement	V_{IN_SP}	1		275	mV/V	4 Bit setting s. 3.3.1
5.3.2	Analog Offset Compensation Range (6 Bit setting)		-20 -25 -31		20 25 31	count	 ADJREF:BCUR>3 ADJREF:BCUR=7
5.3.3	A/D Resolution	r_{ADC}	9		15	Bit	3 Bit setting
5.3.4	D/A Resolution	r_{DAC}		11		Bit	@ analogue output
5.3.5	PWM - Resolution	r_{PWM}	9		12	Bit	
5.3.6	Reference current for external temperature diodes	I_{TS}	8	18	40	µA	
5.3.7	Sensitivity internal temperature diode	ST_{T_SI}	2800	3200	3600	ppm f.s. /K	Raw values - without conditioning

[3] lower stabilization capacitors can increase noise level at the output
[4] if used, consider special requirements of ZACwire™ single wire interface stated in “Functional Description” chapter 4.3

5.3.8 Cycle Rate versus A/D-Resolution

(linear related to master clock frequency[5] - values calculated at exact 2 MHz)

ADC Order	Resolution	Conversion Cycle f_{CYC}	
O_{ADC}	r_{ADC} Bit	f_{CLK}=2MHz Hz	f_{CLK}=2.25MHz Hz
1	9	1302	1465
	10	781	879
	11	434	488
	12	230	259
	13	115	129
	14	59	67
	15	30	34
2	11	3906	4395
	12	3906	4395
	13	1953	2197
	14	1953	2197
	15	977	1099

5.3.9 PWM Frequency

PWM	PWM Freq./Hz at 2 MHz Clock[5]				PWM Freq./Hz at 2.25 MHz Clock[6]			
Resolution	Clock Divider				Clock Divider			
r_{PWM} [Bit]	1	0,5	0,25	0,125	1	0,5	0,25	0,125
9	3906	1953	977	488	4395	2197	1099	549
10	1953	977	488	244	2197	1099	549	275
11	977	488	244	122	1099	549	275	137
12	488	244	122	61	549	275	137	69

[5] Internal RC – Oscillator: coarse adjustment to1, 2 and 4 MHz, fine tuning +/- 25% , external clock is also possible
[6] Internal RC – Oscillator: coarse adjustment to1.125, 2.25 and 4.5 MHz, fine tuning +/- 25% , external clock is also possible

5.4 Electrical Parameters (Voltages related to VSS)

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
5.4.1 Supply / Regulation							
5.4.1.1	Supply current	I_{SUPP}		2.5	4	mA	without bridge current and without load current, $f_{CLK} \leq 2.25MHz$
5.4.1.2	Supply current for current loop	I_{SUPP_CL}		2.0	2.5		without bridge current, $f_{CLK} \leq 1.2MHz$, Bias-Adjustment ≤ 1
5.4.1.2	Temperature Coeff. Voltage Reference [1]	TC_{REF}	-200	+/- 50	200	ppm/K	
5.4.2 Analog Front End							
5.4.2.1	Parasitic differential input offset current[1]	I_{IN_OFF}	-2 -10		2 10	nA	temp. range 5.2.2., T_{ADV}
5.4.3 DAC & Analog Output (Pin OUT)							
5.4.3.1	Output Signal Range	V_{OUT_SR}	0.025		0.975	VDDA	Voltage mode, assuming maximum load of 2k
5.4.3.2	Output Slew rate [1]	SR_{OUT}	0.1			V/µs	Voltage mode, C_L<20nF
5.4.3.3	Short circuit current limitation	I_{OUT_max}	5	10	20	mA	
5.4.4 PWM Output (Pin OUT, IO1)							
5.4.4.1	PWM high voltage	V_{PWM_H}	0.9			VDDA	R_L > 10 kΩ
5.4.4.2	PWM low voltage	V_{PWM_L}			0.1	VDDA	R_L > 10 kΩ
5.4.4.3	PWM output slew rate[1]	SR_{PWM}	15			V/µs	C_L < 1nF
5.4.5 Temperature Sensors (Output IRT)							
5.4.5.1	Sensitivity external diode or resistor meas.	ST_{TS_E}	1450	1520	1590	ppm f.s. / mV	Raw values - without conditioning
5.4.6 Digital Outputs (IO1, IO2,OUT in digital mode)							
5.4.6.1	Output-High-Level	V_{DOUT_H}	0.9			VDDA	
5.4.6.2	Output-Low-Level	V_{DOUT_L}			0.1	VDDA	
5.4.6.3	Output Current[1]	I_{DOUT}	4			mA	

[1] no measurement in serial production, parameter is guarantied by design and/or quality observation

5.4.7 System Response							
5.4.7.1	Startup time[1] [2]	t_{STA}	2		5	ms	Power up to first measure result at output, without OWI – start window
5.4.7.2	Response time	t_{RESP}	$2/f_{CON}$		$3/f_{CON}$		
5.4.7.2	Overall accuracy (Deviation from ideal line including INL, gain and offset errors)	AC_{OUT}			0.1 0.25	%	T_{ADV}, V_{ADV} (-25...+85°C, 4.5…5.5V) ADJREF:BCUR>3
5.4.7.3	Peak-to-Peak-Noise@output	V_{OUT_NS}			5	mV	shorted inputs, bandwith ≤ 2kHz
5.4.7.4	Ratiometricity Error	RE_{OUT_5} RE_{OUT_3}			500 1000	ppm ppm	4.5 – 5.0V & 5.0 – 5.5V 2.7 – 3.0V & 3.0 – 3.3V

5.5 Interface Characteristics

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
5.5.1 Multiport Serial Interfaces (I^2C, SPI)							
5.5.1.1	Input-High-Level	$V_{I2C\_IN\_H}$	0.7		1	VDDA	
5.5.1.2	Input-Low-Level	$V_{I2C\_IN\_L}$	0		0.3	VDDA	
5.5.1.3	Output-Low-Level	$V_{I2C\_OUT\_L}$			0.1	VDDA	Open-Drain I_{OL}= -3mA
5.5.1.4	load capacitance @ SDA	C_{SDA}			400	pF	
5.5.1.5	Clock frequency SCL	f_{SCL}			400	kHz	
5.5.2 One Wire Serial Interface (ZACwire™)							
5.5.2.1	Pullup resistance master	R_{OWI_PU}	330			Ω	
5.5.2.2	OWI line resistance	R_{OWI_LINE}			0.05	R_{OWI_PU}	
5.5.2.3	OWI load capacitance	C_{OWI_LOAD}			0.08	t_{OWI_BIT} / R_{OWI_PU}	$20\mu s < t_{OWI\_BIT} < 100\mu s$
5.5.2.4	Voltage level Low	V_{OWI_L}			0.2	VDDA	
5.5.2.5	Voltage level High	V_{OWI_H}	0.75			VDDA	

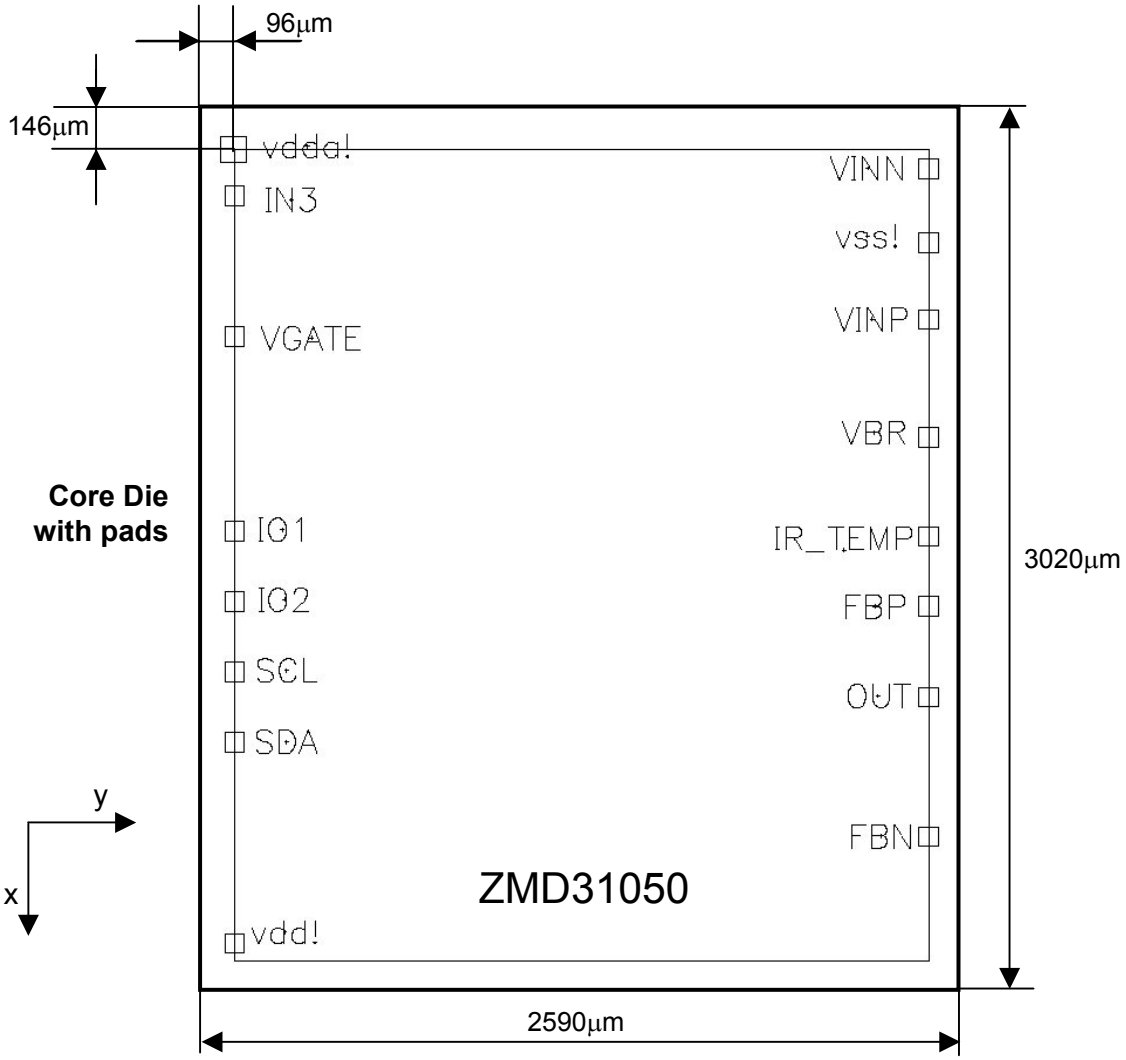
[1] no measurement in serial production, parameter is guarantied by design and/or quality observation

[2] Depends on resolution and configuration - start routine begins approximately 0.8ms after power on

6. Die Dimensions and Pad Coordinates

6.1 Die Dimensions

- Die size (incl. scribeline): 3170µm x 2740µm ≈ 8.7sqmm
- Core die size (without scribeline): 3020µm x 2590µm ≈ 7.8sqmm
- Die thickness: 390µm
- Scribeline (distance between two core dice on wafer): 150µm
- Pads size: 68µm x 68µm (exception: VDDA: 90µm x 90µm)



6.2 Pad Coordinates

All pad coordinates are for pad centers and related to the center of the VDDA pad.

Pin-No.	Name	X coordinate in µm	Y coordinate in µm
1	VDDA	0	0
2	IN3	160	0
3	VGATE	650	0
4	IO1	1320	0
5	IO2	1560	0
6	SCL	1800	0
7	SDA	2050	0
8	VDD	2740	0
9	FBN	2370	2400
10	OUT	1890	2400
11	FBP	1580	2400
12	IR_TEMP	1340	2400
13	VBR	990	2400
14	VINP	590	2400
15	VSS	320	2400
16	VINN	70	2400

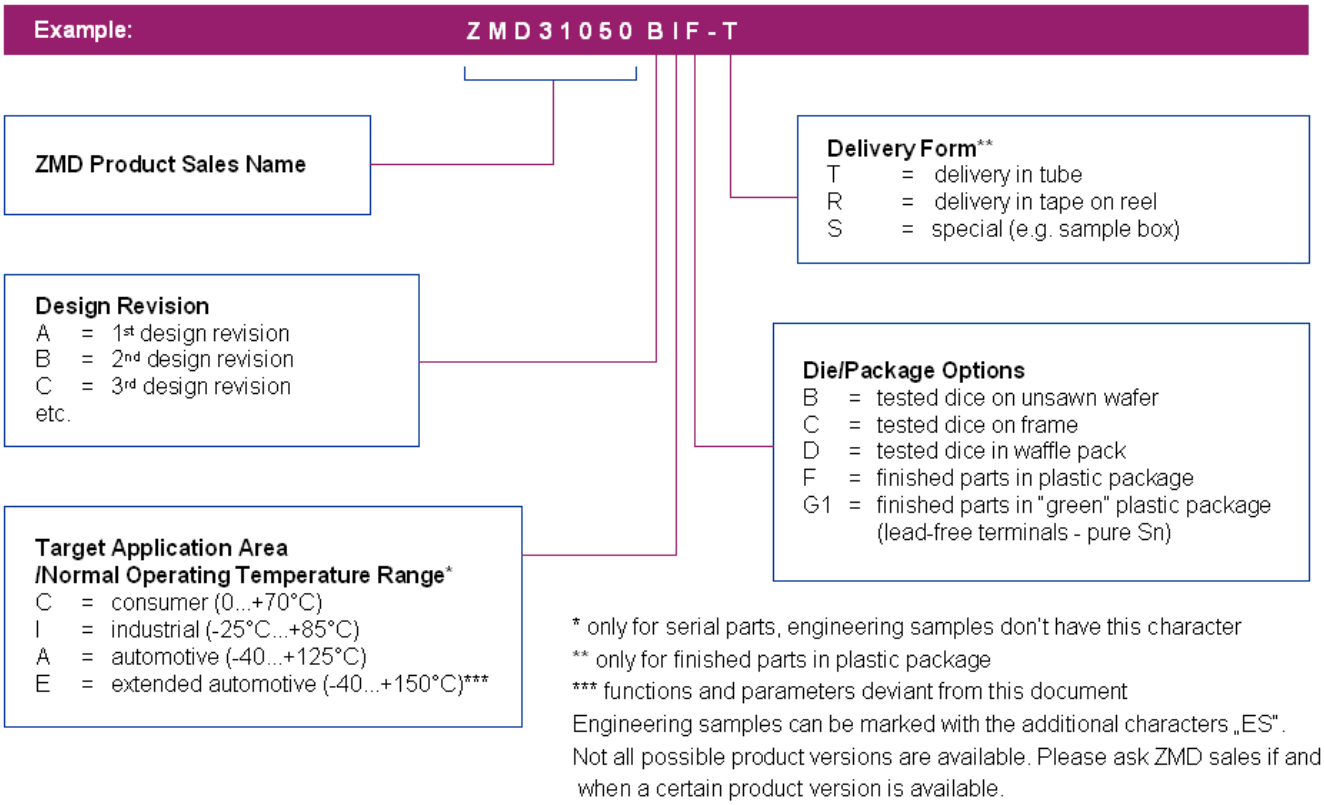
7. Test

Functions and parameters given in this datasheet are design objectives and therefore preliminary. The final functions and parameters will be specified later, in a final datasheet. ZMD will assure the final functions and parameters by serial production tests. Depending on the product version (see section 10), different serial production tests will be performed.

8. Qualification

Depending on the product version (see section 10), different pre-production qualification procedures will be performed. The product versions “automotive” and “extended automotive” (target application area) will be qualified according to AEC-Q100.

9. Product Versions / Ordering Codes



* only for serial parts, engineering samples don't have this character
** only for finished parts in plastic package
*** functions and parameters deviant from this document
Engineering samples can be marked with the additional characters „ES".
Not all possible product versions are available. Please ask ZMD sales if and when a certain product version is available.

10. Customization

For high-volume applications, which require an up- or downgraded functionality compared to the ZMD31050, ZMD can customize the circuit design by adding or removing certain functional blocks.
For it ZMD has a considerable library of sensor-dedicated circuitry blocks. Thus ZMD can provide a custom solution quickly. Please contact ZMD sales for further information.

11. Related Documents

- ZMD31050 Product Flyer
- ZMD31050 Feature Sheet
- ZMD31050 Functional Description
- ZMD31050 Application Kit Description
- ZMD31050 Calibration DLL Description

For the current version of this document please look at www.zmd.biz.

ZMD31050

Advanced Differential Sensor Signal Conditioner

Datasheet PRELIMINARY

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