

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK3307 is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3307	TO-3P

FEATURES

- Super low on-state resistance:
- ★ $R_{DS(on)1} = 9.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 35 \text{ A)}$
- ★ $R_{DS(on)2} = 14 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4 \text{ V, } I_D = 35 \text{ A)}$
- Low C_{iss} : $C_{iss} = 4650 \text{ pF TYP.}$
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	$V_{GSS(AC)}$	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 70	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 280	A
★ Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	120	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	3.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
★ Single Avalanche Current ^{Note2}	I_{AS}	45	A
★ Single Avalanche Energy ^{Note2}	E_{AS}	202	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

- ★ **2.** Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

THERMAL RESISTANCE

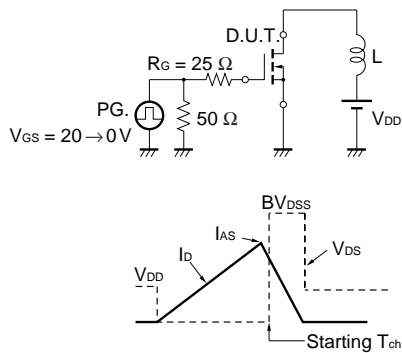
★ Channel to Case	$R_{th(ch-C)}$	1.04	$^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-A)}$	41.7	$^\circ\text{C/W}$

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

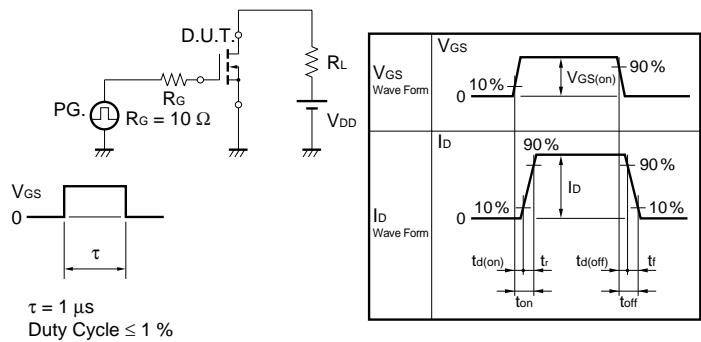
★ ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 35 A		7.5	9.5	mΩ
	R _{DS(on)2}	V _{GS} = 4 V, I _D = 35 A		10.5	14	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 35 A	30	47		S
Drain Leakage Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		4650		pF
Output Capacitance	C _{oss}			780		pF
Reverse Transfer Capacitance	C _{rss}			380		pF
Turn-on Delay Time	t _{d(on)}	I _D = 35 A, V _{GS(on)} = 10 V, V _{DD} = 30 V, R _G = 10 Ω		90		ns
Rise Time	t _r			1260		ns
Turn-off Delay Time	t _{d(off)}			270		ns
Fall Time	t _f			370		ns
Total Gate Charge	Q _G	I _D = 70 A, V _{DD} = 48 V, V _{GS} = 10 V		90		nC
Gate to Source Charge	Q _{GS}			14		nC
Gate to Drain Charge	Q _{GD}			38		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 70 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 70 A, V _{GS} = 0 V, di/dt = 100 A/μs		60		ns
Reverse Recovery Charge	Q _{rr}			110		nC

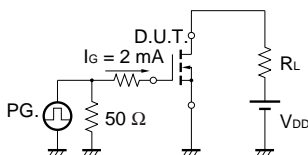
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

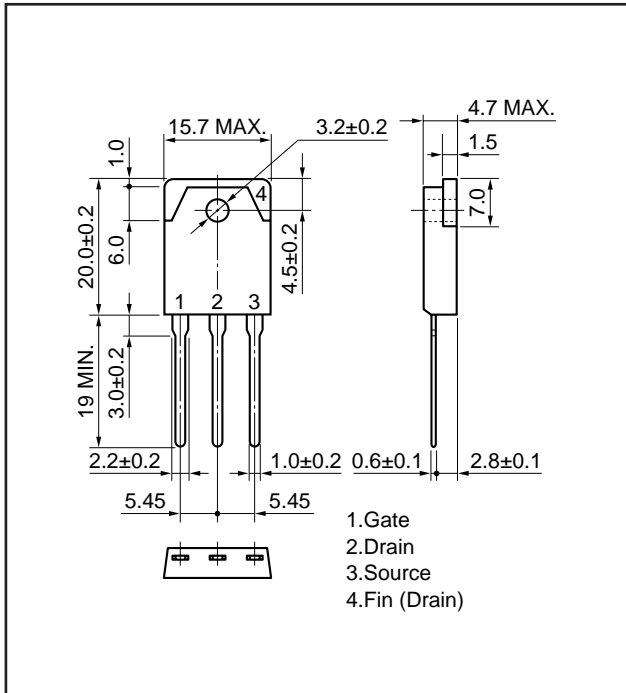


TEST CIRCUIT 3 GATE CHARGE

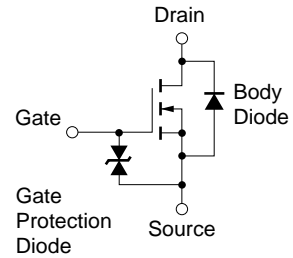


PACKAGE DRAWING (Unit: mm)

TO-3P (MP-88)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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