

DATA SHEET

74ALVT162821

2.5V/3.3V 20-bit bus-interface

D-type flip-flop; positive-edge trigger with
30 Ω termination resistors (3-State)

Product specification
Supersedes data of 1997 Feb 13
IC23 Data Handbook

1998 Oct 02

2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with 30Ω termination resistors (3-State)

74ALVT162821

FEATURES

- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- 20-bit positive-edge triggered register
- 5V I/O Compatible
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Output capability +12mA/-12mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ALVT162821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive. It is designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility to 5V.

The 74ALVT162821 has two 10-bit, edge triggered registers, with each register coupled to a 3-State output buffer. The two sections of each register are controlled independently by the clock (nCP) and Output Enable (\overline{nOE}) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable (\overline{nOE}) controls all ten 3-State buffers independent of the register operation. When \overline{nOE} is Low, the data in the register appears at the outputs. When \overline{nOE} is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74ALVT162821 is designed with 30Ω series resistance in both High and Low output stages. This design reduces the line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters. The series termination resistors reduce overshoot and undershoot and are ideal for driving memory arrays.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nCP to nQ	$C_L = 50\text{pF}$	4.4 3.8	3.2 3.2	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	3	3	pF
C_{OUT}	Output capacitance	$V_O = 0$ or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	μA

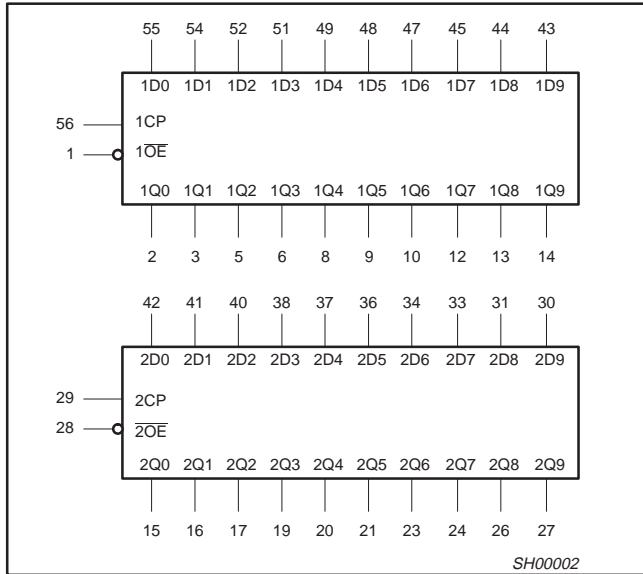
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to +85°C	74ALVT162821 DL	AV162821 DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ALVT162821 DGG	AV162821 DGG	SOT364-1

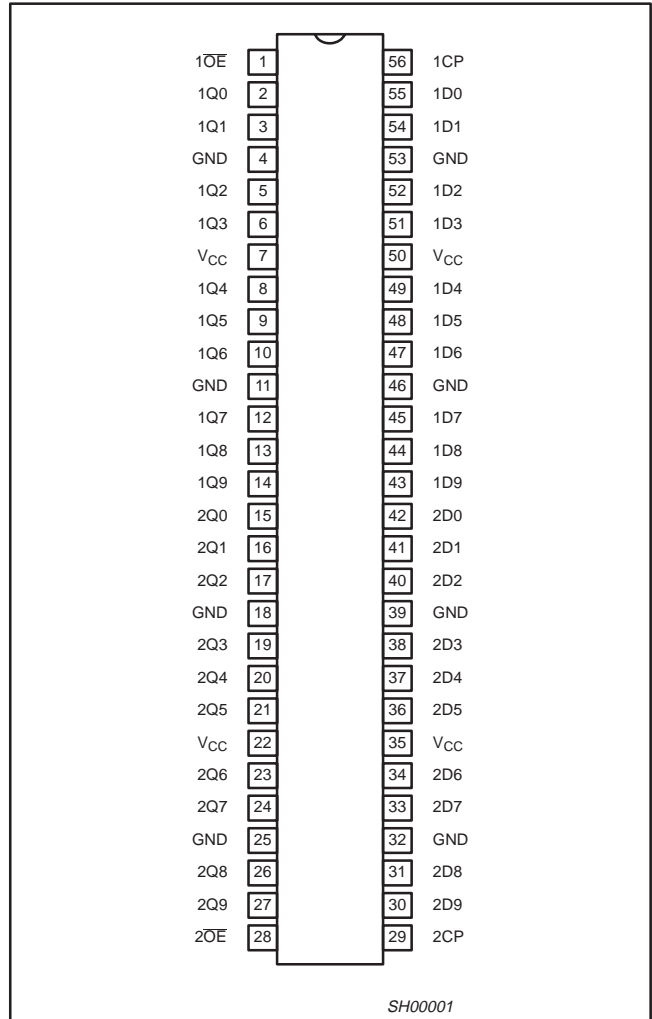
2.5V/3.3V 20-bit bus-interface D-type flip-flop;
positive-edge trigger with 30Ω termination resistors (3-State)

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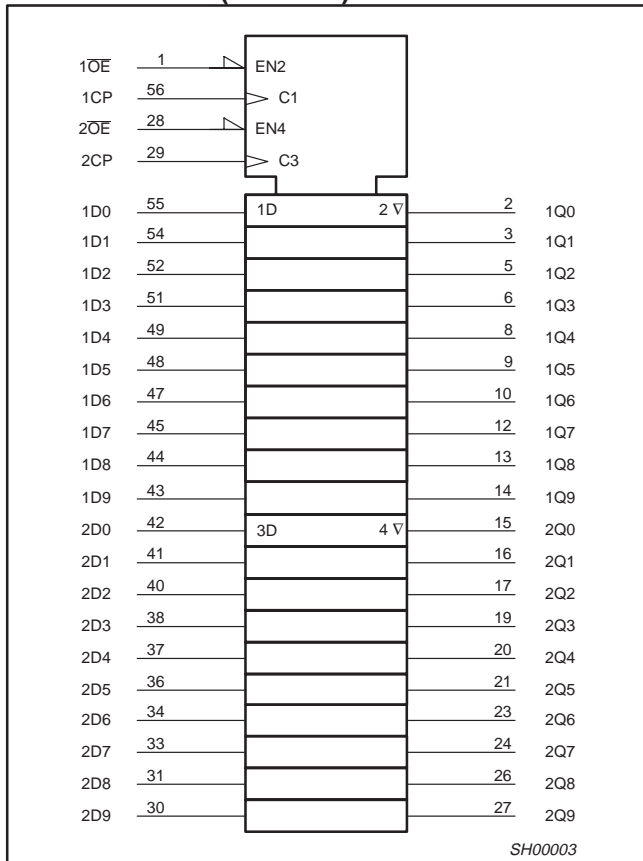
LOGIC SYMBOL



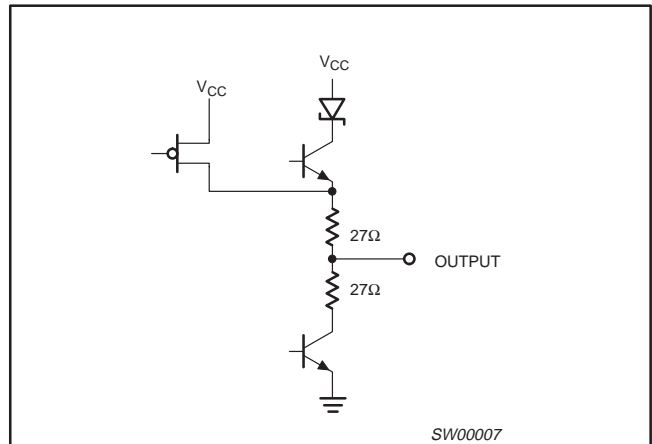
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC OF EACH OUTPUT



2.5V/3.3V 20-bit bus-interface D-type flip-flop;
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PIN DESCRIPTION

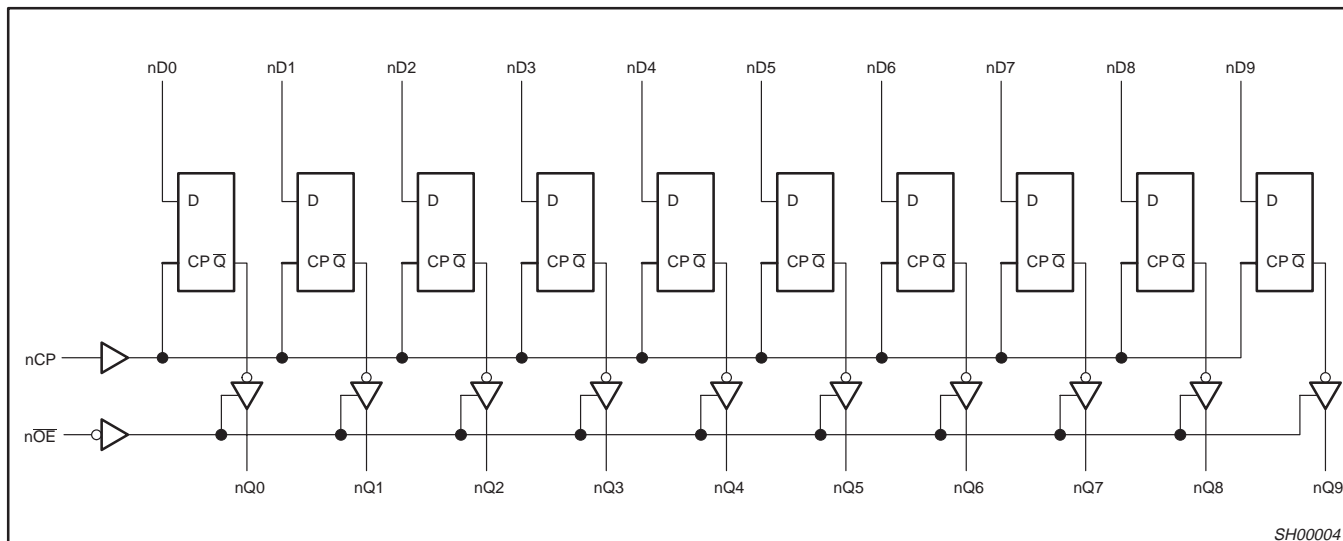
PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 - 1D9 2D0 - 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 - 1Q9 2Q0 - 2Q9	Data outputs
1, 28	1OE, 2OE	Output enable inputs (active-Low)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	VCC	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
nOE	nCP	nDx		nQ0 - nQ9	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level
 h = High voltage level one set-up time prior to the Low-to-High clock transition
 L = Low voltage level
 l = Low voltage level one set-up time prior to the Low-to-High clock transition
 NC= No change
 X = Don't care
 Z = High impedance "off" state
 ↑ = Low to High clock transition
 ↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



SH00004

2.5V/3.3V 20-bit bus-interface D-type flip-flop;
positive-edge trigger with 30Ω termination resistors (3-State)

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I _{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V _I	Input voltage	0	5.5	0	5.5	V
V _{IH}	High-level input voltage	1.7		2.0		V
V _{IL}	Input voltage		0.7		0.8	V
I _{OH}	High-level output current		-8		-12	mA
I _{OL}	Low-level output current		12		12	mA
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	-40	+85	°C

2.5V/3.3V 20-bit bus-interface D-type flip-flop;
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DC ELECTRICAL CHARACTERISTICS (3.3V ± 0.3V RANGE)

			LIMITS			
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 3.0V; I _{IK} = -18mA		-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 3.0 to 3.6V; I _{OH} = -100μA	V _{CC} -0.2	V _{CC}		V
		V _{CC} = 3.0V; I _{OH} = -32mA	2.0	2.3		
V _{OL}	Low-level output voltage	V _{CC} = 3.0V; I _{OL} = 100μA		0.07	0.2	V
		V _{CC} = 3.0V; I _{OL} = 16mA		0.25	0.4	
		V _{CC} = 3.0V; I _{OL} = 32mA		0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 64mA		0.4	0.55	
V _{RST}	Power-up output low voltage ⁶	V _{CC} = 3.6V; I _O = 1mA; V _I = V _{CC} or GND			0.55	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins	0.1	±1	μA
		V _{CC} = 0 or 3.6V; V _I = 5.5V		0.1	10	
		V _{CC} = 3.6V; V _I = V _{CC}	Data pins ⁴	0.5	1	
		V _{CC} = 3.6V; V _I = 0V		0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		0.1	±100	μA
I _{HOLD}	Bus Hold current Data inputs ⁷	V _{CC} = 3V; V _I = 0.8V	75	130		μA
		V _{CC} = 3V; V _I = 2.0V	-75	-140		
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V	±500			
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V		10	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} OE/OE = Don't care		1	±100	μA
I _{OZH}	3-State output High current	V _{CC} = 3.6V; V _O = 3.0V; V _I = V _{IL} or V _{IH}		0.5	5	μA
I _{OZL}	3-State output Low current	V _{CC} = 3.6V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		0.5	-5	μA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.07	0.1	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		5.1	7	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵		0.07	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		0.04	0.4	mA

NOTES:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.2V a transition time of 100μsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ± 0.3V RANGE)GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T _{amb} = -40 to +85°C V _{CC} = +3.3V			
			MIN	TYP	MAX	
f _{MAX}	Maximum clock frequency	1	150			MHz
t _{PLH} t _{PHL}	Propagation delay nCP to nQx	1	1.0 1.0	3.2 3.2	5.0 4.7	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	3	1.0	3.4	5.6	ns
		4	0.5	2.3	3.7	
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	3	1.5	3.7	5.4	ns
		4	1.5	3.0	4.3	

NOTE:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

2.5V/3.3V 20-bit bus-interface D-type flip-flop;
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AC SETUP REQUIREMENTS (3.3V ± 0.3V RANGE)GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +3.3\text{V} \pm 0.3\text{V}$		
			MIN	TYP	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low nDx to nCP	1	1.5 1.5	0.1 0.1	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low nDx to nCP	2	0.5 0.5	0.1 0.1	ns
$t_w(\text{H})$ $t_w(\text{L})$	nCP pulse width High or Low	2	1.5 1.5		ns

DC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			$\text{Temp} = -40^\circ\text{C to } +85^\circ\text{C}$			
			MIN	TYP ¹	MAX	
V_{IK}	Input clamp voltage	$V_{\text{CC}} = 2.3\text{V}$; $I_{\text{IK}} = -18\text{mA}$		-0.85	-1.2	V
V_{OH}	High-level output voltage	$V_{\text{CC}} = 2.3 \text{ to } 3.6\text{V}$; $I_{\text{OH}} = -100\mu\text{A}$ $V_{\text{CC}} = 2.3\text{V}$; $I_{\text{OH}} = -8\text{mA}$	$V_{\text{CC}} - 0.2$ 1.8	V_{CC} 2.1		V
V_{OL}	Low-level output voltage	$V_{\text{CC}} = 2.3\text{V}$; $I_{\text{OL}} = 100\mu\text{A}$ $V_{\text{CC}} = 2.3\text{V}$; $I_{\text{OL}} = 24\text{mA}$ $V_{\text{CC}} = 2.3\text{V}$; $I_{\text{OL}} = 8\text{mA}$		0.07 0.3 0.4	0.2 0.5	V
V_{RST}	Power-up output low voltage ⁷	$V_{\text{CC}} = 2.7\text{V}$; $I_{\text{O}} = 1\text{mA}$; $V_{\text{I}} = V_{\text{CC}}$ or GND			0.55	V
I_{I}	Input leakage current	$V_{\text{CC}} = 2.7\text{V}$; $V_{\text{I}} = V_{\text{CC}}$ or GND $V_{\text{CC}} = 0$ or 2.7V ; $V_{\text{I}} = 5.5\text{V}$ $V_{\text{CC}} = 2.7\text{V}$; $V_{\text{I}} = V_{\text{CC}}$ $V_{\text{CC}} = 2.7\text{V}$; $V_{\text{I}} = 0$	Control pins Data pins ⁴	0.1 0.1 0.1 0.1	± 1 10 1 -5	μA
I_{OFF}	Off current	$V_{\text{CC}} = 0\text{V}$; V_{I} or $V_{\text{O}} = 0$ to 4.5V		0.1	± 100	μA
I_{HOLD}	Bus Hold current Data inputs ⁶	$V_{\text{CC}} = 2.3\text{V}$; $V_{\text{I}} = 0.7\text{V}$ $V_{\text{CC}} = 2.3\text{V}$; $V_{\text{I}} = 1.7\text{V}$		90 -10		μA
I_{EX}	Current into an output in the High state when $V_{\text{O}} > V_{\text{CC}}$	$V_{\text{O}} = 5.5\text{V}$; $V_{\text{CC}} = 2.3\text{V}$		10	125	μA
$I_{\text{PU/PD}}$	Power up/down 3-State output current ³	$V_{\text{CC}} \leq 1.2\text{V}$; $V_{\text{O}} = 0.5\text{V}$ to V_{CC} ; $V_{\text{I}} = \text{GND}$ or V_{CC} OE/OE = Don't care		1	± 100	μA
I_{OZH}	3-State output High current	$V_{\text{CC}} = 2.7\text{V}$; $V_{\text{O}} = 2.3\text{V}$; $V_{\text{I}} = V_{\text{IL}}$ or V_{IH}		0.5	5	μA
I_{OZL}	3-State output Low current	$V_{\text{CC}} = 2.7\text{V}$; $V_{\text{O}} = 0.5\text{V}$; $V_{\text{I}} = V_{\text{IL}}$ or V_{IH}		0.5	-5	μA
I_{CCH}	Quiescent supply current	$V_{\text{CC}} = 2.7\text{V}$; Outputs High, $V_{\text{I}} = \text{GND}$ or V_{CC} , $I_{\text{O}} = 0$		0.04	0.1	mA
I_{CCL}		$V_{\text{CC}} = 2.7\text{V}$; Outputs Low, $V_{\text{I}} = \text{GND}$ or V_{CC} , $I_{\text{O}} = 0$		2.3	4.5	
I_{CCZ}		$V_{\text{CC}} = 2.7\text{V}$; Outputs Disabled; $V_{\text{I}} = \text{GND}$ or V_{CC} , $I_{\text{O}} = 0^5$		0.04	0.1	
ΔI_{CC}	Additional supply current per input pin ²	$V_{\text{CC}} = 2.3\text{V}$ to 2.7V ; One input at $V_{\text{CC}} - 0.6\text{V}$, Other inputs at V_{CC} or GND		0.04	0.4	mA

NOTES:

- All typical values are at $V_{\text{CC}} = 2.5\text{V}$ and $T_{\text{amb}} = 25^\circ\text{C}$.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From $V_{\text{CC}} = 1.2\text{V}$ to $V_{\text{CC}} = 2.5\text{V} \pm 0.3\text{V}$ a transition time of 100μsec is permitted. This parameter is valid for $T_{\text{amb}} = 25^\circ\text{C}$ only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- Not guaranteed.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

2.5V/3.3V 20-bit bus-interface D-type flip-flop;
positive-edge trigger with 30Ω termination resistors (3-State)

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AC CHARACTERISTICS (2.5V ± 0.2V RANGE)

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = -40$ to $+85^\circ\text{C}$ $V_{\text{CC}} = +2.5\text{V} \pm 0.2\text{V}$			
			MIN	TYP	MAX	
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.0	4.4 3.8	7.0 6.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.5 1.0	4.6 2.8	7.5 4.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.5 1.0	3.5 3.7	5.5 5.7	ns

NOTE:

1. All typical values are at $V_{\text{CC}} = 3.3\text{V}$ and $T_{\text{amb}} = 25^\circ\text{C}$.

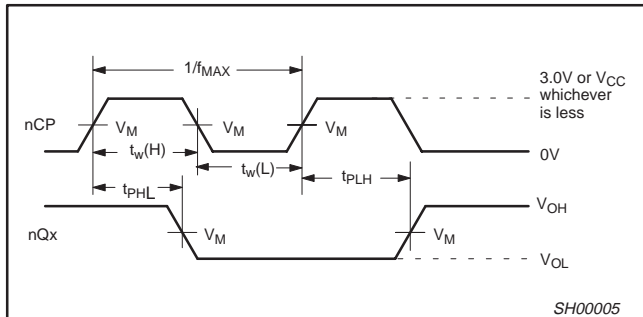
AC SETUP REQUIREMENTS (2.5V ± 0.2V RANGE)

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$

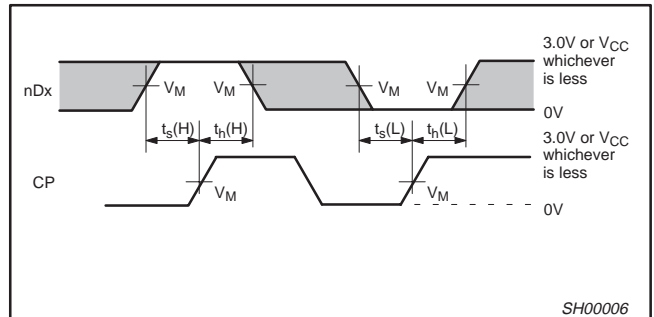
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$T_{\text{amb}} = -40$ to $+85^\circ\text{C}$ $V_{\text{CC}} = +2.5 \pm 0.2\text{V}$		
			MIN	TYP	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low nDx to nCP	1	1.5 2.0	0.1 0.5	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low nDx to nCP	2	0.3 0.5	-0.5 -0.1	ns
$t_w(\text{H})$ $t_w(\text{L})$	nCP pulse width High or Low	2	1.5 1.5		ns

AC WAVEFORMS

$V_M = 1.5\text{V}$ at $V_{\text{CC}} \geq 3.0\text{V}$; $V_M = V_{\text{CC}}/2$ at $V_{\text{CC}} \leq 2.7\text{V}$
 $V_X = V_{\text{OL}} + 0.3\text{V}$ at $V_{\text{CC}} \geq 3.0\text{V}$; $V_X = V_{\text{OL}} + 0.15\text{V}$ at $V_{\text{CC}} \leq 2.7\text{V}$
 $V_Y = V_{\text{OH}} - 0.3\text{V}$ at $V_{\text{CC}} \geq 3.0\text{V}$; $V_Y = V_{\text{OH}} - 0.15\text{V}$ at $V_{\text{CC}} \leq 2.7\text{V}$



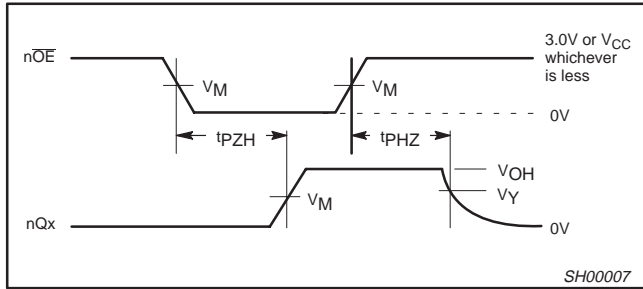
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock frequency



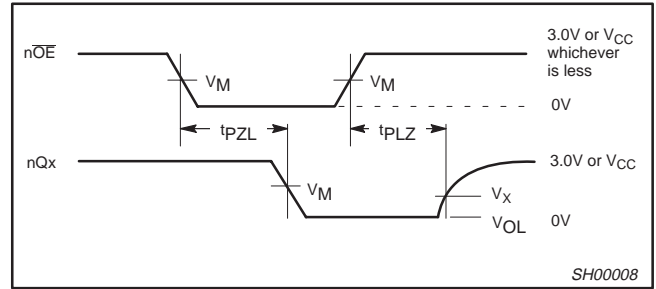
Waveform 2. Data Setup and Hold Times

2.5V/3.3V 20-bit bus-interface D-type flip-flop;
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Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or $V_{CC} \times 2$
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00025

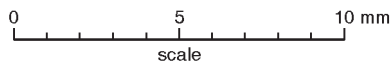
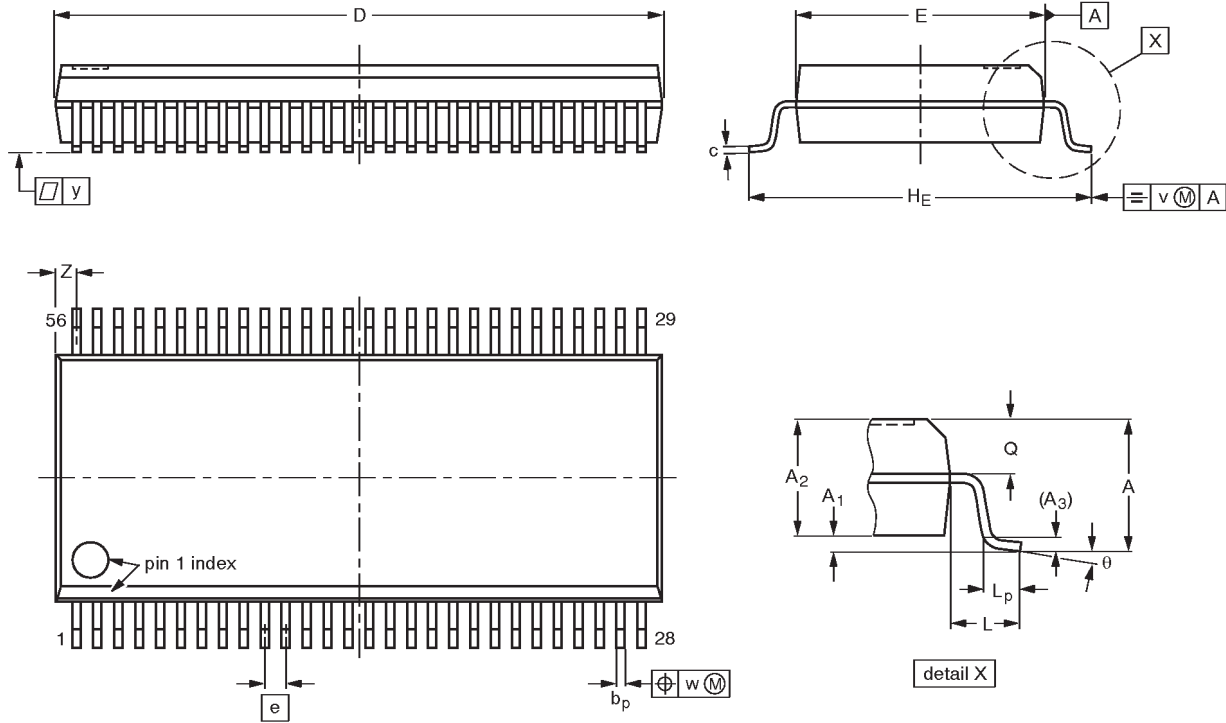
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	$\leq 2.5\text{ns}$

2.5V/3.3V 20-bit bus-interface D-type flip-flop;
positive-edge trigger with 30Ω termination resistors (3-State)

74ALVT162821

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

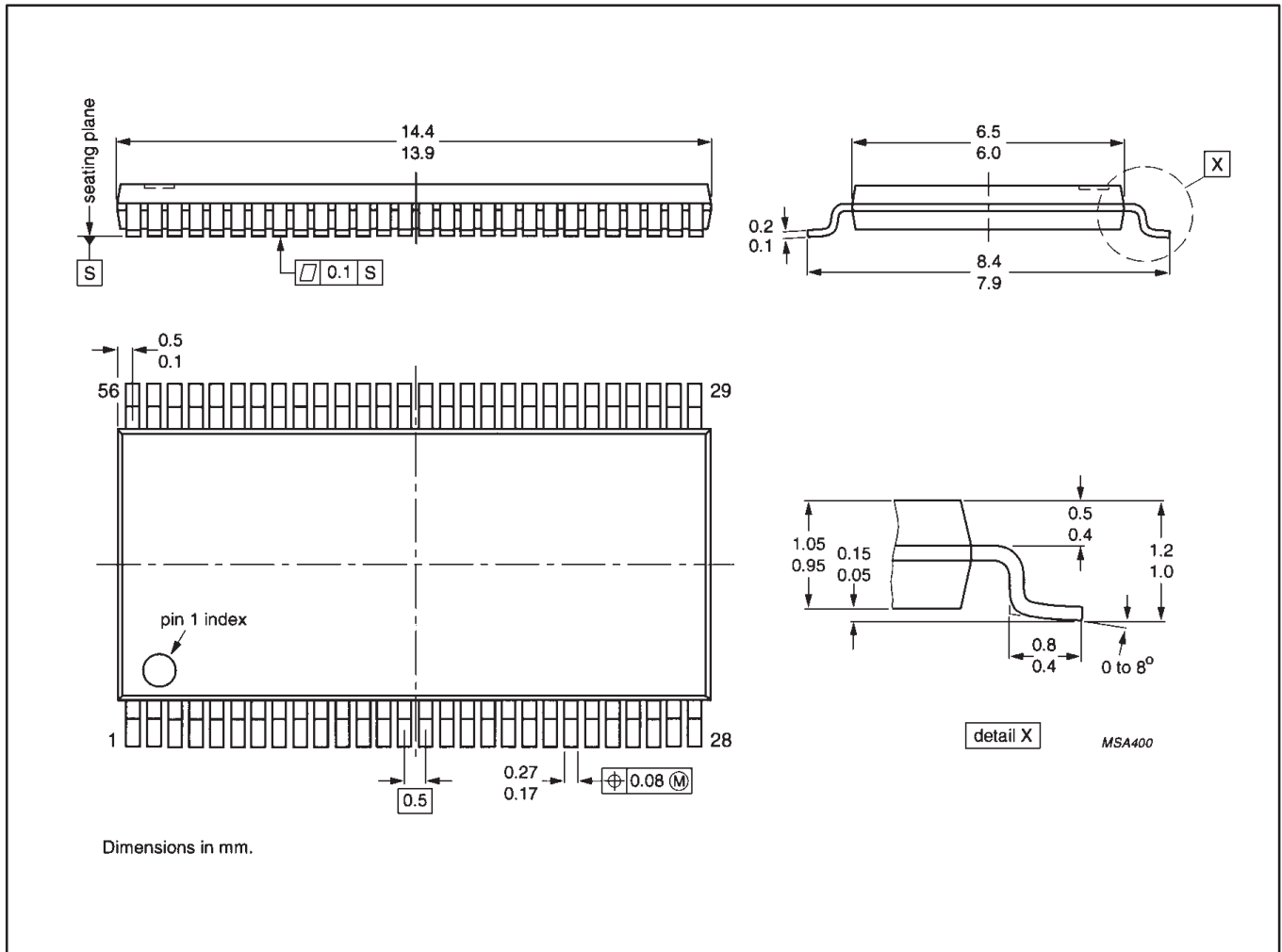
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

2.5V/3.3V 20-bit bus-interface D-type flip-flop;
positive-edge trigger with 30Ω termination resistors (3-State)

74ALVT162821

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



2.5V/3.3V 20-bit bus-interface D-type flip-flop;
positive-edge trigger with 30Ω termination resistors (3-State)

74ALVT162821

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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