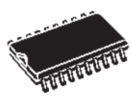
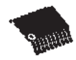
74LCX574

OCTAL D-TYPE FLIP FLOP NON INVERTING (3-STATE) WITH 5V TOLERANT INPUTS AND OUTPUTS

- 5V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED: f_{MAX} = 150 MHz (MIN.) at V_{CC} = 3V
- POWER-DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 24 mA (MIN)
- PCI BUS LEVELS GUARANTEED AT 24mA
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 2.0V to 3.6V (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 574
- LATCH-UP PERFORMANCE EXCEEDS 500mA
- ESD PERFORMANCE: HBM >2000V; MM > 200V





M	T
(Micro Package)	(TSSOP Package)

ORDER CODES :

74LCX574M 74LCX574T

DESCRIPTION

The LCX574 is a low voltage CMOS OCTAL D-TYPE FLIP FLOP with 3 STATE OUTPUT NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal enviroment for both inputs and outputs.

These 8 bit D-Type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

On the positive transition of the clock, the Q outputs will be set to logic state that were setup at the D inputs.

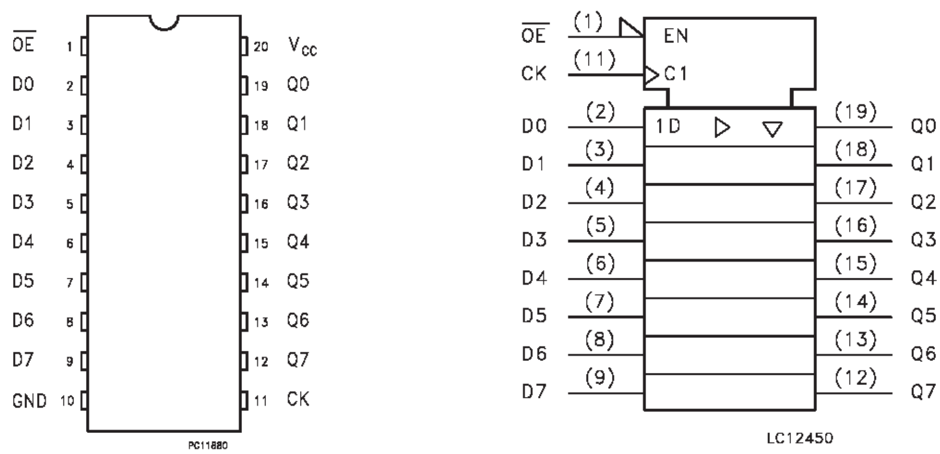
While the ($\overline{OE}$) input is low, the 8 outputs will be in al normal logic state (high or low logic level) and while high level, the outputs will be in a high impedance state.

The output control does not affect the internal operation of flip flop, that is, the old data can be retained or the new data can be entered even while the outputs are off.

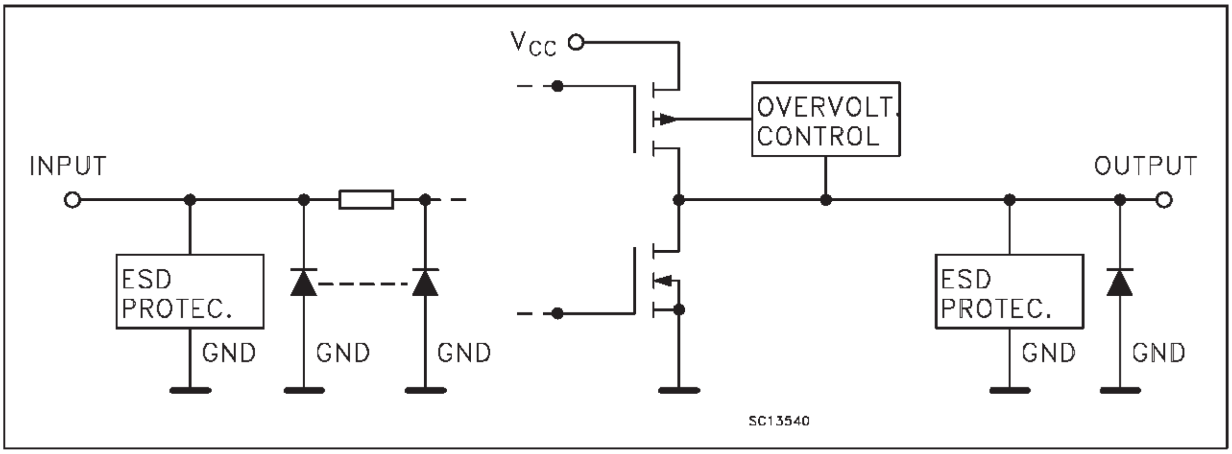
It has same speed performance at 3.3V than 5V, AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

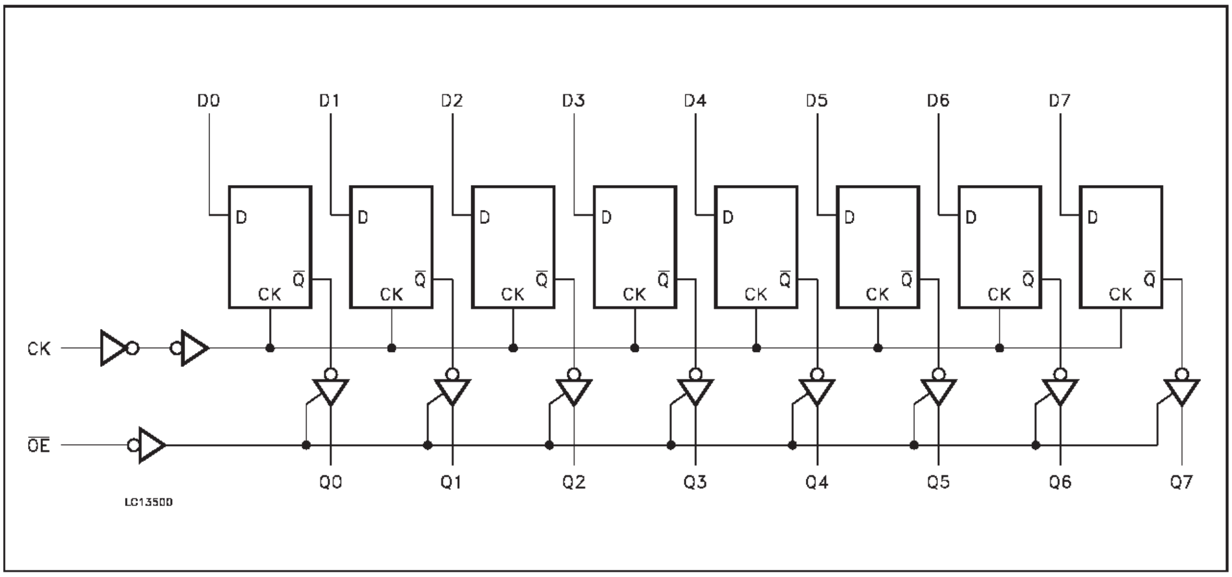
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3 State Outputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	↓	X	NO CHANGE
L	↑	L	L
L	↑	H	H

X: "H" or "L"
Z: High Impedance

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 7.0	V
V_I	DC Input Voltage	-0.5 to + 7.0	V
V_O	DC Output Voltage (OFF state)	-0.5 to + 7.0	V
V_O	DC Output Voltage (High or Low State) (note1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note2)	± 50	mA
I_O	DC Output Source/Sink Current	± 50	mA
I_{CC}	DC Supply Current per Supply Pin	± 100	mA
I_{GND}	DC Ground Current per Supply Pin	± 100	mA
T_{stg}	Storage Temperature	-65 to +150	^oC
T_L	Lead Temperature (10 sec)	300	^oC

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
1) I_O absolute maximum rating must be observed
2) V_O < GND, V_O > V_{CC}

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2.0 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (OFF state)	0 to 5.5	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 3.0 to 3.6V)	± 24	mA
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 2.7 to 3.0V)	± 12	mA
T_{op}	Operating Temperature:	-40 to +85	^oC
dt/dv	Input Transition Rise or Fall Rate (V_{CC} = 3.0V) (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.5V to 3.6V
2) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value		Unit
		V_{CC} (V)			-40 to 85 °C		
					Min.	Max.	
V_{IH}	High Level Input Voltage	2.7 to 3.6			2.0		V
V_{IL}	Low Level Input Voltage	2.7 to 3.6				0.8	V
V_{OH}	High Level Output Voltage	2.7 to 3.6	V_I = V_{IH} or V_{IL}	I_O=-100 µA	V_{CC}-0.2		V
		2.7		I_O=-12 mA	2.2		
		3.0		I_O=-18 mA	2.4		
				I_O=-24 mA	2.2		
V_{OL}	Low Level Output Voltage	2.7 to 3.6	V_I = V_{IH} or V_{IL}	I_O=100 µA		0.2	V
		2.7		I_O=12 mA		0.4	
		3.0		I_O=16 mA		0.4	
		3.0		I_O=24 mA		0.55	
I_I	Input Leakage Current	2.7 to 3.6	V_I = 0 to 5.5 V			±5	µA
I_{OZ}	3 State Output Leakage Current	2.7 to 3.6	V_I = V_{IH} or V_{IL} V_O = 0 to 5.5V			±5	µA
I_{off}	Power Off Leakage Current	0	V_I or V_O = 5.5V			100	µA
I_{CC}	Quiescent Supply Current	2.7 to 3.6	V_I = V_{CC} or GND			10	µA
			V_I or V_O = 3.6 to 5.5V			±10	
ΔI_{CC}	ICC incr. per input	2.7 to 3.6	V_{IH} = V_{CC} -0.6V			500	µA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1)	3.3	C_L = 50 pF V_{IL} = 0 V V_{IH} = 3.3V		0.8		V
V_{OLV}					-0.8		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input t_r = t_f = 2.5 ns)

Symbol	Parameter	Test Condition		Value		Unit
		V_{CC} (V)	Waveform	-40 to 85 °C		
				Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time	2.7	1	1.5	9.5	ns
		3.0 to 3.6		1.5	8.5	
t_{PZL} t_{PZH}	Output Enable Time to HIGH and LOW level	2.7	2	1.5	9.5	ns
		3.0 to 3.6		1.5	8.5	
t_{PLZ} t_{PHZ}	Output Disable Time from HIGH and LOW level	2.7	2	1.5	8.5	ns
		3.0 to 3.6		1.5	7.5	
t_s	Setup Time, HIGh or LOW level Dn to CK	2.7	1	2.5		ns
		3.0 to 3.6		2.5		
t_h	Hold Time, HIGh or LOW level Dn to CK	2.7	1	1.5		ns
		3.0 to 3.6		1.5		
t_w	CK Pulse Width, HIGH or LOW	2.7	3	3.3		ns
		3.0 to 3.6		3.3		
f_{MAX}	Clock Pulse Frequency	3.0 to 3.6	1	150		MHz
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1, 2)	3.0 to 3.6			1.0	ns

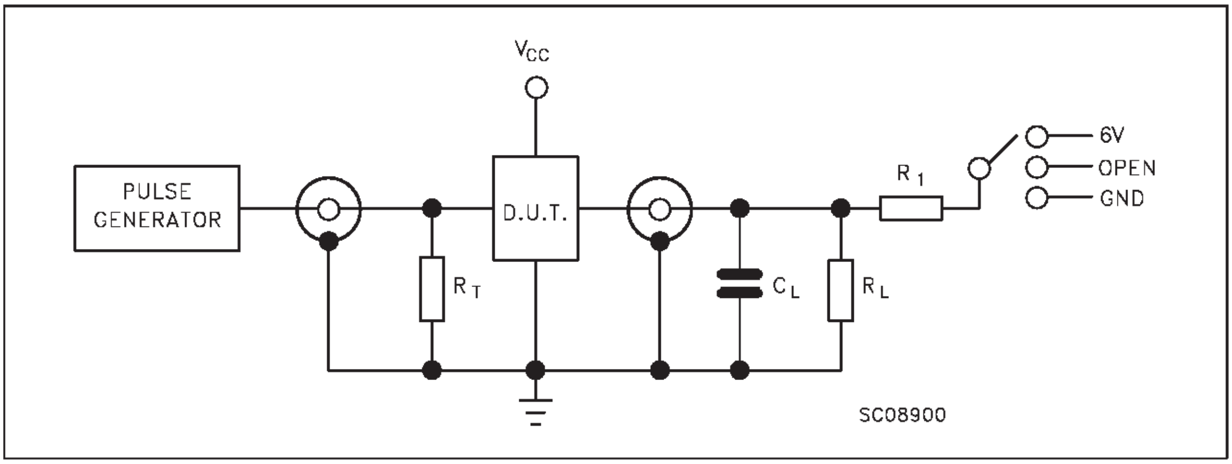
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{pHLn}|$)
2) Parameter guaranteed by design

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance	3.3	V_{IN} = 0 to V_{CC}		6		pF
C_{OUT}	Output Capacitance	3.3	V_{IN} = 0 to V_{CC}		12		pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3	f_{IN} = 10MHz V_{IN} = 0 or V_{CC}		25		pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/8$ (per Flip-Flop)

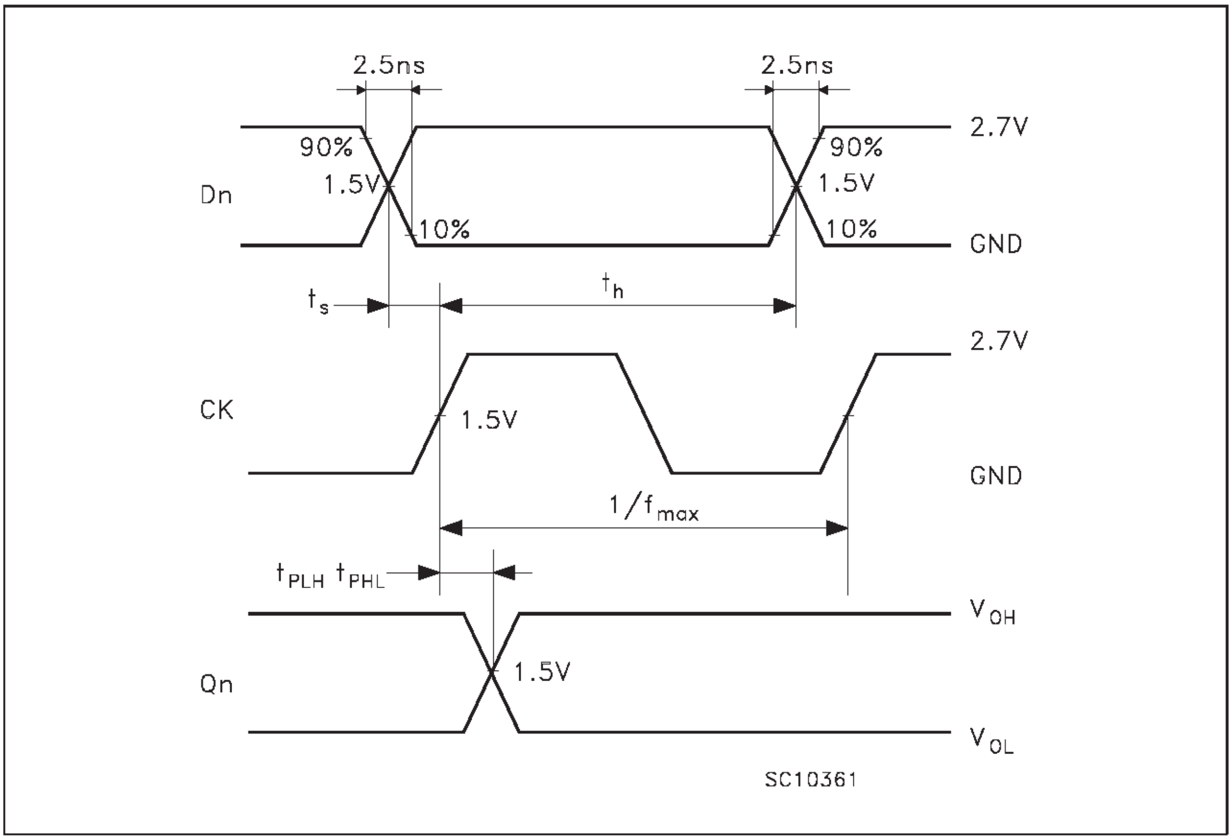
TEST CIRCUIT



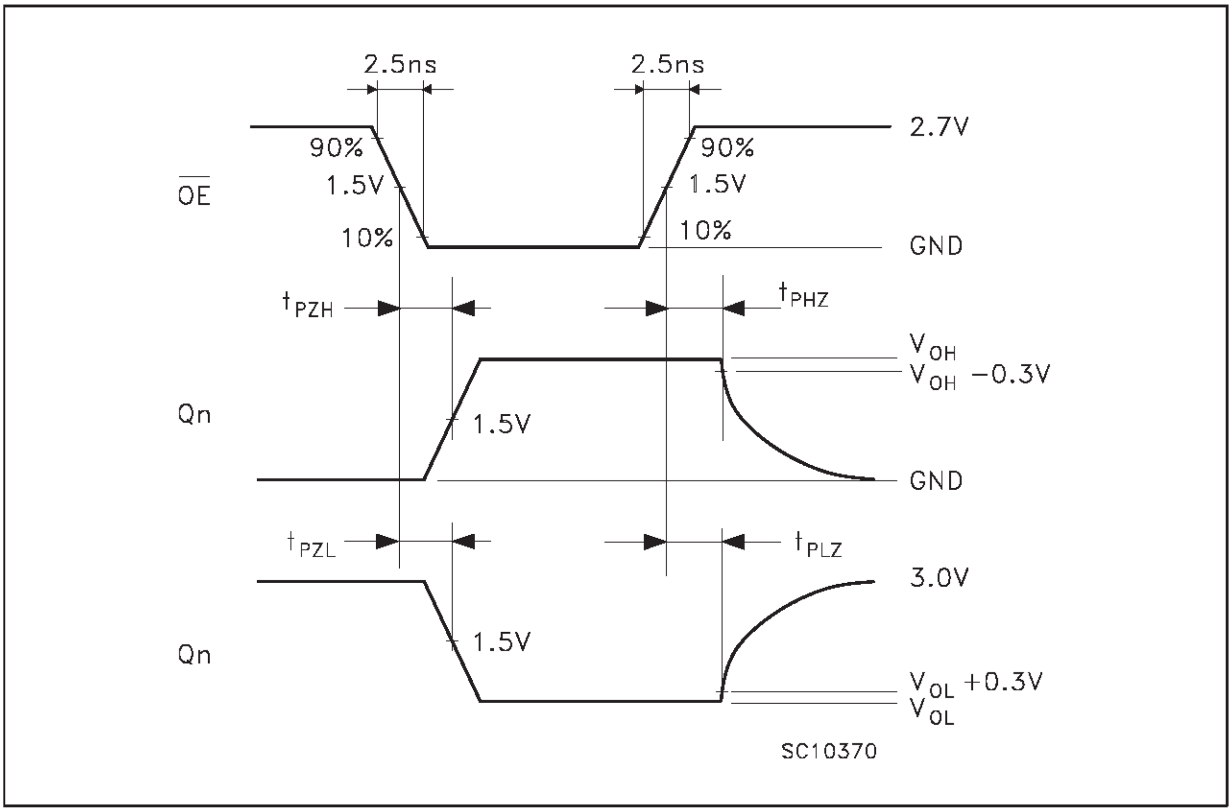
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50 pF or equivalent (includes jig and probe capacitance)
R_L = R_1 = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

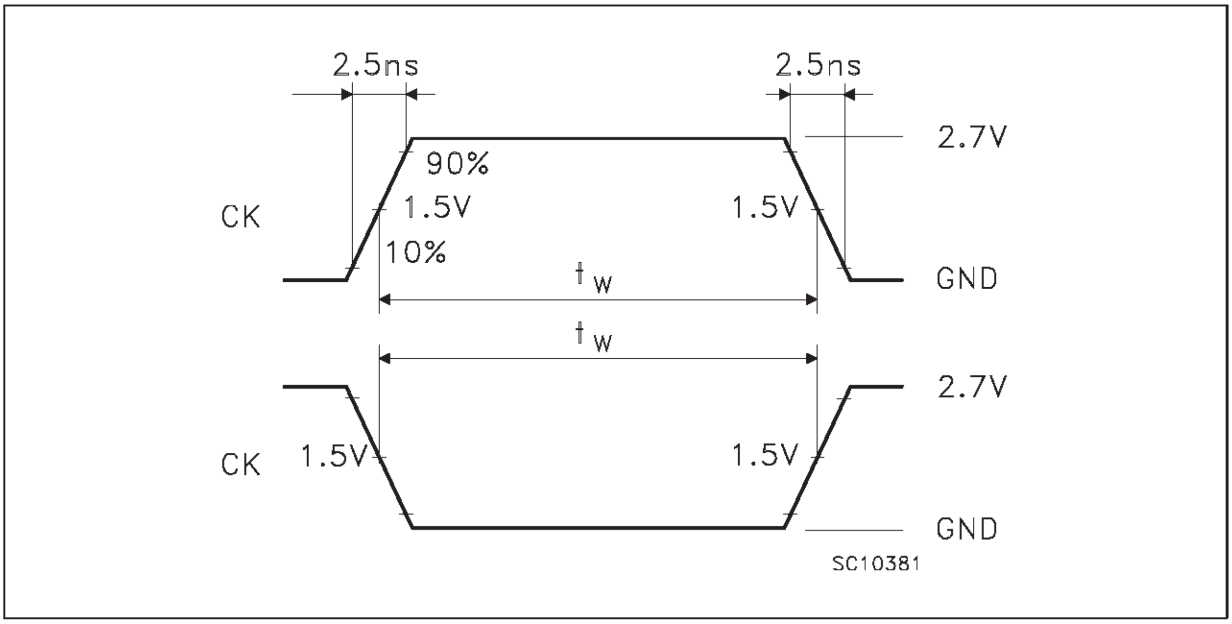
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)

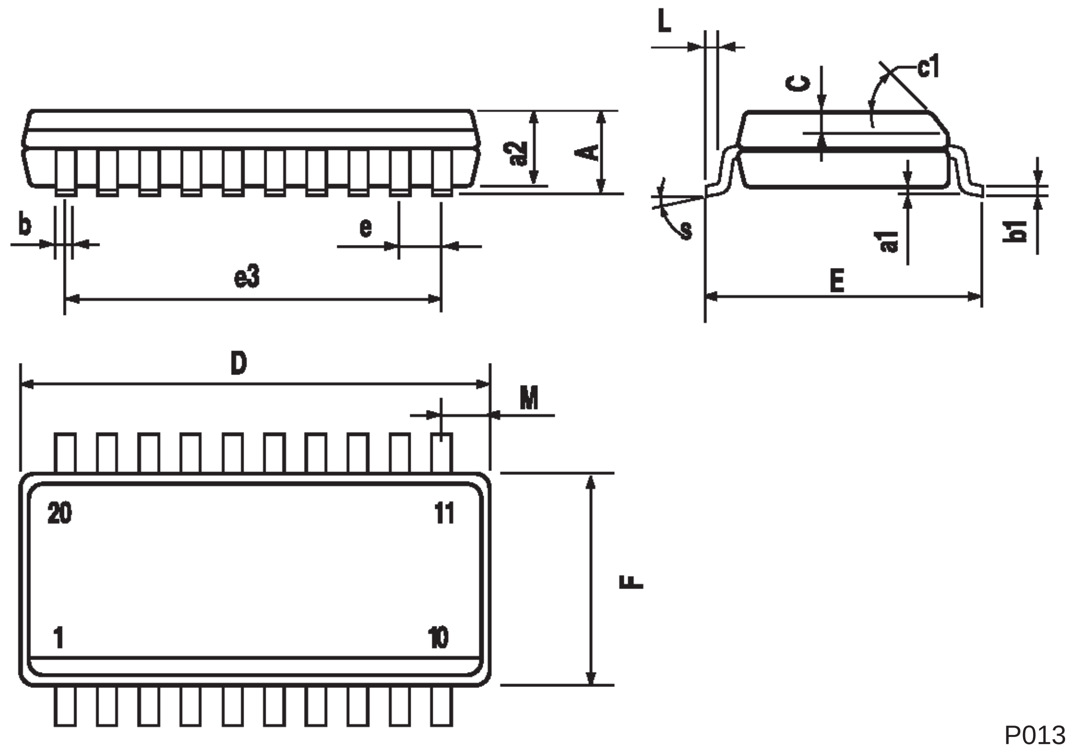


WAVEFORM 3: PULSE WIDTH



SO-20 MECHANICAL DATA

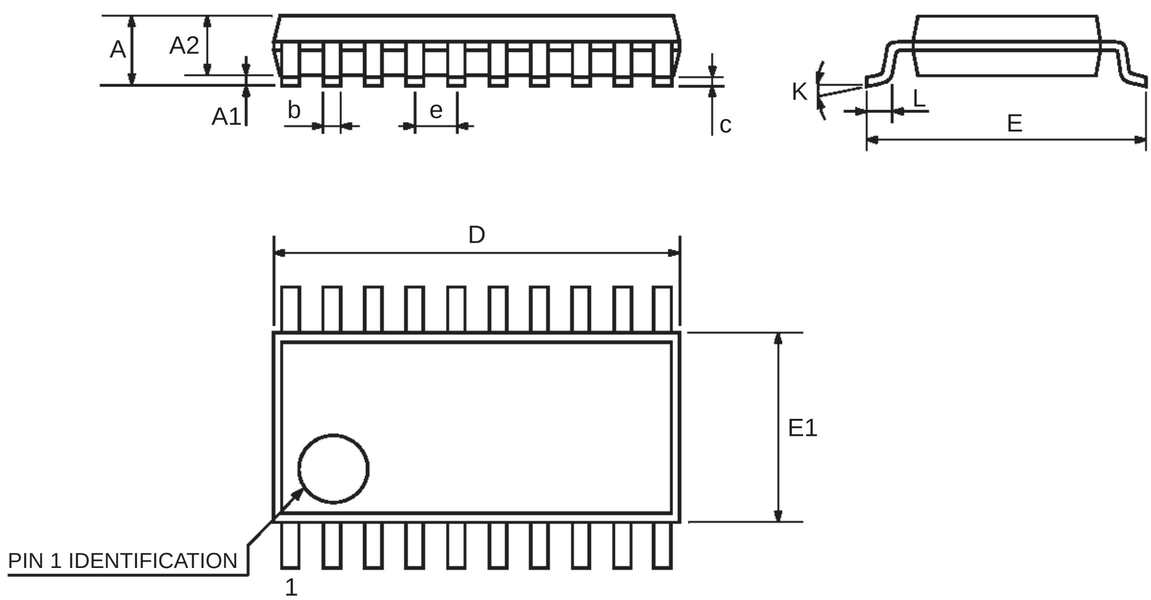
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



P013L

TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0^o	4^o	8^o	0^o	4^o	8^o
L	0.50	0.60	0.70	0.020	0.024	0.028



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