

Features

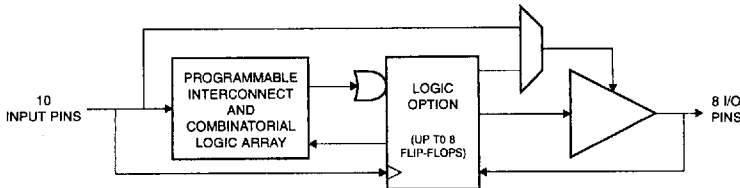
- Industry Standard Architecture Emulates Many 20-Pin PALs® Low Cost Easy-to-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Devices 7.5 ns Maximum Pin-to-Pin Delay
- Several Power Saving Options

Device	Icc, Stand-By	Icc, Active
ATF16V8B	50 mA	55 mA
ATF16V8BQ	35 mA	40 mA
ATF16V8BL	5 mA	30 mA
ATF16V8BQL	5 mA	20 mA

- CMOS and TTL Compatible Inputs and Outputs Input and I/O Pull-Up Resistors
- Advanced Flash Technology Reprogrammable 100% Tested
- High Reliability CMOS Process 20 Year Data Retention 100 Erase/Write Cycles 2,000 V ESD Protection 200 mA Latchup Immunity
- Full Military, Commercial, and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

High Performance Flash PLD

Block Diagram



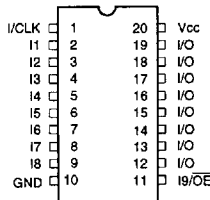
Description

The ATF16V8B is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 7.5 ns and power dissipation as low as 10 mA are offered. All speed ranges are specified over the full 5 V ± 10% range for military and industrial temperature ranges, and 5 V ± 5% for commercial temperature ranges.

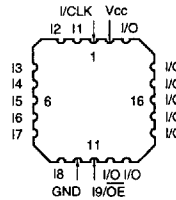
Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
OE	Output Enable
VCC	+5 V Supply

DIP/SOIC



LCC/PLCC





Absolute Maximum Ratings*

Temperature Under Bias.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-2.0 V to +7.0 V ⁽¹⁾
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0 V to +14.0 V ⁽¹⁾
Programming Voltage with Respect to Ground.....	-2.0 V to +14.0 V ⁽¹⁾

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

1. Minimum voltage is -0.6 V dc, which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC} + 0.75$ V dc, which may overshoot to 7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Conditions

	Commercial	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
Vcc Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units	
I_{IL}	Input or I/O Low Leakage Current	$0 \leq V_{IN} \leq V_{IL}(MAX)$		-150	μA	
I_{IH}	Input or I/O High Leakage Current	$3.5 \leq V_{IN} \leq V_{CC}$		10	μA	
I_{CC}	Power Supply Current, Standby	$V_{CC} = MAX,$ $V_{IN} = MAX,$ Outputs Open	ATF16V8B	Com.	110	mA
				Ind., Mil.	120	mA
I_{CC2}	Clocked Power Supply Current	$V_{CC} = MAX,$ Outputs Open	ATF16V8BL	Com.	10	mA
				Ind., Mil.	15	mA
I_{CC3}	Clocked Power Supply Current	$V_{CC} = MAX,$ Outputs Open, $f=25$ MHz	ATF16V8BL	Com.	15	mA/MHz ⁽²⁾
				Ind., Mil.	20	mA/MHz ⁽²⁾
I_{CC3}	Clocked Power Supply Current	$V_{CC} = MAX,$ Outputs Open, $f=25$ MHz		Com.	115	mA
				Ind., Mil.	140	mA
$I_{OS}^{(1)}$	Output Short Circuit Current	$V_{OUT} = 0.5$ V		-130	mA	
V_{IL}	Input Low Voltage		-0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	$V_{CC}+0.75$	V	
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or $V_{IL},$ $V_{CC} = MIN$	$I_{OL} = 24$ mA	Com., Ind.	0.5	V
			$I_{OL} = 16$ mA	Mil.	0.5	V
V_{OH}	Output High Voltage	$V_{IN}=V_{IH}$ or $V_{IL},$ $V_{CC}=MIN$	$I_{OH} = -4.0$ mA	2.4	V	

- Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. Low frequency only, contact factory for I_{CC} versus frequency characterization curves.

D.C. Characteristics

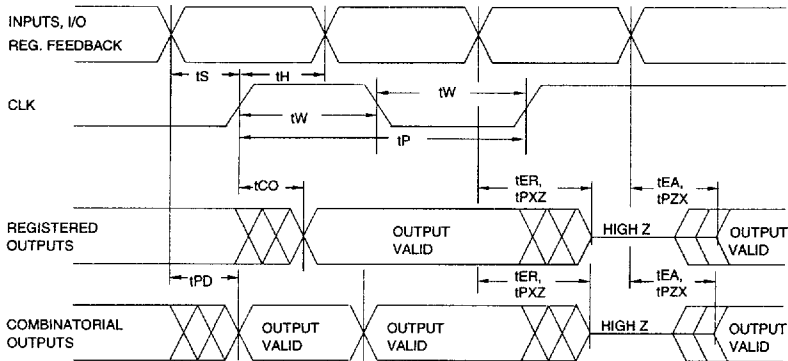
Symbol	Parameter	Condition	Min	Typ	Max	Units	
I_{IL}	Input or I/O Low Leakage Current	$0 \leq V_{IN} \leq V_{IL}(MAX)$		-35	-100	μA	
I_{IH}	Input or I/O High Leakage Current	$3.5 \leq V_{IN} \leq V_{CC}$			10	μA	
I_{CC}	Power Supply Current, Standby	$V_{CC} = MAX,$ $V_{IN} = MAX,$ Outputs Open	B-7, -10	Com.	55	85	mA
				Ind., Mil.	55	95	mA
			B-15, -25	Com.	50	75	mA
				Ind., Mil.	50	80	mA
			BQ-10	Com.	35	55	mA
			BL-15, BQL-15, -25	Com.	5	10	mA
		Ind., Mil.	5	15	mA		
I_{CC2}	Clocked Power Supply Current	$V_{CC} = MAX,$ Outputs Open	BL-15, BQL-15, -25	Com.	1	$mA/MHz^{(2)}$	
				Ind., Mil.	1	$mA/MHz^{(2)}$	
I_{CC3}	Clocked Power Supply Current	$V_{CC} = MAX,$ Outputs Open, $f=15 MHz$	B-7, -10	Com.	60	90	mA
				Ind., Mil.	60	100	mA
			B-15, -25	Com.	55	85	mA
				Ind., Mil.	55	95	mA
			BQ-10	Com.	40	55	mA
			BL-15	Com.	30	40	mA
				Ind., Mil.	30	45	mA
			BQL-15, -25	Com.	20	35	mA
		Ind., Mil.	20	40	mA		
$I_{OS}^{(1)}$	Output Short Circuit Current	$V_{OUT} = 0.5 V$			-130	mA	
V_{IL}	Input Low Voltage		-0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		$V_{CC}+0.75$	V	
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or $V_{IL},$ $V_{CC} = MIN$	$I_{OL} = 24 mA$	Com., Ind.		0.5	V
			$I_{OL} = 16 mA$	Mil.		0.5	V
V_{OH}	Output High Voltage	$V_{IN}=V_{IH}$ or $V_{IL},$ $V_{CC}=MIN$	$I_{OH} = -4.0 mA$	2.4		V	

- Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. Low frequency only. See Supply Current versus Input Frequency curves.





A.C. Waveforms ⁽¹⁾



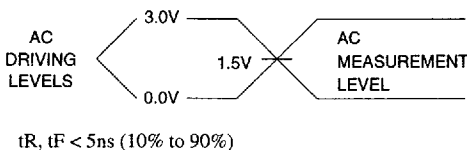
Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics ⁽¹⁾

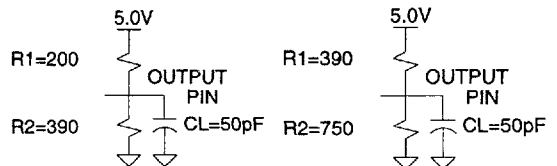
Symbol	Parameter	-7		-10		-15		-25		Units		
		Min	Max	Min	Max	Min	Max	Min	Max			
t _{PD}	Input or Feedback to Non-Registered Output	8 outputs switching		3	7.5	3	10	3	15	3	25	ns
		1 output switching		7								ns
t _{CF}	Clock to Feedback		3		6		8		10		ns	
t _{CO}	Clock to Output	2	5	2	7	2	10	2	12		ns	
t _S	Input or Feedback Setup Time	5		7.5		12		15			ns	
t _H	Hold Time	0		0		0		0			ns	
t _P	Clock Period	8		12		16		24			ns	
t _w	Clock Width	4		6		8		12			ns	
F _{MAX}	External Feedback 1/(t _S +t _{CO})	100		68		45		37			MHz	
	Internal Feedback 1/(t _S +t _{CF})	125		74		50		40			MHz	
	No Feedback 1/(t _P)	125		83		62		41			MHz	
t _{EA}	Input to Output Enable — Product Term	3	9	3	10	3	15	3	20		ns	
t _{ER}	Input to Output Disable — Product Term	2	9	2	10	2	15	2	20		ns	
t _{PZX}	OE pin to Output Enable	2	6	2	10	2	15	2	20		ns	
t _{PXZ}	OE pin to Output Disable	1.5	6	1.5	10	1.5	15	1.5	20		ns	

Note: 1. See ordering information for valid part numbers and speed grades.

Input Test Waveforms and Measurement Levels:



Output Test Loads:



Pin Capacitance (f = 1 MHz, T = 25°C) ⁽¹⁾

	Typ	Max	Units	Conditions
C _{IN}	5	8	pF	V _{IN} = 0 V
C _{OUT}	6	8	pF	V _{OUT} = 0 V

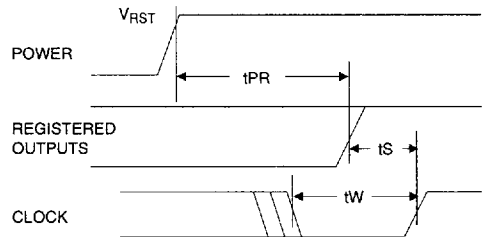
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The registers in the ATF16V8Bs are designed to reset during power up. At a point delayed slightly from VCC crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how VCC actually rises in the system, the following conditions are required:

- 1) The VCC rise must be monotonic,
- 2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
- 3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t _{PR}	Power-Up Reset Time	600	1,000	ns
V _{RST}	Power-Up Reset Voltage	3.8	4.5	V

Preload of Registered Outputs

The ATF16V8B's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Electronic Signature Word

There are 64-bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8B fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

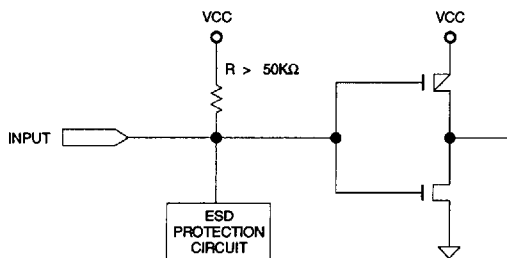
Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See *CMOS PLD Programming Hardware & Software Support* for information on software/programming.

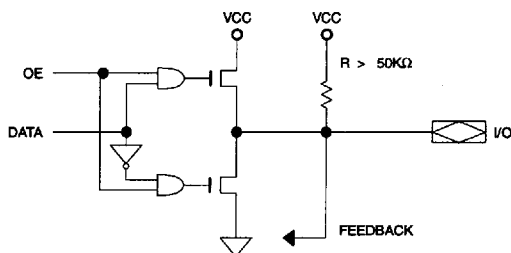
Input and I/O Pull-Ups

The ATF16V8B and ATF16V8BL have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to Vcc. This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be overdriven by TTL-compatible drivers (see input and I/O diagrams below).

Input Diagram



I/O Diagram



Functional Logic Diagram Description

The Logic Option and Functional Diagrams describe the ATF16V8B architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF16V8B can be configured in one of three different modes. Each mode makes the ATF16V8B look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8B universal architecture can be programmed to emulate many 20-pin PAL devices. These architectural subsets

can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8B can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

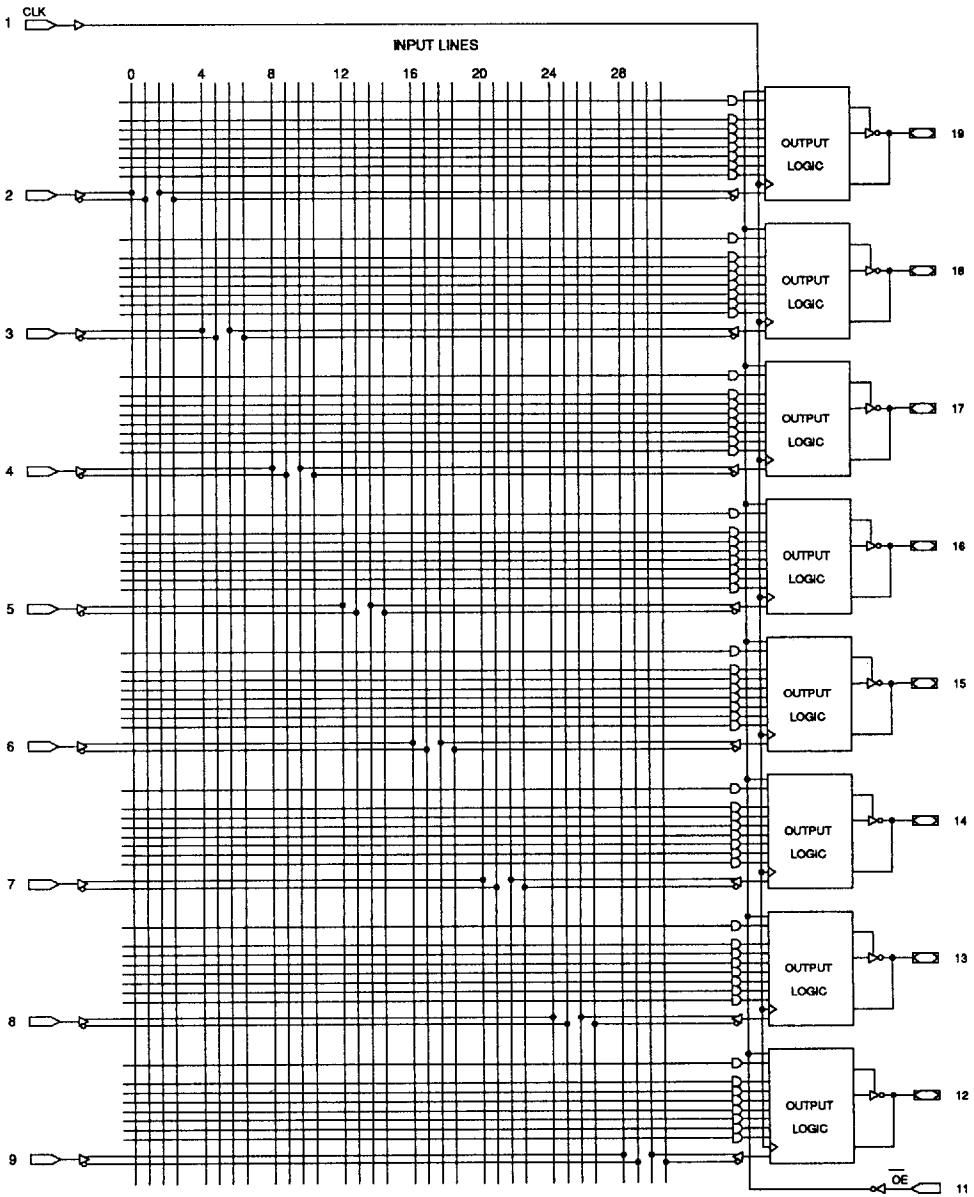
Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the content of the ATF16V8B. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/IC	GAL16V8_R ⁽¹⁾	GAL16V8_C7 ⁽¹⁾	GAL16V8_C8 ⁽¹⁾	GAL16V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL16V8A
PLDesigner	P16V8R	P16V8C	P16V8C	P16V8A
Tango-PLD	G16V8R	G16V8C	G16V8AS	G16V8

Note: 1. Only applicable for version 3.4 or lower.

Registered Mode Logic Diagram



1



ATF16V8B Complex Mode

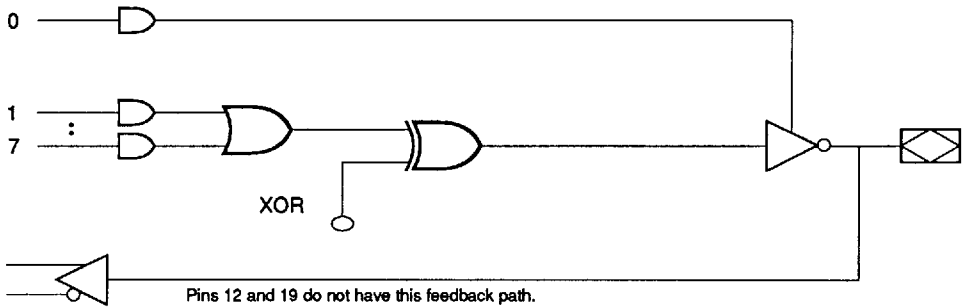
PAL Device Emulation/PAL Replacement

In the Complex Mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

16L8
16H8
16P8

Complex Mode Option



ATF16V8B Complex Mode

PAL Device Emulation/PAL Replacement

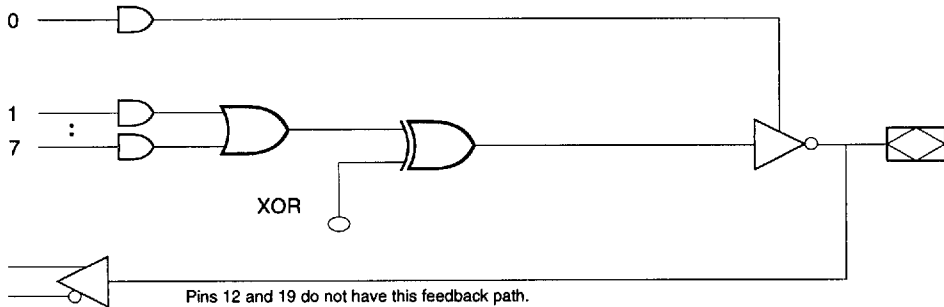
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Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

- 16L8
- 16H8
- 16P8

1

Complex Mode Option



ATF16V8B Simple Mode

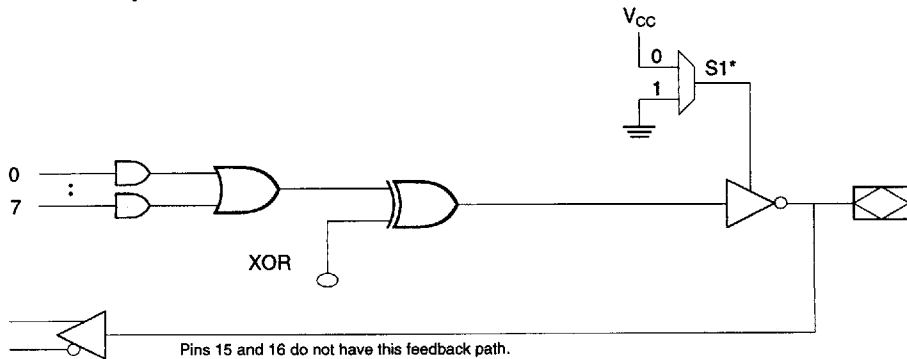
PAL Device Emulation / PAL Replacement

In the Simple Mode, 8 product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without OE control. The following simple PALs can be emulated using this mode:

- | | | |
|------|------|------|
| 10L8 | 10H8 | 10P8 |
| 12L6 | 12H6 | 12P6 |
| 14L4 | 14H4 | 14P4 |
| 16L2 | 16H2 | 16P2 |

Simple Mode Option

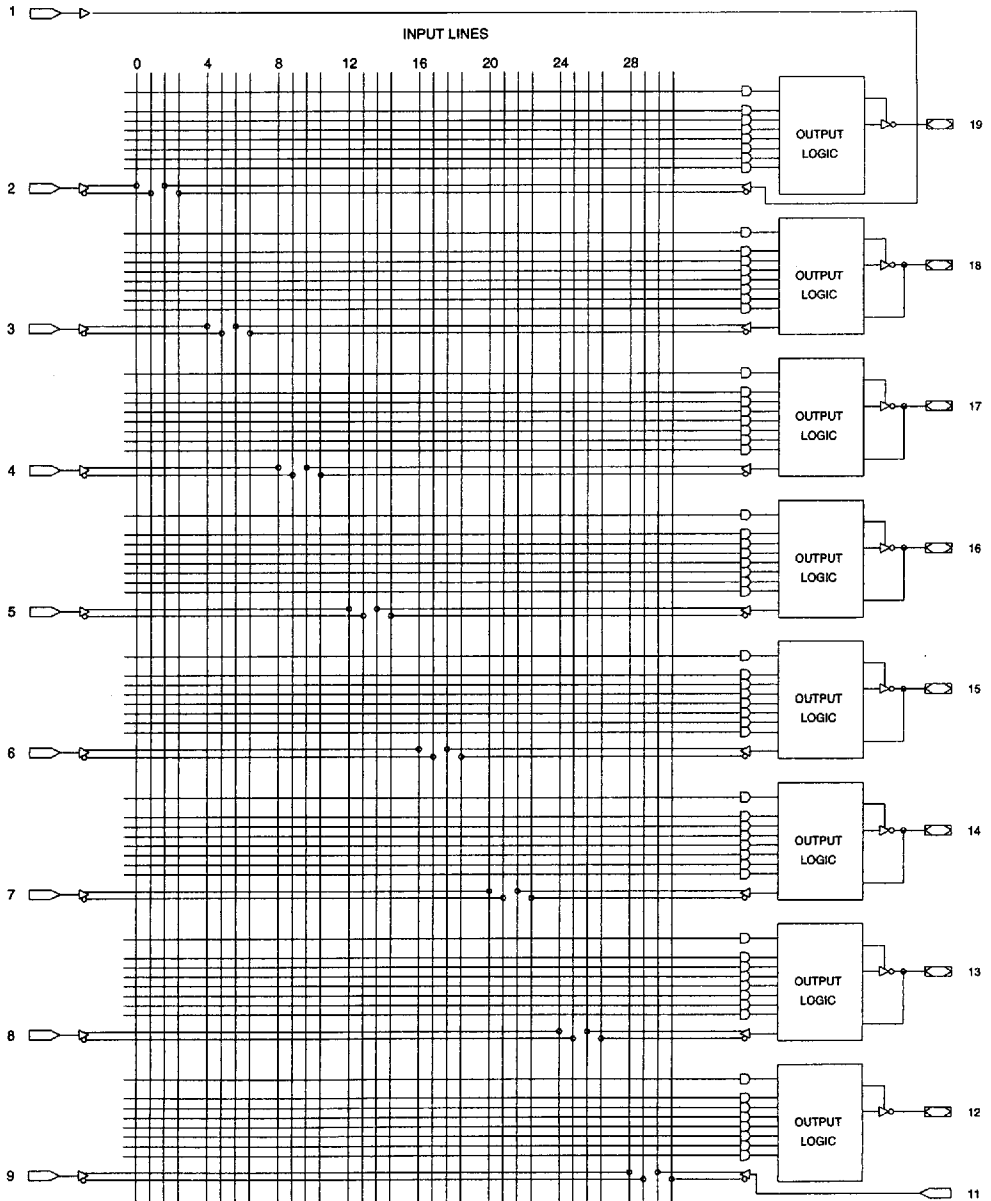


* - Pins 15 and 16 are always enabled.

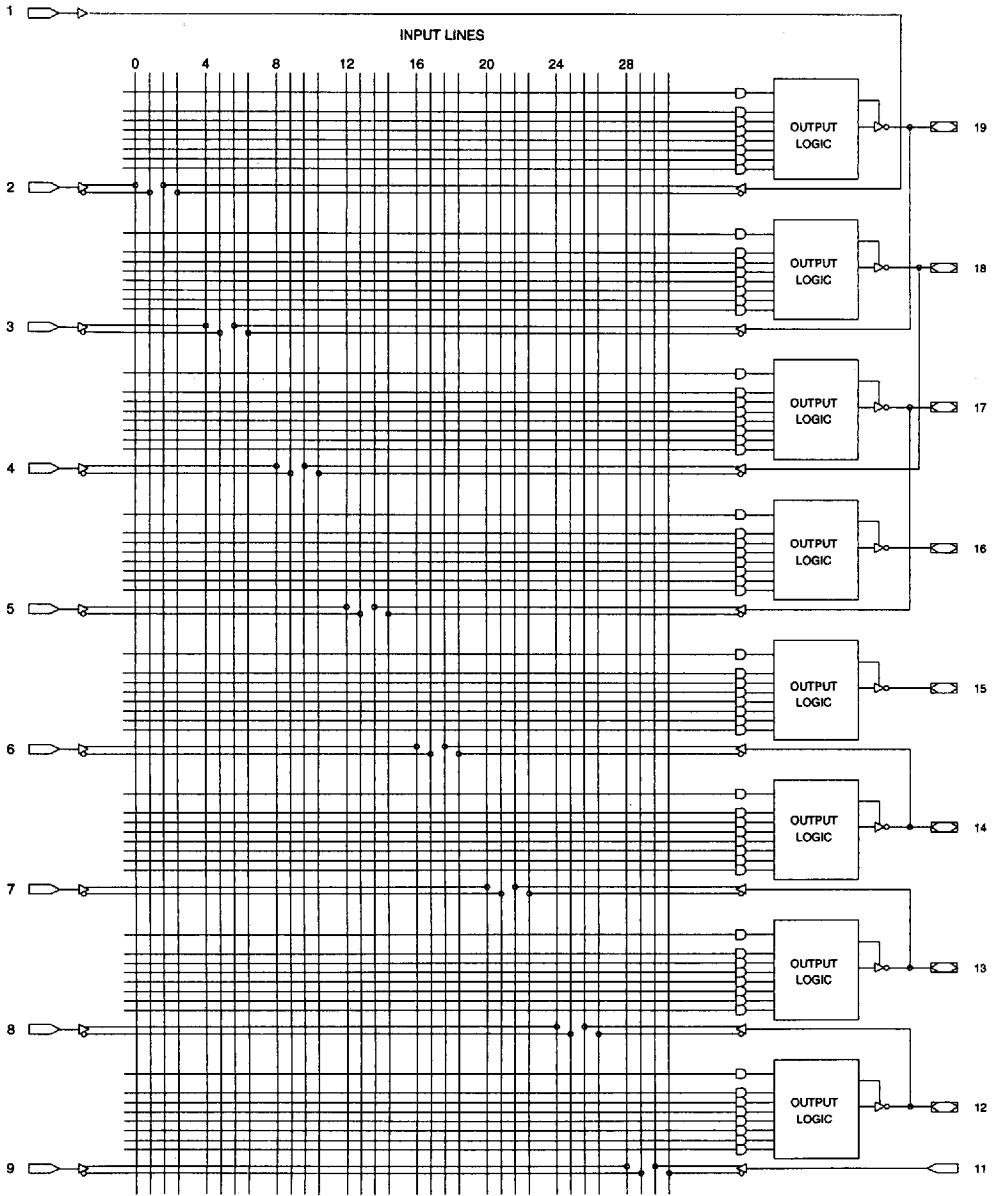




Complex Mode Logic Diagram

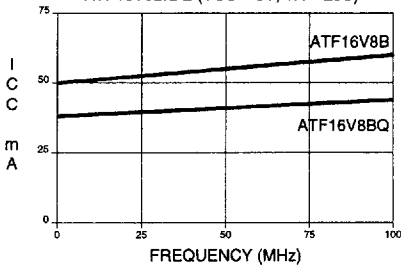


Simple Mode Logic Diagram



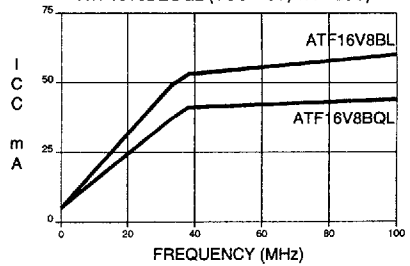
SUPPLY CURRENT vs. INPUT FREQUENCY

ATF16V8B/BQ (VCC = 5V, TA = 25C)



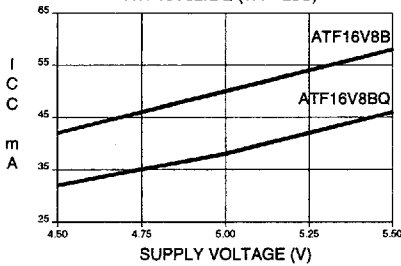
SUPPLY CURRENT vs. INPUT FREQUENCY

ATF16V8BL/BQL (VCC = 5V, TA = 25C)



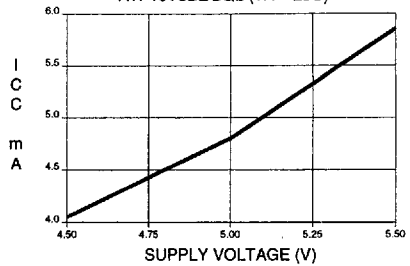
SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATF16V8B/BQ (TA = 25C)



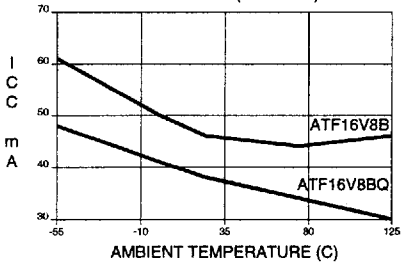
SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATF16V8BL/BQL (TA = 25C)



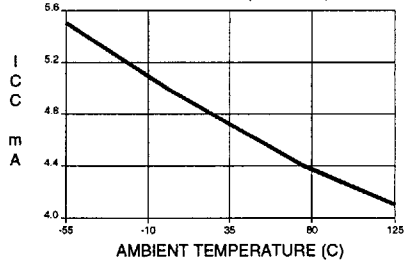
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATF16V8B/BQ (VCC = 5V)



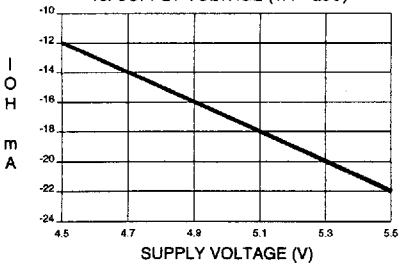
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATF16V8BL/BQL (VCC = 5V)



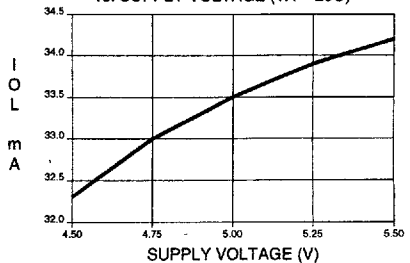
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (TA = 25C)

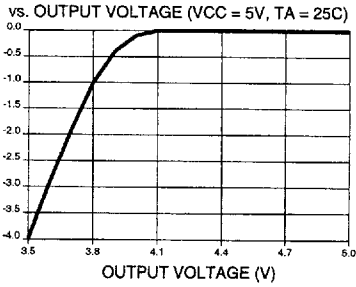


OUTPUT SINK CURRENT

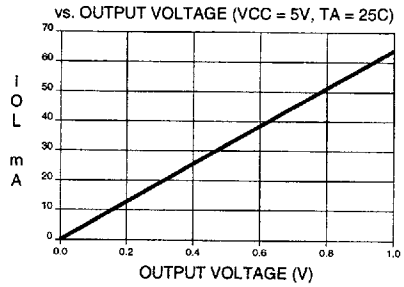
vs. SUPPLY VOLTAGE (TA = 25C)



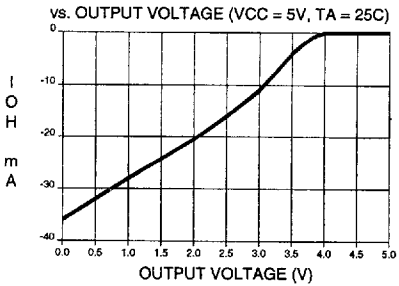
OUTPUT SOURCE CURRENT



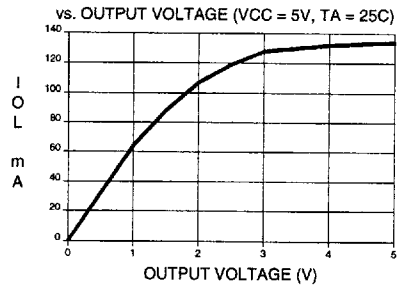
OUTPUT SINK CURRENT



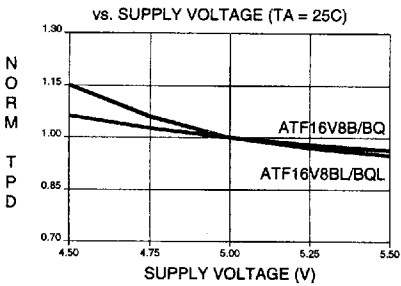
OUTPUT SOURCE CURRENT



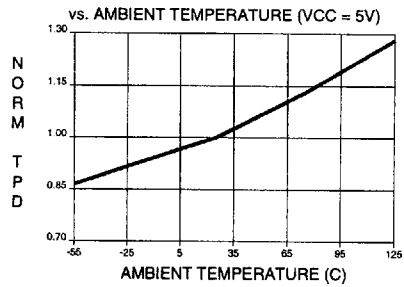
OUTPUT SINK CURRENT



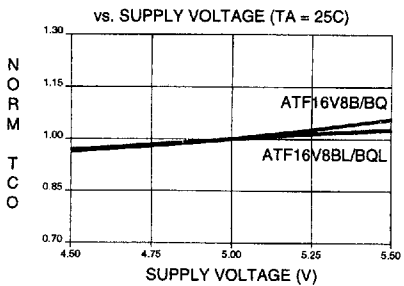
NORMALIZED TPD



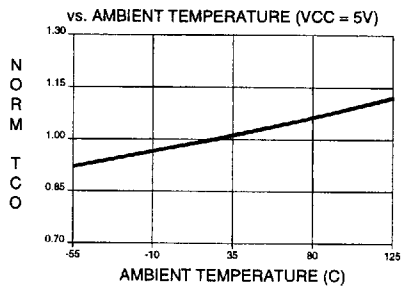
NORMALIZED TPD

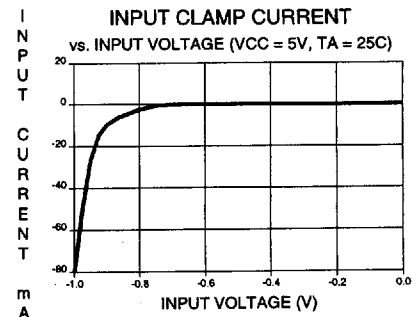
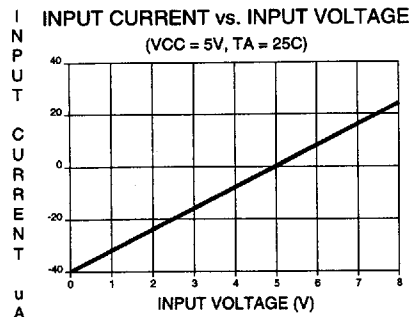
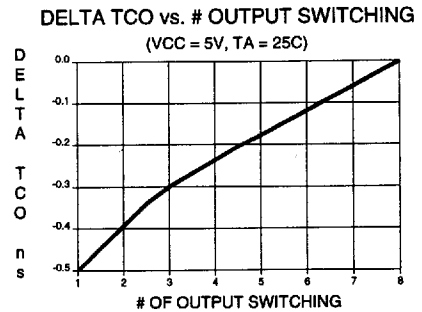
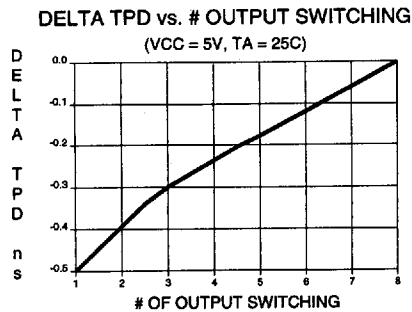
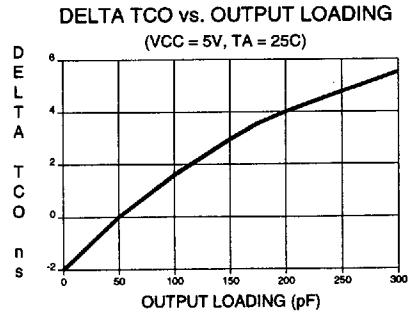
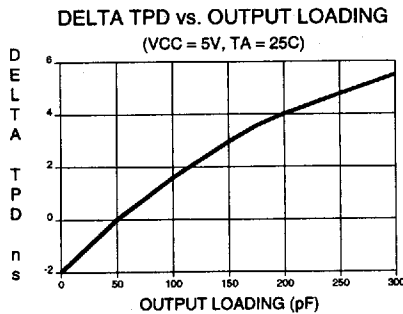
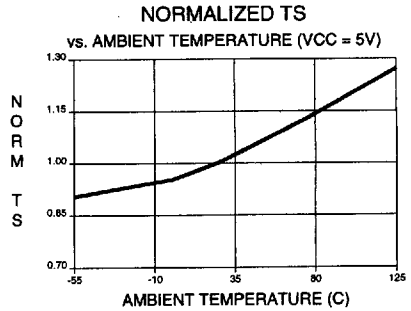
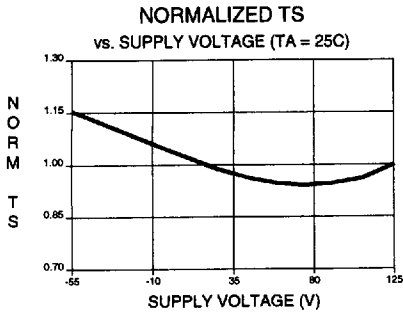


NORMALIZED TCO



NORMALIZED TCO





Ordering Information

t _{PD} (ns)	t _s (ns)	t _{CO} (ns)	Ordering Code	Package	Operation Range
7.5	5	5	ATF16V8B-7GC	20D3	Commercial (0°C to 70°C)
			ATF16V8B-7JC	20J	
			ATF16V8B-7PC	20P3	
			ATF16V8B-7SC	20S	
10	7.5	7	ATF16V8B-10GC	20D3	Commercial (0°C to 70°C)
			ATF16V8B-10JC	20J	
			ATF16V8B-10PC	20P3	
			ATF16V8B-10SC	20S	
		ATF16V8B-10GI	20D3	Industrial (-40°C to 85°C)	
		ATF16V8B-10JI	20J		
		ATF16V8B-10PI	20P3		
		ATF16V8B-10SI	20S		
		ATF16V8B-10GM	20D3	Military (-55°C to 125°C)	
		ATF16V8B-10NM	20L		
		ATF16V8B-10GM/883	20D3		
		ATF16V8B-10NM/883	20L		
15	12	10	ATF16V8B-15GC	20D3	Commercial (0°C to 70°C)
			ATF16V8B-15JC	20J	
			ATF16V8B-15PC	20P3	
			ATF16V8B-15SC	20S	
		ATF16V8B-15GI	20D3	Industrial (-40°C to 85°C)	
		ATF16V8B-15JI	20J		
		ATF16V8B-15PI	20P3		
		ATF16V8B-15SI	20S		
		ATF16V8B-15GM	20D3	Military (-55°C to 125°C)	
		ATF16V8B-15NM	20L		
		ATF16V8B-15GM/883	20D3		
		ATF16V8B-15NM/883	20L		
25	15	12	ATF16V8B-25GC	20D3	Commercial (0°C to 70°C)
			ATF16V8B-25JC	20J	
			ATF16V8B-25PC	20P3	
			ATF16V8B-25SC	20S	
		ATF16V8B-25GI	20D3	Industrial (-40°C to 85°C)	
		ATF16V8B-25JI	20J		
		ATF16V8B-25PI	20P3		
		ATF16V8B-25SI	20S		



Ordering Information

t _{pd} (ns)	t _s (ns)	t _{co} (ns)	Ordering Code	Package	Operation Range
15	12	10	ATF16V8BL-15GC	20D3	Commercial (0°C to 70°C)
			ATF16V8BL-15JC	20J	
			ATF16V8BL-15PC	20P3	
			ATF16V8BL-15SC	20S	
			ATF16V8BL-15GI	20D3	Industrial (-40°C to 85°C)
			ATF16V8BL-15JI	20J	
			ATF16V8BL-15PI	20P3	
			ATF16V8BL-15SI	20S	
			ATF16V8BL-15GM	20D3	Military (-55°C to 125°C)
			ATF16V8BL-15NM	20L	
			ATF16V8BL-15GM/883	20D3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			ATF16V8BL-15NM/883	20L	
10	7.5	7	ATF16V8BQ-10JC	20J	Commercial (0°C to 70°C)
			ATF16V8BQ-10PC	20P3	
15	12	10	ATF16V8BQL-15JC	20J	Commercial (0°C to 70°C)
			ATF16V8BQL-15PC	20P3	
			ATF16V8BQL-15SC	20S	
25	15	12	ATF16V8BQL-25JC	20J	Commercial (0°C to 70°C)
			ATF16V8BQL-25PC	20P3	
			ATF16V8BQL-25SC	20S	
			ATF16V8BQL-25JI	20J	
ATF16V8BQL-25PI	20P3				
			ATF16V8BQL-25SI	20S	
			ATF16V8BQL-25GM	20D3	Military (-55°C to 125°C)
			ATF16V8BQL-25NM	20L	
			ATF16V8BQL-25GM/883	20D3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			ATF16V8BQL-25NM/883	20L	

Package Type

20D3	20 Lead, 0.300" Wide, Ceramic Dual Inline Package (Cerdip)
20J	20 Lead, Plastic J-Leaded Chip Carrier (PLCC)
20L	20 Pad, Ceramic Leadless Chip Carrier (LCC)
20P3	20 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)