FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21371-1E

ASSP

Fractional-N PLL Frequency Synthesizer

MB15F83UL

■ DESCRIPTION

The Fujitsu MB15F83UL is Fractional-N Phase Locked Loop (PLL) frequency synthesizer with fast lock up function.

The Fractional-N PLL operating up to 2000 MHz and the integer PLL operating up to 600 MHz are integrated on one chip.

The MB15F83UL is used, as charge pump which is well-balanced output current with 1.5 mA and 6 mA selectable by serial data, direct power save control and digital lock detector. In addition, the MB15F83UL adopts a new architecture to achieve fast lock.

The new package (Thin Bump Chip Carrier20) decreases a mount area of MB15F83UL more than 30% comparing with the former B.C.C.16 (for dual PLL, MB15F03SL) .

The MB15F83UL is ideally suited for wireless mobile communications, such as GSM.

■ FEATURES

- High frequency operation : RF synthesizer : 2000 MHz Max.
  : IF synthesizer : 600 MHz Max.
- Low power supply voltage : V_{CC} = 2.7 V to 3.6 V
- Ultra Low power supply current : I_{CC} = 5.8 mA Typ. (V_{CC} = Vp = 3.0 V, Ta = +25 °C, SW = 0 in IF and RF locking state)

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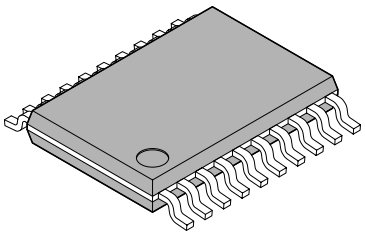
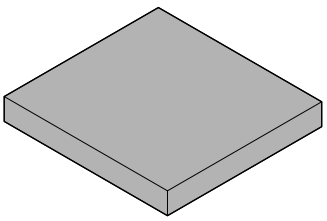
■ PACKAGES

20-pin, Plastic TSSOP



(FPT-20P-M06)

20-pad, Plastic BCC



(LCC-20P-M05)

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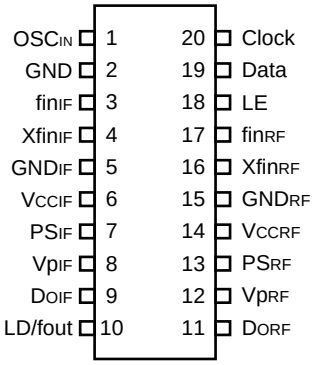
- Direct power saving function : Power supply current in power saving mode
  Typ. 0.1 µA (V_{CC} = Vp = 3.0 V, Ta = +25 °C) , Max. 10 µA (V_{CC} = Vp = 3.0 V)
- Fractional function : modulo 13 fixed (implemented in RF-PLL)
- Dual modulus prescaler : 2000 MHz prescaler (16/17 fixed) /600 MHz prescaler (8/9 or 16/17)
- Serial input programmable reference divider : RF : 7 bit (3 to 127) /IF : 14 bit (3 to 16383)
- Serial input programmable divider consisting of :
  RF section - Binary 4-bit swallow counter : 0 to 15
  - Binary 10-bit programmable counter : 18 to 1,023
  - Binary 4-bit fractional counter numerator : 0 to 15
  IF section - Binary 4-bit swallow counter : 0 to 15
  - Binary 11-bit programmable counter : 3 to 2,047
- On-chip phase comparator for fast lock and low noise
- Operating temperature : Ta = –40 °C to +85 °C
- Small package Bump Chip Carrier.0 (3.4 mm × 3.6 mm × 0.6 mm)

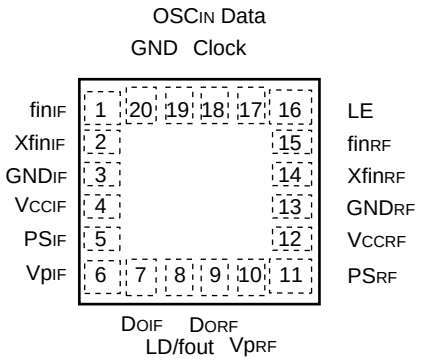
■ PIN ASSIGNMENTS

(TSSOP-20)
TOP VIEW



(FPT-20P-M06)

(BCC-20)
TOP VIEW

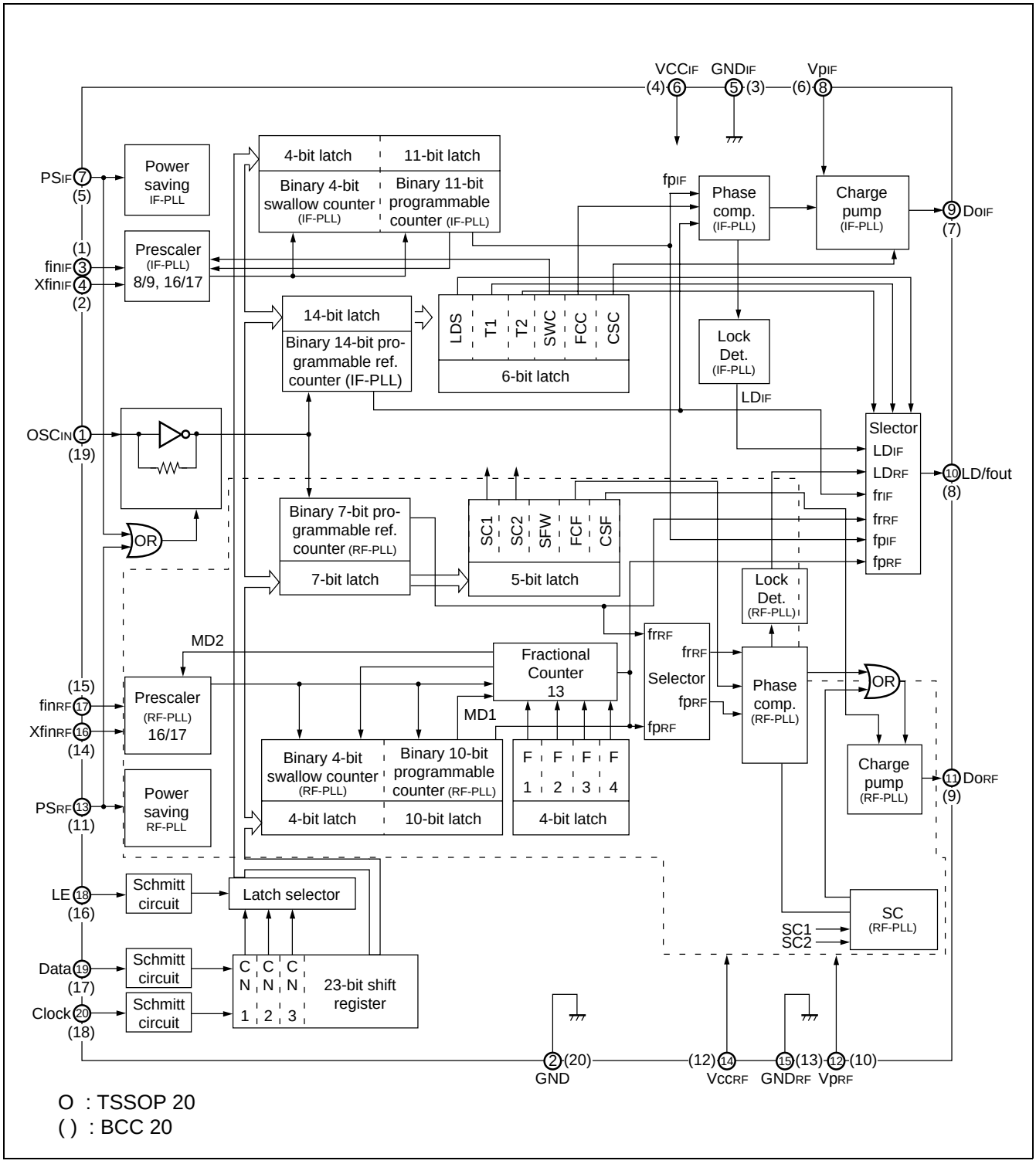


(LCC-20P-M05)

■ PIN DESCRIPTION

Pin no.		Pin name	I/O	Descriptions
TSSOP	BCC			
1	19	OSC_{IN}	I	The programmable reference divider input pin. TCXO should be connected with an AC coupling capacitor.
2	20	GND	—	Ground pin for OSC input buffer and the shift register circuit.
3	1	fin_{IF}	I	Prescaler input pin for the IF-PLL. Connection to an external VCO should be AC coupling.
4	2	$Xfin_{IF}$	I	Prescaler complimentary input pin for the IF-PLL section. This pin should be grounded via a capacitor.
5	3	GND_{IF}	—	Ground pin for the IF-PLL section.
6	4	V_{CCIF}	—	Power supply voltage input pin for the IF-PLL section (except for the charge pump circuit) , the shift register and the oscillator input buffer. When power is OFF, latched data of IF-PLL is lost.
7	5	PS_{IF}	I	Power saving mode control signal pin for the IF-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.) PS_{IF} = “H”; Normal mode / PS_{IF} = “L”; Power saving mode
8	6	Vp_{IF}	—	Power supply voltage input pin for the IF-PLL charge pump.
9	7	Do_{IF}	O	Charge pump output pin for the IF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
10	8	LD/fout	O	Look detect signal output (LD) /phase comparator monitoring output (fout) pins. The output signal is selected by an LDS bit in a serial data. LDS bit = “H”; outputs fout signal / LDS bit = “L”; outputs LD signal
11	9	Do_{RF}	O	Charge pump output pin for the RF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
12	10	Vp_{RF}	—	Power supply voltage input pin for the RF-PLL charge pump.
13	11	PS_{RF}	I	Power saving mode control pin for the RF-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.) PS_{RF} = “H”; Normal mode / PS_{RF} = “L”; Power saving mode
14	12	V_{CCRF}	—	Power supply voltage input pin for the RF-PLL section (except for the charge pump circuit) .
15	13	GND_{RF}	—	Ground pin for the RF-PLL section.
16	14	$Xfin_{RF}$	I	Prescaler complimentary input pin for the RF-PLL section. This pin should be grounded via a capacitor.
17	15	fin_{RF}	I	Prescaler input pin for the RF-PLL. Connection to an external VCO should be AC coupling.
18	16	LE	I	Load enable signal input pin (with the schmitt trigger circuit.) On a rising edge of load enable, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
19	17	Data	I	Serial data input pin (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
20	18	Clock	I	Clock input pin for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a rising edge of the clock.

■ BLOCK DIAGRAM



O : TSSOP 20
( ) : BCC 20

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			Min.	Max.	
Power supply voltage		V_{CC}	–0.5	+4.0	V
		Vp	V_{CC}	+4.0	V
Input voltage		V_I	–0.5	V_{CC} + 0.5	V
Output voltage	LD / fout	V_O	GND	V_{CC}	V
	Do	V_{DO}	GND	Vp	V
Storage temperature		Tstg	–55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	$V_{CCRF} = V_{CCIF}$
	Vp	V_{CC}	3.0	3.6	V	
Input voltage	V_I	GND	—	V_{CC}	V	
Operating temperature	Ta	–40	—	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 V to 3.6 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current		I_{CCIF} *1	fin_{IF} = 480 MHz, SW_C = 0 V_{CCIF} = Vp_{IF} = 3.0 V	1.0	1.6	2.3	mA
		I_{CCRF} *1	fin_{RF} = 2000 MHz V_{CCRF} = Vp_{RF} = 3.0 V	2.8	4.2	5.8	mA
Power saving current		I_{PSIF}	PS = "L"	—	0.1 *2	10	µA
		I_{PSRF}	PS = "L"	—	0.1 *2	10	µA
Operating frequency	fin_{IF} *3	fin_{IF}	IF PLL	100	—	600	MHz
	fin_{RF} *3	fin_{RF}	RF PLL	400	—	2000	MHz
	OSC_{IN}	f_{OSC}	—	3	—	40	MHz
Input sensitivity	fin_{IF}	$Pfin_{IF}$	IF PLL, 50 Ω system	–15	—	+2	dBm
	fin_{RF}	$Pfin_{RF}$	RF PLL, 50 Ω system	–15	—	+2	dBm
	OSC_{IN}	V_{OSC}	—	0.5	—	V_{CC}	Vp-p
"H" level input voltage	Data, Clock, LE	V_{IH}	Schmitt triger input	0.7 V_{CC} + 0.4	—	—	V
"L" level input voltage		V_{IL}	Schmitt triger input	—	—	0.3 V_{CC} – 0.4	
"H" level input voltage	PS_{IF} PS_{RF}	V_{IH}	—	0.7 V_{CC}	—	—	V
"L" level input voltage		V_{IL}	—	—	—	0.3 V_{CC}	
"H" level input current	Data, Clock, LE, PS_{IF}, PS_{RF}	I_{IH} *4	—	–1.0	—	+1.0	µA
"L" level input current		I_{IL} *4	—	–1.0	—	+1.0	
"H" level input current	OSC_{IN}	I_{IH}	—	0	—	+100	µA
"L" level input current		I_{IL} *4	—	–100	—	0	
"H" level output voltage	LD/ fout	V_{OH}	V_{CC} = Vp = 3.0 V, I_{OH} = –1 mA	V_{CC} – 0.4	—	—	V
"L" level output voltage		V_{OL}	V_{CC} = Vp = 3.0 V, I_{OL} = 1 mA	—	—	0.4	
"H" level output voltage	Do_{IF} Do_{RF}	V_{DOH}	V_{CC} = Vp = 3.0 V, I_{DOH} = –0.5 mA	Vp – 0.4	—	—	V
"L" level output voltage		V_{DOL}	V_{CC} = Vp = 3.0 V, I_{DOL} = 0.5 mA	—	—	0.4	
High impedance cutoff current	Do_{IF} Do_{RF}	I_{OFF}	V_{CC} = Vp = 3.0 V V_{OFF} = 0.5 V to Vp – 0.5 V	—	—	2.5	nA
"H" level output current	LD/ fout	I_{OH} *4	V_{CC} = Vp = 3.0 V	—	—	–1.0	mA
"L" level output current		I_{OL}	V_{CC} = Vp = 3.0 V	1.0	—	—	

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(V_{CC} = 2.7 V to 3.6 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition		Value			Unit
					Min.	Typ.	Max.	
"H" level output current	D_{OIF} D_{ORF}	I_{DOH} *4	V_{CC} = Vp = 3.0 V, V_{DOH} = Vp / 2, Ta = +25 °C	CS bit = "H"	–8.2	–6.0	–4.1	mA
				CS bit = "L"	–2.2	–1.5	–0.8	mA
"L" level output current		I_{DOL}	V_{CC} = Vp = 3.0 V, V_{DOL} = Vp / 2, Ta = +25 °C	CS bit = "H"	4.1	6.0	8.2	mA
				CS bit = "L"	0.8	1.5	2.2	mA
Charge pump current rate	I_{DOL}/I_{DOH}	I_{DOMT} *5	V_{DO} = Vp / 2		—	3	—	%
	vs V_{DO}	I_{DOVD} *6	0.5 V ≤ V_{DO} ≤ Vp – 0.5 V		—	10	—	%
	vs Ta	I_{DOTA} *7	–40 °C ≤ Ta ≤ +85 °C, V_{DO} = Vp / 2		—	5	—	%

*1 : Conditions ; fosc = 13 MHz, Ta = +25 °C in locking state.

*2 : $V_{CCIF} = Vp_{IF} = V_{CCRF} = Vp_{RF}$ = 3.0 V, fosc = 13 MHz, Ta = +25 °C, in power saving mode.

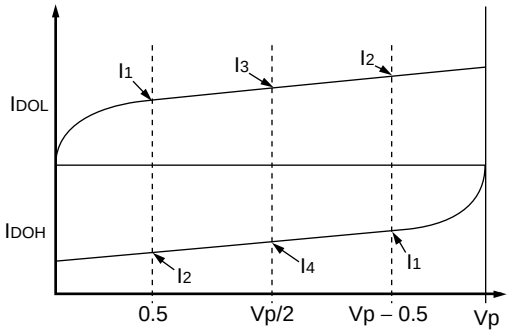
*3 : AC coupling. 1000 pF capacitor is connected.

*4 : The symbol "–" (minus) means direction of current flow.

*5 : V_{CC} = Vp = 3.0 V, Ta = +25 °C $(||I_3| - |I_4||) \ / \ [(|I_3| + |I_4|) \ / \ 2] \times 100$ (%)

*6 : V_{CC} = Vp = 3.0 V, Ta = +25 °C $[(||I_2| - |I_1||) / 2] / [(|I_1| + |I_2|) \ / \ 2] \times 100$ (%) (Applied to each I_{DOL} and I_{DOH})

*7 : V_{CC} = Vp = 3.0 V, Ta = +25 °C$[(||I_{DO\ (85\ °C)}| - |I_{DO\ (-40\ °C)}||) \ / \ 2] / [(|I_{DO\ (85\ °C)}| + |I_{DO\ (-40\ °C)}|) \ / \ 2] \times 100$ (%) (Applied to each I_{DOL} and I_{DOH})



■ FUNCTIONAL DESCRIPTION

1. Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections and programmable reference dividers of IF/RF-PLL sections are controlled individually.
Serial data of binary code is entered through Data pin.
On a rising edge of clock, one bit of serial data is transferred into the shift register. On a rising edge of load enable signal, the data stored in the shift register is transferred to one of latches depending upon the control bit data setting.

	The programmable reference counter for the IF-PLL	The programmable counter and the swallow counter for the IF-PLL	The programmable reference counter for the RF-PLL	The prgrammable counter and the swallow counter for the RF-PLL
CN1	0	1	0	1
CN2	0	0	1	1
CN3	0	0	0	0

Note **:** (CN3 = 1 is pohibited)

(1) Serial data format

LSB Direction of data shift → MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0	0	0	R_{C1}	R_{C2}	R_{C3}	R_{C4}	R_{C5}	R_{C6}	R_{C7}	R_{C8}	R_{C9}	R_{C10}	R_{C11}	R_{C12}	R_{C13}	R_{C14}	LDS	T1	T2	SW_C	FC_C	CS_C
1	0	0	A_{C1}	A_{C2}	A_{C3}	A_{C4}	0	0	0	N_{C1}	N_{C2}	N_{C3}	N_{C4}	N_{C5}	N_{C6}	N_{C7}	N_{C8}	N_{C9}	N_{C10}	N_{C11}	X	X
0	1	0	R_{F1}	R_{F2}	R_{F3}	R_{F4}	R_{F5}	R_{F6}	R_{F7}	0	0	0	0	0	0	0	0	SC1	SC2	1	FC_F	CS_F
1	1	0	A_{F1}	A_{F2}	A_{F3}	A_{F4}	0	N_{F1}	N_{F2}	N_{F3}	N_{F4}	N_{F5}	N_{F6}	N_{F7}	N_{F8}	N_{F9}	N_{F10}	F1	F2	F3	F4	0

Control bit (CN3)
Control bit (CN2)
Control bit (CN1)

R_{C1} to R_{C14} : Divide ratio setting bits for the reference counter of the IF (3 to 16383)
A_{C1} to A_{C4} : Divide ratio setting bits for the swallow counter of the IF (0 to 15, A < N)
N_{C1} to N_{C11} : Divide ratio setting bits for the programmable counter of the IF (3 to 2047)
LDS, T1, T2 : Select bits for the lock detect output or a monitoring phase comparison frequency
SW_C : Divide ratio setting for the prescaler of the IF
FC_C : Phase control bit for the phase detector of the IF
CS_C : Charge pump current select bit of the IF
R_{F1} to R_{F7} : Divide ratio setting bits for the reference counter of the RF (3 to 127)
A_{F1} to A_{F4} : Divide ratio setting bits for the swallow counter of the RF (0 to 15, A < N – 2)
N_{F1} to N_{F10} : Divide ratio setting bits for the programmable counter of the RF (18 to 1023)
F1 to F4 : Fractional-N increment setting bit for the fractional accumulator (0 to 15, F < Q)
SC1, SC2 : Spurious cancel set bit of the RF.
FC_F : Phase control bit for the phase detector of the RF.
CS_F : Charge pump current select bit of the RF
X : Dummy bit (Set “0” or “1”)

Note: Data input with MSB first.

(2) Data Setting

• RF synthesizer Data Setting (Fractional-N)

The divide ratio can be calculated using the following equation :

$f_{VCORF} = N_{TOTAL} \times fosc \div R$

$N_{TOTAL} = P \times N + A + F / Q \quad \leftarrow \quad (A < N - 2, F < Q)$

f_{VCORF} : Output frequency of external voltage controlled oscillator (VCO)
N_{TOTAL} : Total division ratio from prescaler input to the phase detector input
fosc : Output frequency of the reference frequency oscillator
R : Preset divide ratio of binary 7 bit reference counter (3 to 127)
P : Preset divide ratio of modulus prescaler (16 fixed)
N : Preset divide ratio of binary 10 bit programmable counter (18 to 1023)
A : Preset divide ratio of binary 4 bit swallow counter (0 to 15)
F : A numerator of fractional-N (0 to 15)
Q : A denominator of fractional-N, modulo 13

• Binary 7-bit Programmable Reference Counter Data Setting (R_{F1} to R_{F7})

Divide ratio (R)	R_{F7}	R_{F6}	R_{F5}	R_{F4}	R_{F3}	R_{F2}	R_{F1}
3	0	0	0	0	0	1	1
4	0	0	0	0	1	0	0
—	—	—	—	—	—	—	—
52	0	1	1	0	1	0	0
—	—	—	—	—	—	—	—
127	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited.

• Fractional-N incremant of the fractional accumulator Data Setting (F1 to F4)

Setting value(F)	F4	F3	F2	F1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
—	—	—	—	—
15	1	1	1	1

Note : F < Q

• **Binary 10-bit Programable Counter Data Setting (N_{F1} to N_{F10})**

Divide ratio (N)	N_{F10}	N_{F9}	N_{F8}	N_{F7}	N_{F6}	N_{F5}	N_{F4}	N_{F3}	N_{F2}	N_{F1}
18	0	0	0	0	0	1	0	0	1	0
19	0	0	0	0	0	1	0	0	1	1
—	—	—	—	—	—	—	—	—	—	—
32	0	0	0	0	1	0	0	0	0	0
—	—	—	—	—	—	—	—	—	—	—
1023	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 18 is prohibited.

• **Binary 4-bit Swallow Counter Data Setting (A_{F1} to A_{F4})**

Divide ratio (A)	A_{F4}	A_{F3}	A_{F2}	A_{F1}
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
—	—	—	—	—
15	1	1	1	1

Note : A < N – 2

• **Spurious cancel Bit Setting**

Spurious cancel amount	SC1	SC2
Large	0	0
Midium	0	1
Small	1	0

Note : The bits set how much the amount of spurious cancel.
If the Large is selected, a spurious is tended to become small.

• **Phase Comparator Phase Switching Data Setting**

	FC_F = High	FC_F = Low
	D_O	D_O
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO polarity	1	2

Notes : • Z = High-Z
• Depending upon the VCO and LPF polarity, FC bit should be set.

• **Charge pump current select Bit Setting**

CS_F	Current value
1	± 6.0 mA
0	± 1.5 mA

• **IF synthesizer Data Setting (Integer)**

The divide ratio can be calculated using the following equation :

$f_{VCOIF} = [(P \times N) + A] \times fosc \div R \quad (A < N)$

f_{VCOIF}	: Output frequency of external voltage controlled oscillator (VCO)
P	: Preset divide ratio of modulus prescaler (8 or 16)
N	: Preset divide ratio of binary 11 bit programmable counter (3 to 2047)
A	: Preset divide ratio of binary 4 bit swallow counter (0 to 15)
fosc	: Output frequency of the reference frequency oscillator
R	: Preset divide ratio of binary 14 bit reference counter (3 to 16383)

• **Binary 14-bit Programmable Reference Counter Data Setting (R_{C1} to R_{C14})**

Divide ratio (R)	R_{C14}	R_{C13}	R_{C12}	R_{C11}	R_{C10}	R_{C9}	R_{C8}	R_{C7}	R_{C6}	R_{C5}	R_{C4}	R_{C3}	R_{C2}	R_{C1}
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited.

• **Binary 11-bit Programmable Counter Data Setting (N_{C1} to N_{C11})**

Divide ratio (N)	N_{C11}	N_{C10}	N_{C9}	N_{C8}	N_{C7}	N_{C6}	N_{C5}	N_{C4}	N_{C3}	N_{C2}	N_{C1}
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
—	—	—	—	—	—	—	—	—	—	—	—
2047	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited.

• **Binary 4-bit Swallow Counter Data Setting (A_{C1} to A_{C4})**

Divide ratio (A)	A_{C4}	A_{C3}	A_{C2}	A_{C1}
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
—	—	—	—	—
15	1	1	1	1

Note : A < N

• **Prescaler Data Setting (SW_C)**

SW_C	Prescaler divide ratio
1	8/9
0	16/17

• **Phase Comparator Phase Switching Data Setting**

	FC$_C$ = High	**FC$_C$ = Low**
	D$_O$	**D$_O$**
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H

Notes : • Z = High-Z
• Depending upon the VCO and LPF polarity, FC bit should be set.

•**Charge pump current select Data Setting (CS$_C$)**

CS$_C$	**Do current**
1	± 6.0 mA
0	± 1.5 mA

• **Common setting**

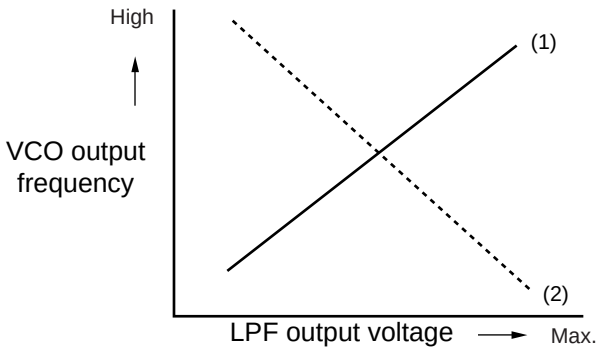
• **LD/fout Output Select Data Setting**

LD/fout		**LDS**	**T1**	**T2**
LD output		0	—	—
fout output	fr_{IF}	1	0	0
	fr_{RF}	1	1	0
	fp_{IF}	1	0	1
	fp_{RF}	1	1	1

• **FC bit Setting**

When designing a synthesizer, the FC bit setting depends on the VCO and LPF characteristics.

When the LPF and VCO characteristics are similar to (1) ,
set FC bit “H”.
When the VCO characteristics are similar to (2) ,
set FC bit “L”.



2. Power Saving Mode (Intermittent Mode Control)

• PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters the power saving mode, reducing the current consumption. See "■ ELECTRICAL CHARACTERISTICS" for the specific value.

The phase detector output, Do, becomes high impedance.

For the single PLL, the lock detector, LD, remains high, indicating a locked condition.

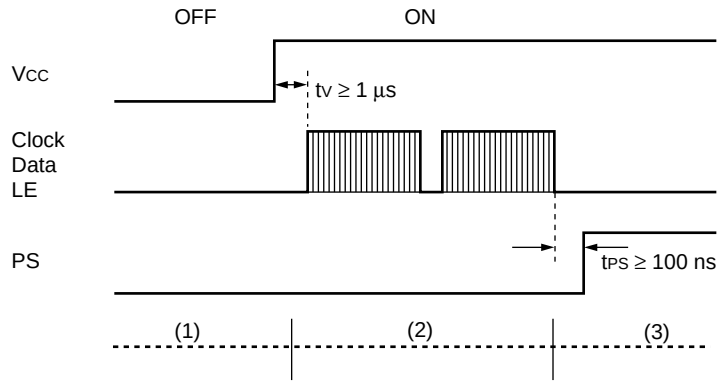
For the dual PLL, the lock detector, LD, is shown in "■PHASE DETECTOR OUTPUT WAVEFORM the LD Output Logic table.

Setting the PS pin high releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth start-up when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (fp) and the reference frequency (fr) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

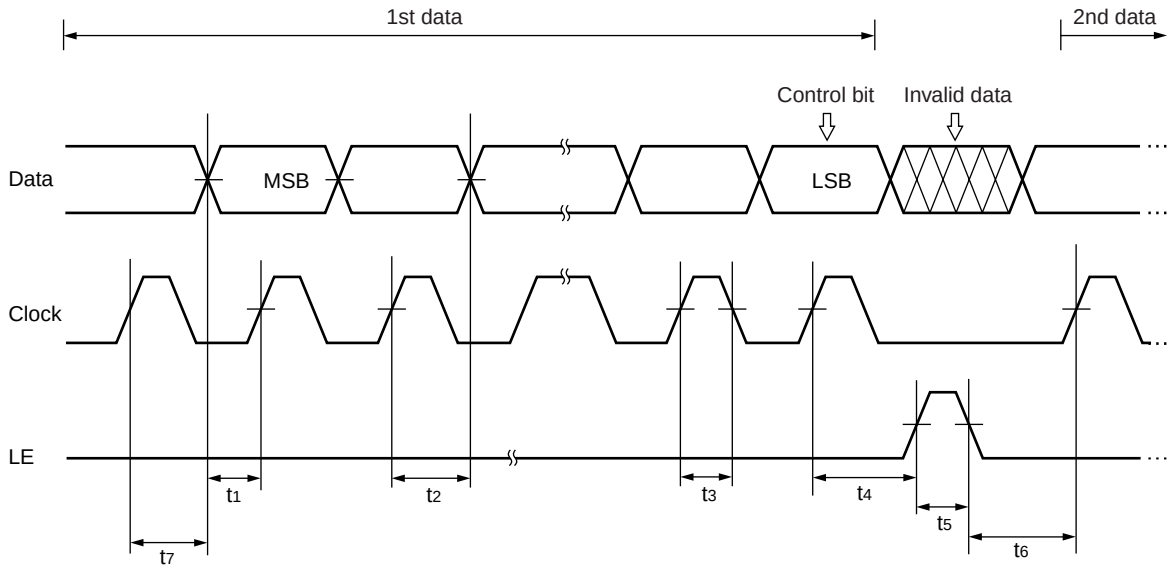
To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

Notes: •When power (V_{CC}) is first applied, the device must be in standby mode and PS = Low, for at least 1 µs.
•PS pin must be set "L" for Power ON.



(1) PS = L (power saving mode) at Power ON
(2) Set serial data 1 µs after power supply remains stable ($V_{CC} \geq 2.2$ V) .
(3) Release power saving mode (PS : L → H) 100 ns after setting serial data.

3. Serial Data Input Timing



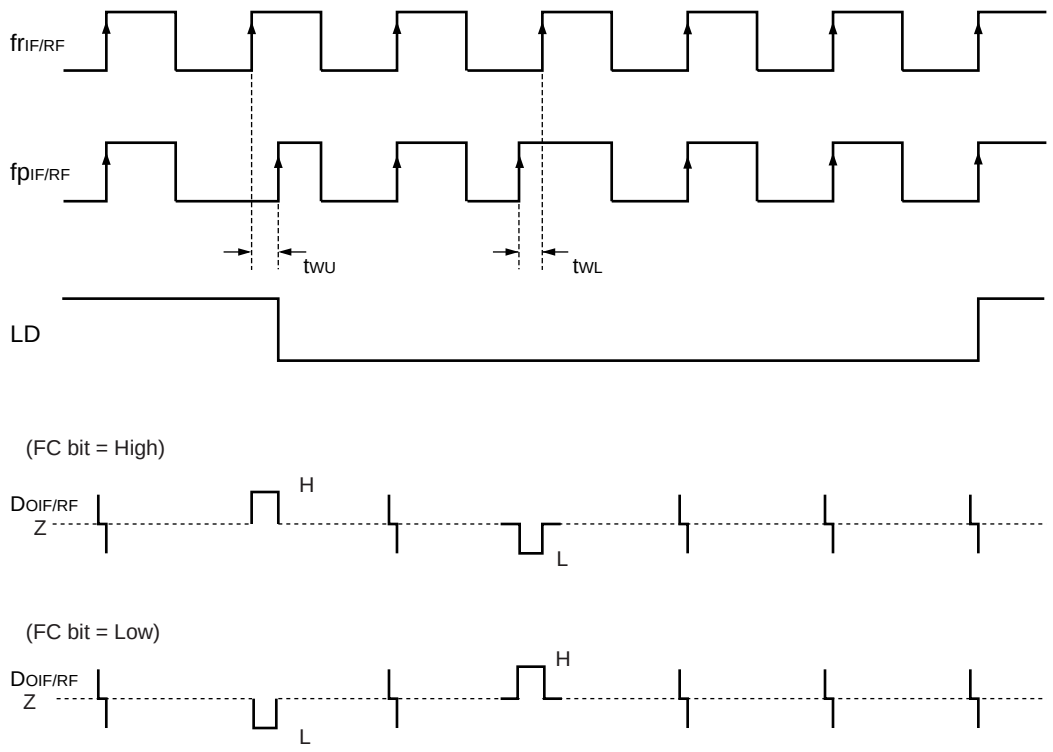
On the rising edge of the clock, one bit of data is transferred into shift register.

Parameter	Min.	Typ.	Max.	Unit
t_1	20	—	—	ns
t_2	20	—	—	ns
t_3	30	—	—	ns
t_4	30	—	—	ns

Parameter	Min.	Typ.	Max.	Unit
t_5	100	—	—	ns
t_6	20	—	—	ns
t_7	100	—	—	ns

Note : LE should be “L” when the data is transferred into the shift register.

■ PHASE DETECTOR OUTPUT WAVEFORM



LD Output Logic Table

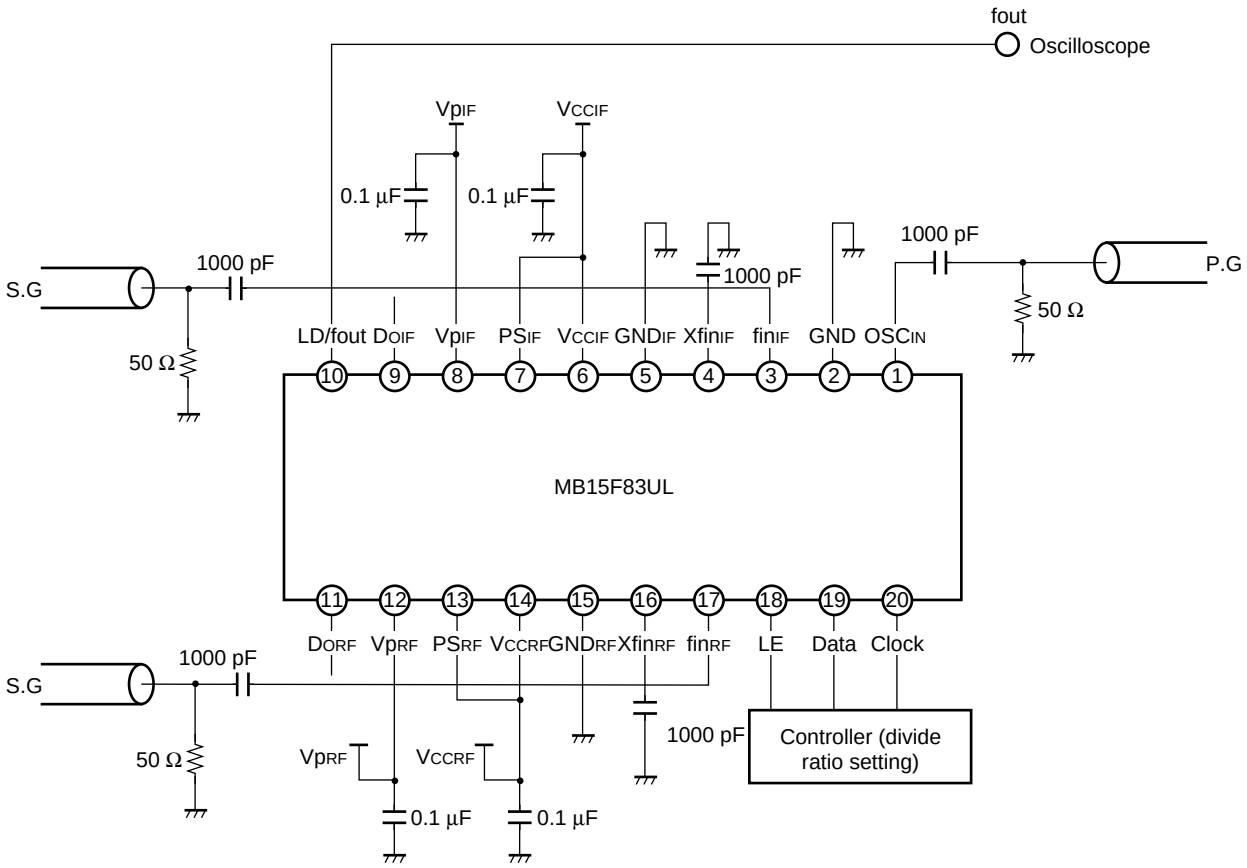
IF-PLL section	RF-PLL section	LD output
Locking state/Power saving state	Locking state/Power saving state	H
Locking state/Power saving state	Unlocking state	L
Unlocking state	Locking state/Power saving state	L
Unlocking state	Unlocking state	L

Notes:
- Phase error detection range = −2 π to +2 π
- Pulses on $Do_{IF/RF}$ signals are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSC_{IN} input frequency as follows.

  $t_{WU} \geq 2/fosc$ [s] : i.e. $t_{WU} \geq 153.8$ ns when fosc = 13.0 MHz

  $t_{WU} \leq 4/fosc$ [s] : i.e. $t_{WL} \leq 307.7$ ns when fosc = 13.0 MHz

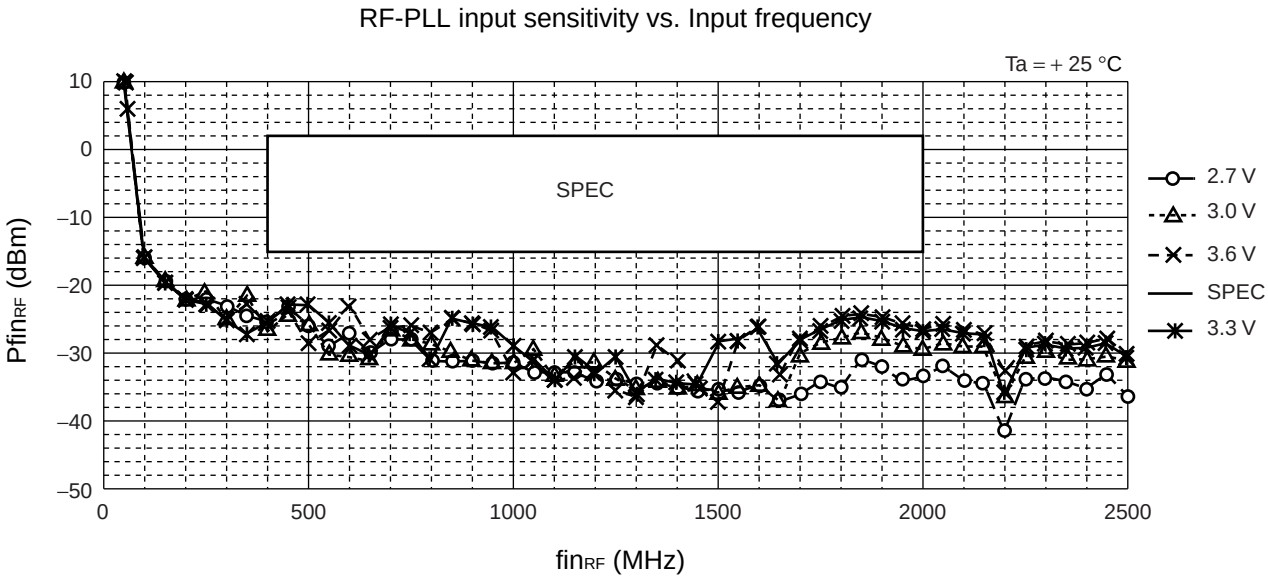
■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSC_{IN})

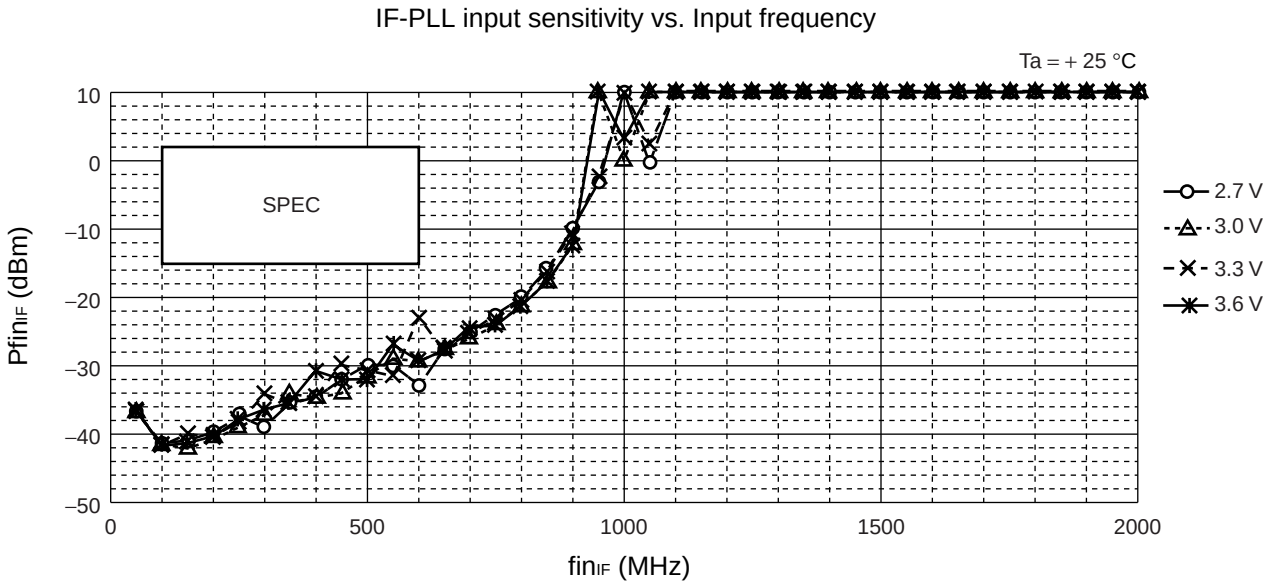


Note : TSSOP-20

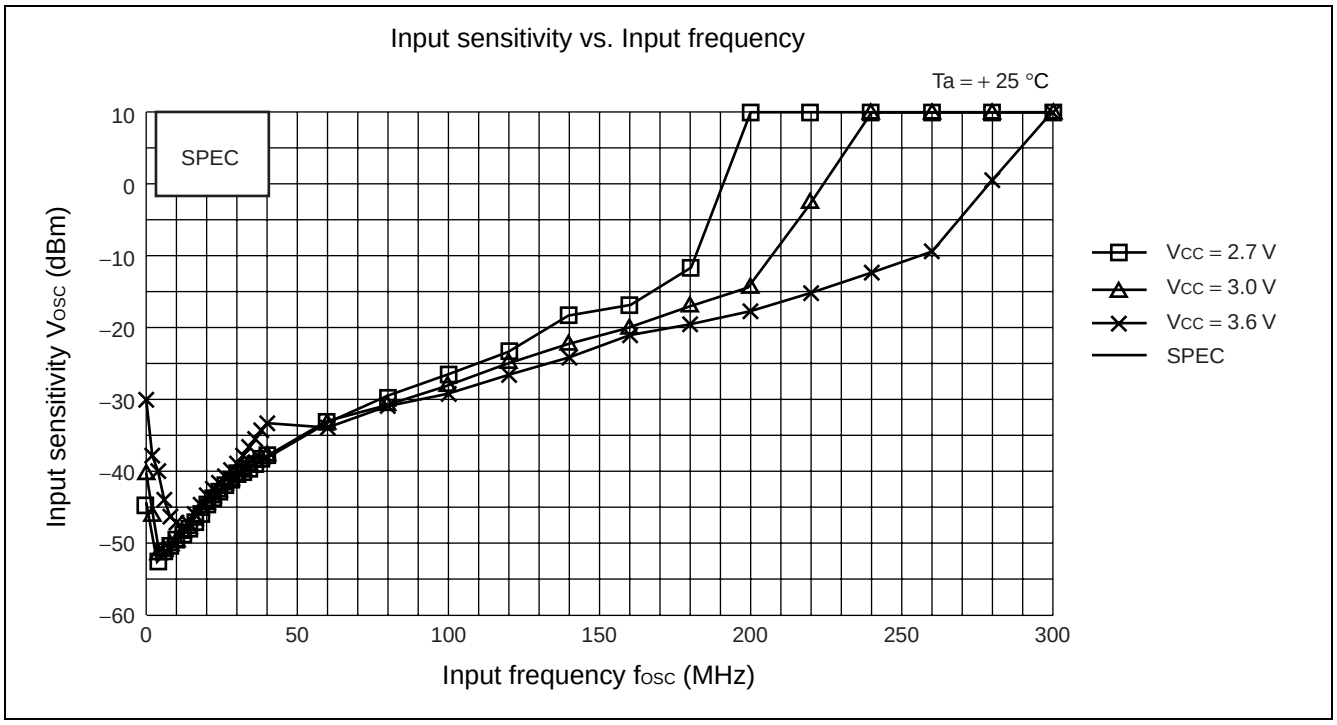
■ TYPICAL CHARACTERISTICS

1. fin input sensitivity





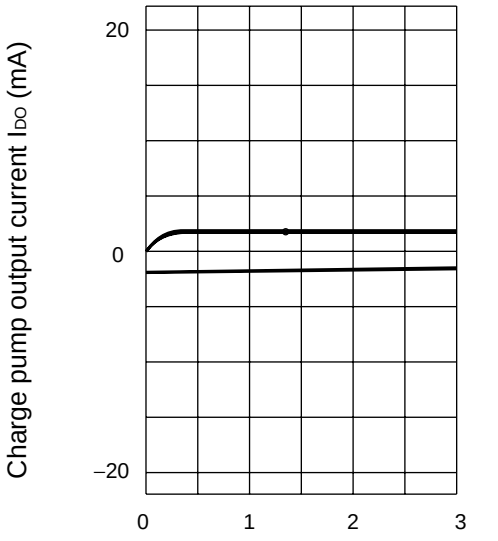
2. OSC_{IN} input sensitivity



3. RF-PLL Do output current

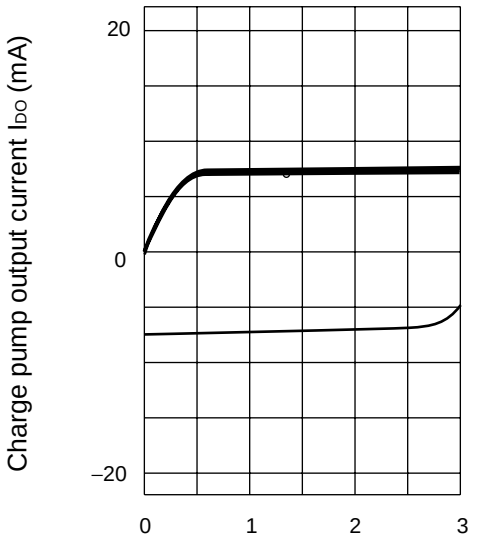
- 1.5 mA mode

$I_{DO} – V_{DO}$



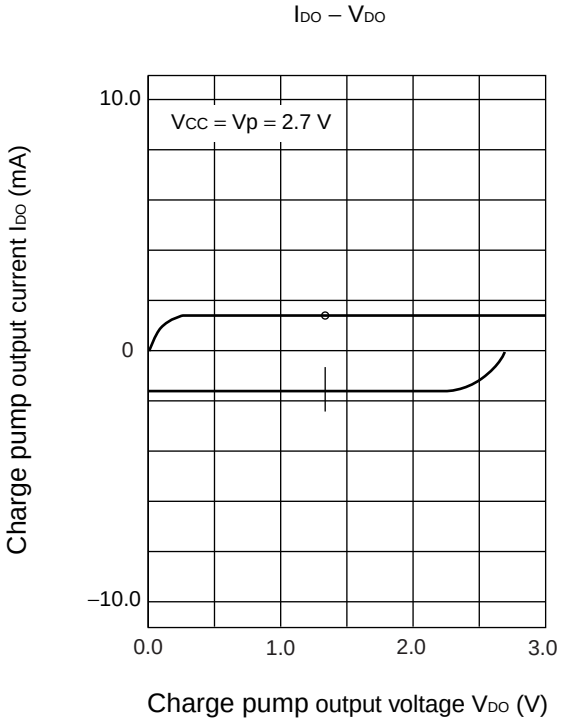
- 6.0 mA mode

$I_{DO} – V_{DO}$

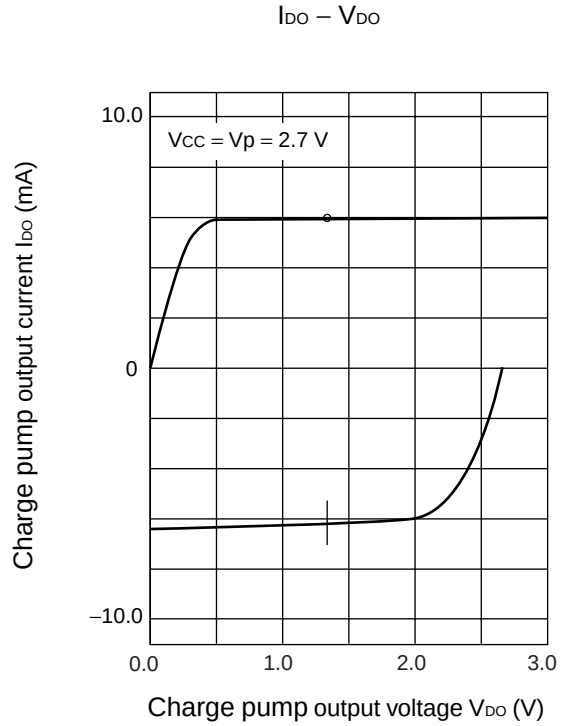


4. IF-PLL Do output current

- 1.5 mA mode

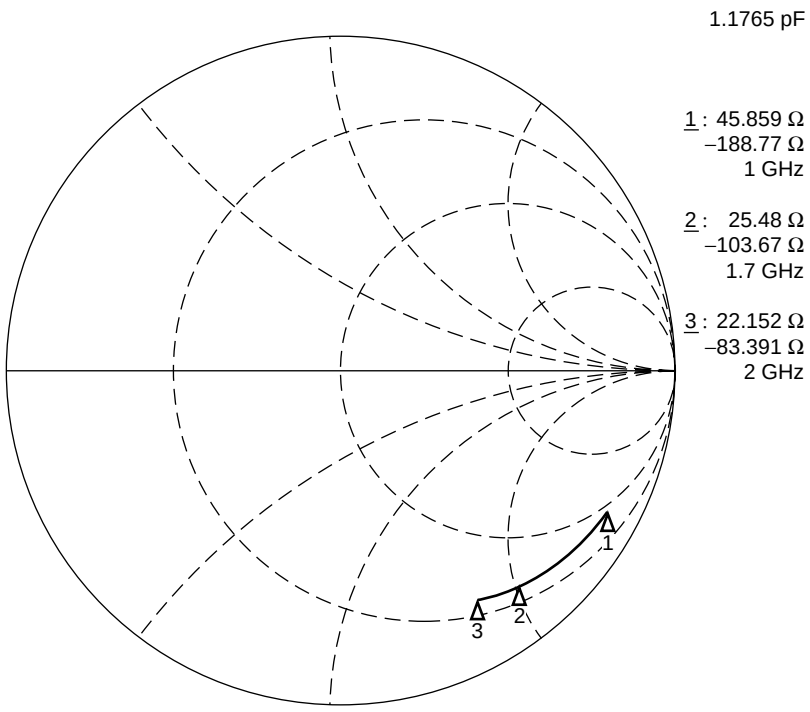


- 6.0 mA mode

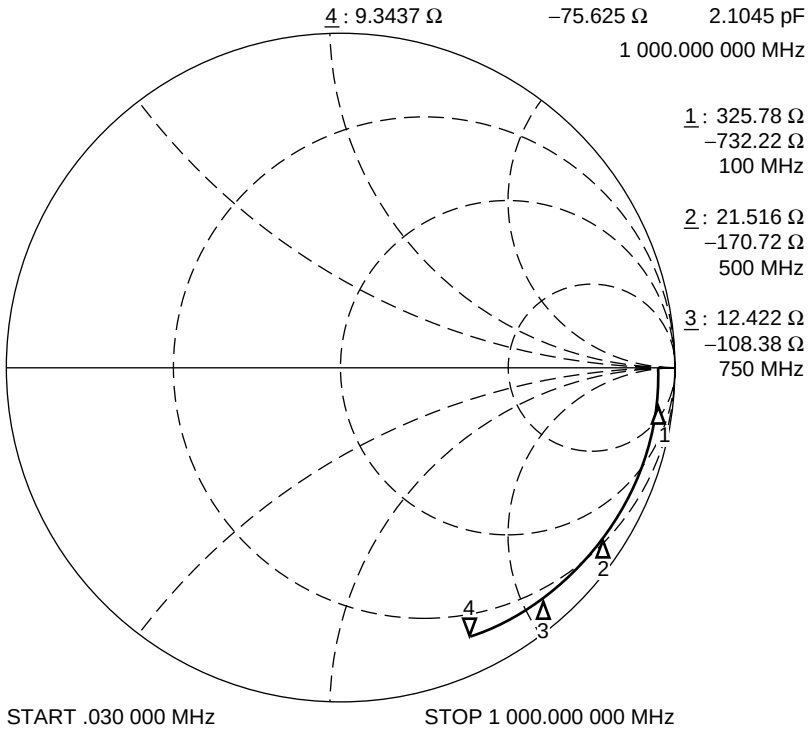


5. fin input impedance

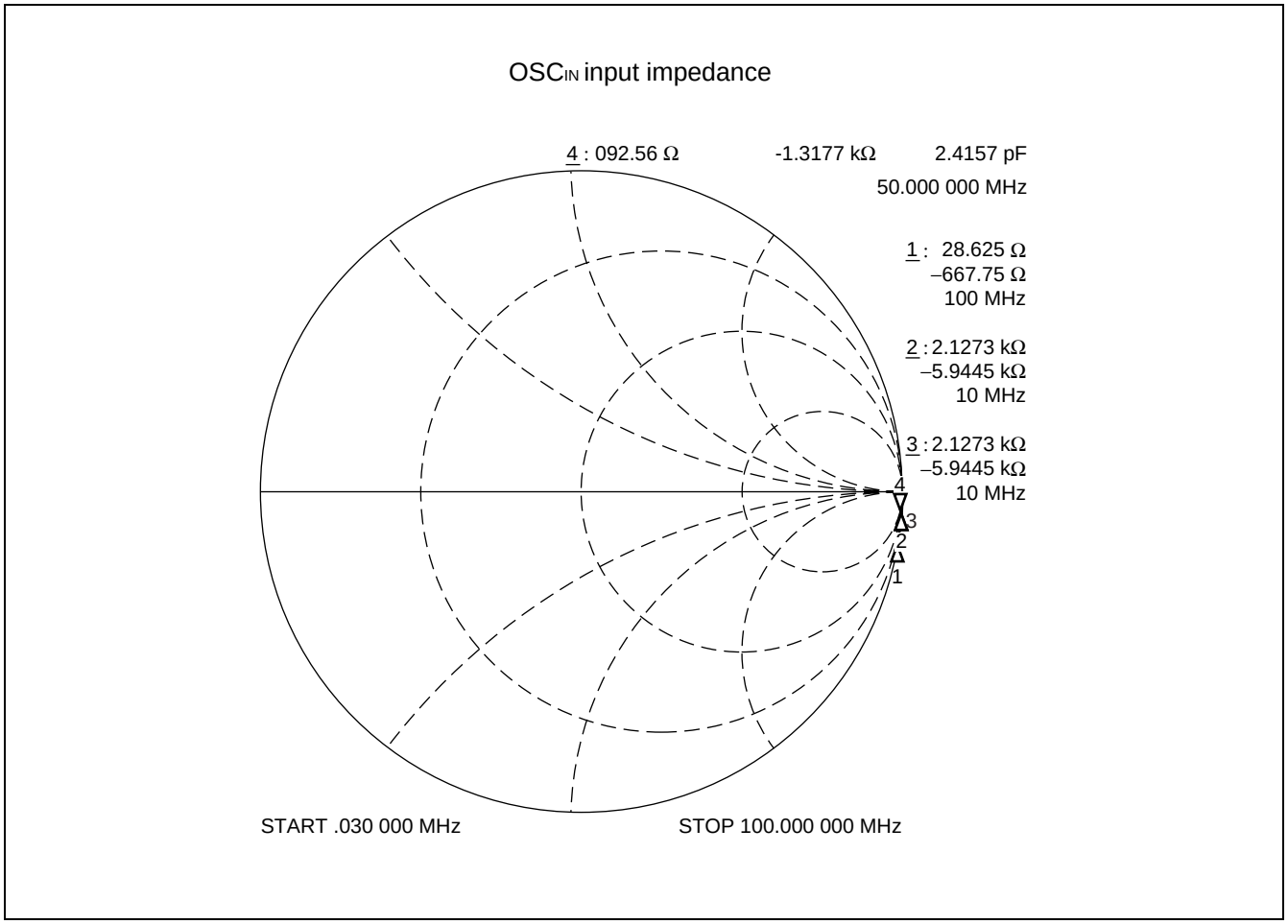
finR input impedance



finIF input impedance



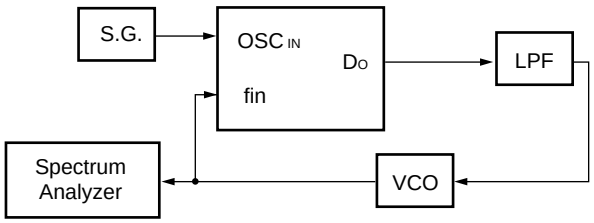
6. OSC_{IN} input impedance



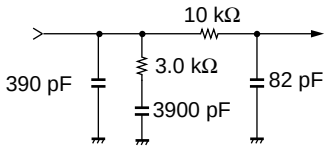
■ REFERENCE INFORMATION

(for Lock-up Time, Phase Noise and Reference Leakage)

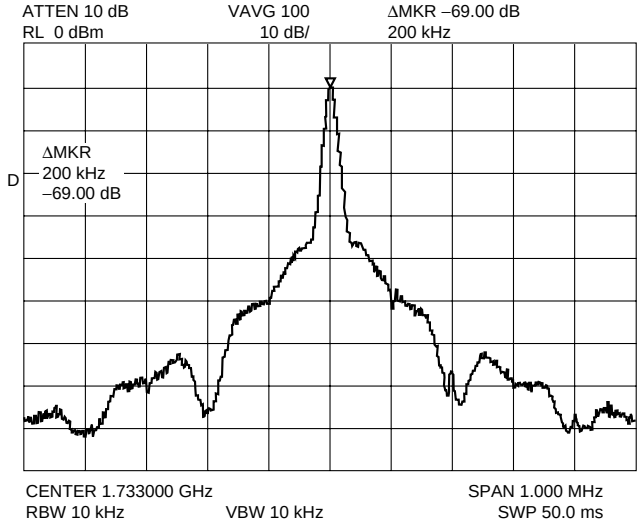
Test Circuit



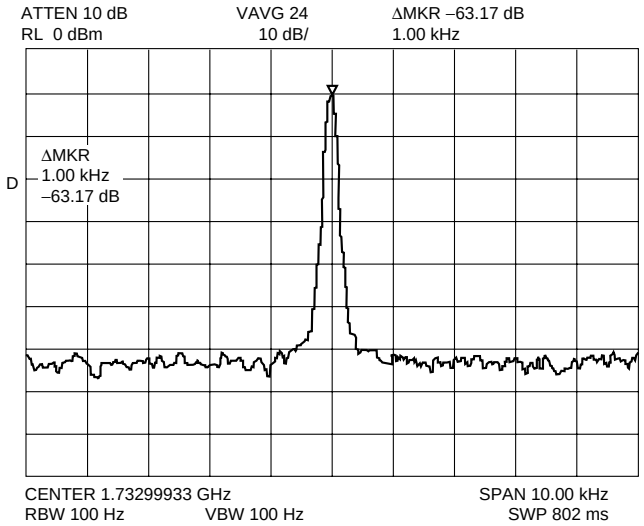
f_{VCO} = 1733 MHz	V_{CC} = 3.0 V
K_V = 44 MHz/V	V_{VCO} = 3.5 V
fr = 200 kHz	Ta = +25 °C
f_{OSC} = 13 MHz	CP : 6 mA mode
LPF	QM = 13



- PLL Reference Leakage

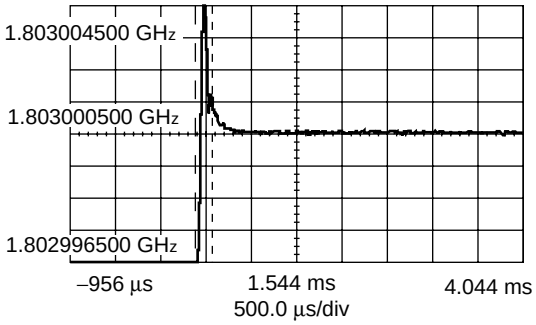


- PLL Phase Noise



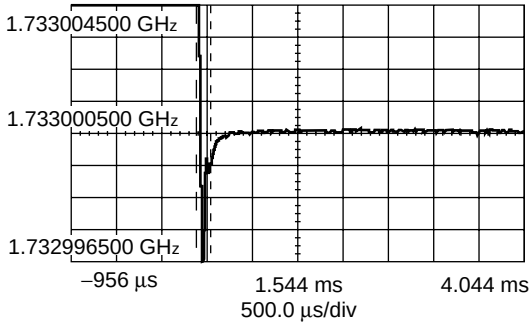
• PLL Lock Up time

1733 MHz→1803 MHz within ± 1 kHz
Lch→Hch 189 µs

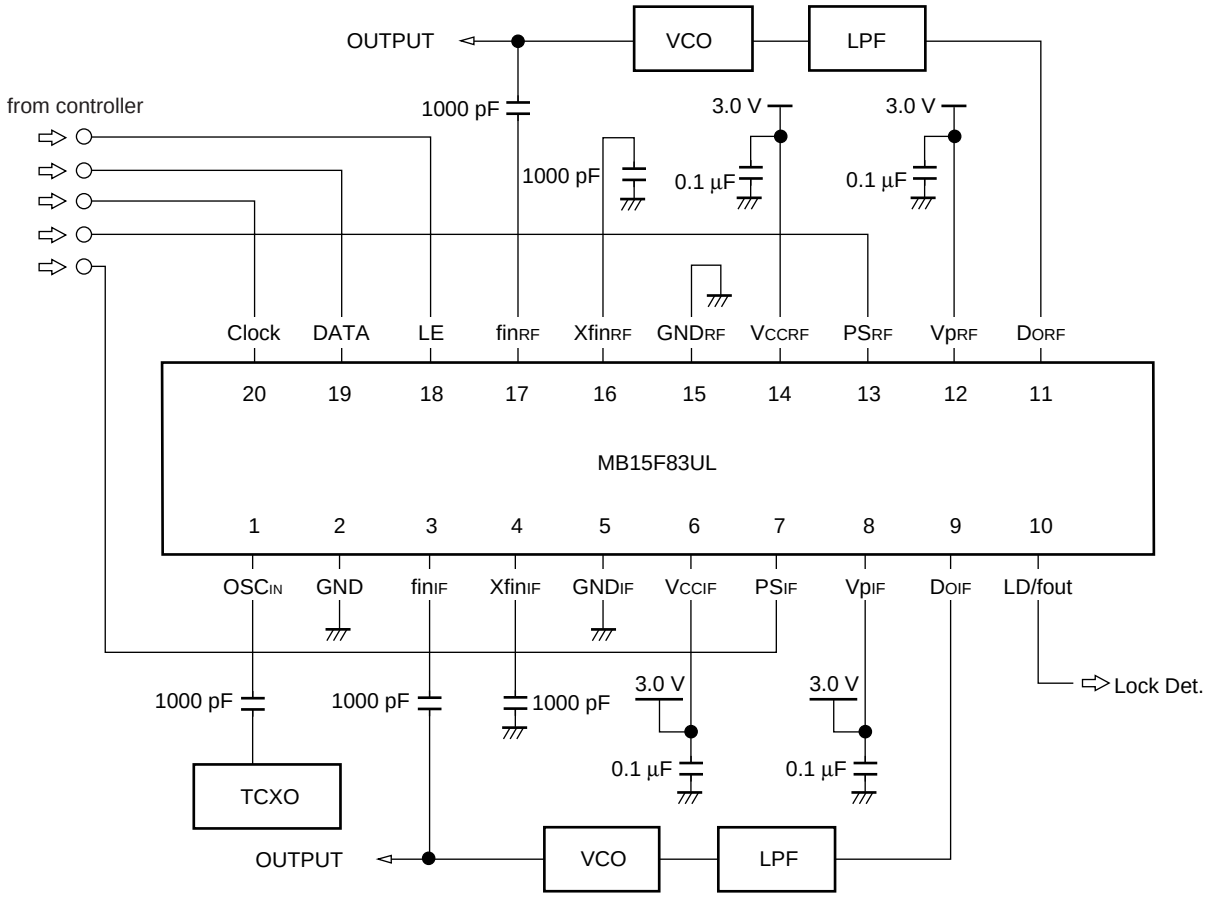


• PLL Lock Up time

1803 MHz→1733 MHz within ± 1 kHz
Hch→Lch 167 µs



■ APPLICATION EXAMPLE



Notes:
- Schmit trigger circuit is provided (insert a pull-up or pull-down resistor to prevent oscillation when open-circuited in the input) .
- TSSOP-20

■ USAGE PRECAUTIONS

(1) V_{CCRF}, Vp_{RF}, V_{CCIF} and Vp_{IF} must be equal voltage.

Even if either RF-PLL or IF-PLL is not used, power must be supplied to V_{CCRF}, Vp_{RF}, V_{CCIF} and Vp_{IF} to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.

(2) To protect against damage by electrostatic discharge, note the following handling precautions :

-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting or removing this device into or from a socket.
-Protect leads with conductive sheet, when transporting a board mounted device.

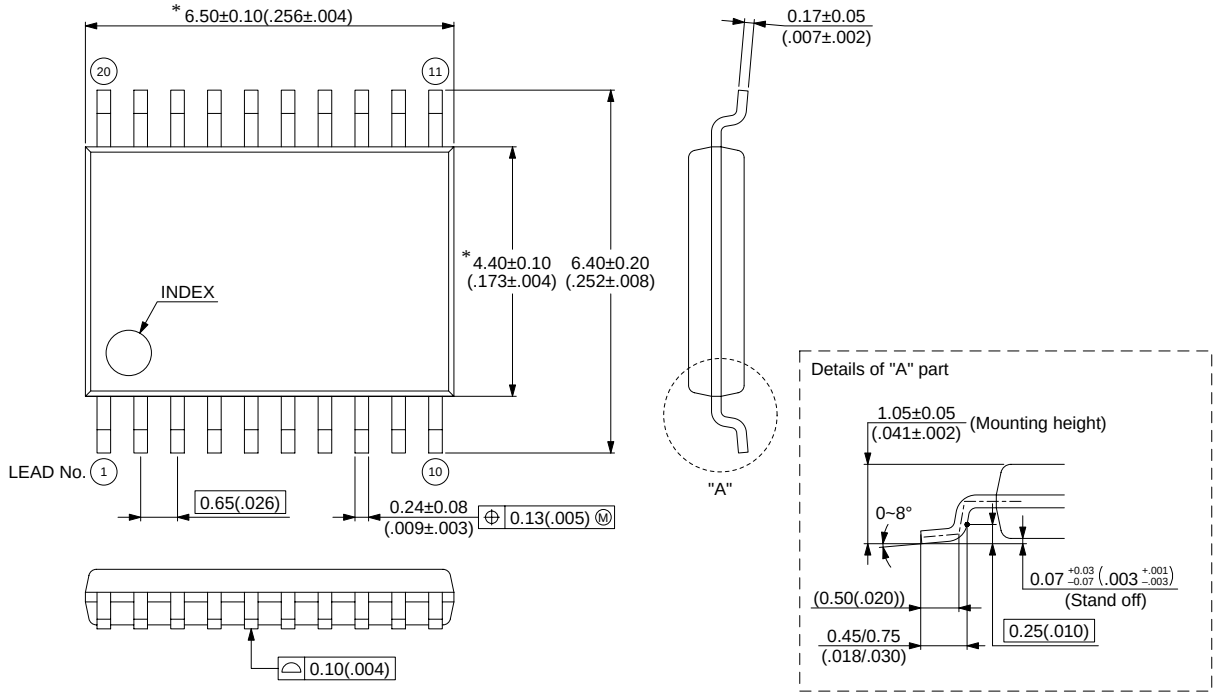
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F83ULPFT	20-pin plastic TSSOP (FPT-20P-M06)	
MB15F83ULPVA	20-pad plastic BCC (LCC-20P-M05)	

■ PACKAGE DIMENSIONS

20-pin Plastic TSSOP
(FPT-20P-M06)

* : These dimensions do not include resin protrusion.

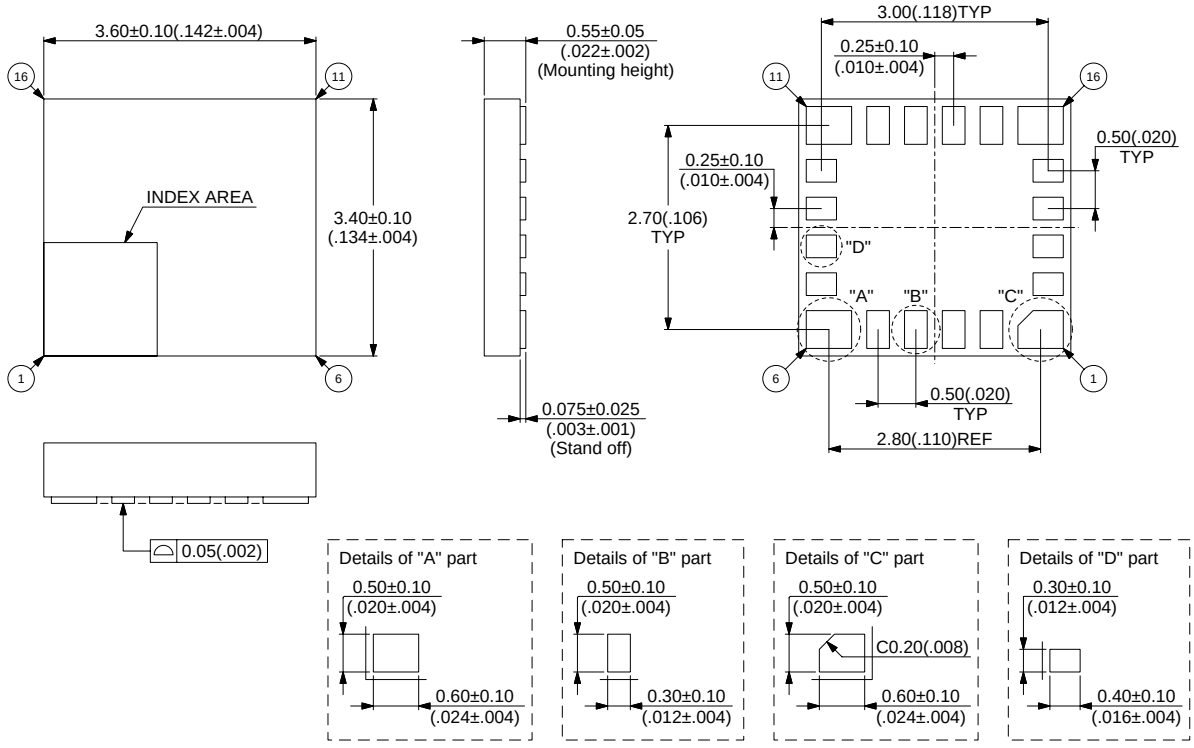


Dimensions in mm (inches)

(Continued)

(Continued)

20-pad plastic BCC
(LCC-20P-M05)



Dimensions in mm (inches)

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