I²C Controllable Buck Regulator in 3mm × 3mm DFN

FEATURES

- **I²C Programmable Output with 21.6mV Resolution**
- **Overtemperature Protected**
- **High Efficiency: Up to 93%**
- **Very Low Quiescent Current: Only 33µA**
- **600mA Output Current at V_{IN} = 3V**
- 2.5V to 5.5V Input Voltage Range
- 1MHz Constant Frequency Operation
- No Schottky Diode Required
- Low Dropout Operation: 100% Duty Cycle
- Stable with Ceramic Capacitors
- Shutdown Mode Draws <1µA Supply Current
- ±2% Output Voltage Accuracy
- Standard (100kHz) or Fast Mode (400kHz) I²C
- 6-Bit Voltage DAC (0.69V to 2.05V)
- Disable Burst Mode Operation
- Enable Power Good Blanking
- Optional External Start-Up Resistors
- Soft-Start
- 10 Lead, 3mm × 3mm DFN Package

APPLICATIONS

- Distributed Power Supplies
- Notebook Computers
- PDAs and Other Handheld Devices

DESCRIPTION

The LTC®3447 is a high efficiency monolithic synchronous current mode buck regulator. Using an I²C interface, the output voltage can be set between 0.69V and 2.05V using an internal 6-bit DAC.

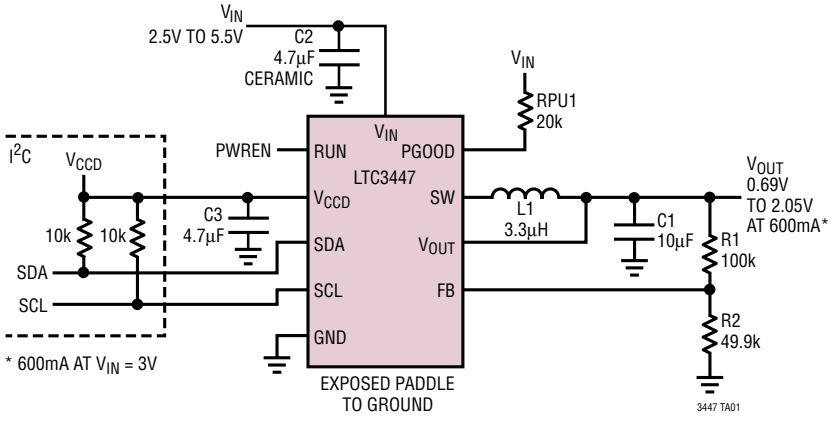
The buck regulator has optional external feedback resistors that can be used for setting the initial start up voltage. The feedback voltage reference for this start-up option is 0.6V. Once the voltage DAC is updated via the I²C, the buck regulator switches from external to internal feedback resistors. When there are no external resistors, the default start-up voltage is 1.38V.

The switching frequency is internally set at 1MHz, allowing the use of small surface mount inductors and capacitors.

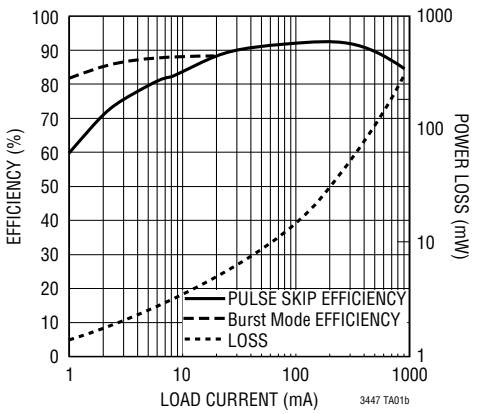
In Burst Mode® operation, supply current is only 33µA, dropping to <1µA in shutdown. The 2.5V to 5.5V input voltage range makes the LTC3447 ideally suited for single cell Li-Ion battery-powered applications. 100% duty cycle capability provides low dropout operation, extending battery life in portable systems. Automatic Burst Mode operation increases efficiency at light loads, further extending battery life.

The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode.

TYPICAL APPLICATION



Efficiency and Power Loss vs Load Current (V_{IN} = 3.6V)

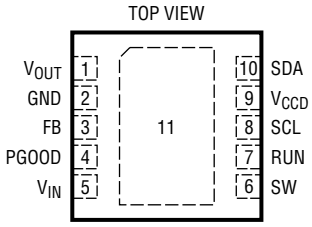


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_{CCD} Voltages ..... –0.3V to 6V
RUN, V_{OUT}, FB Voltages ..... –0.3V to V_{IN}
SW Voltage ..... –0.3V to (V_{IN} + 0.3V)
SCL, SDA Voltages..... – 0.3V to V_{CCD}
P-Channel Switch Source Current (DC) 800mA
N-Channel Switch Sink Current (DC) 800mA
Peak SW Sink and Source Current.....1.3A
Operating Temperature Range (Note 2) ...–40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range.....–65°C to 125°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
10-LEAD (3mm x 3mm)PLASTIC DFN
EXPOSED PAD IS GND (PIN 11)
MUST BE SOLDERED TO PCB

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 2.96°C/W

ORDER PART NUMBER
LTC3447EDD
DD PART MARKING
LBKB

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RUN	Run Threshold			0.3	1	1.5	V
PGOOD	Reports Undervoltage	PGOOD = 0.4V		3			mA
R_{VOUT}	Feedback Resistance				460		kΩ
$V_{OUT(MIN)}$	Regulated Output Voltage		●	0.669	0.69	0.711	V
$V_{OUT(MAX)}$	Regulated Output Voltage		●	1.989	2.05	2.112	V
V_{OUT}	Output Voltage Step Size (6-bits)		●	20.3	21.6	22.9	mV
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 2.5V to 5.5V (Note 6)	●		0.2 0.2	1.2 1	%/V %/V
I_{PK}	Peak Inductor Current	Duty Cycle < 35%, Wafer Level		0.75	1	1.25	A
$V_{LOADREG}$	Output Voltage Load Regulation				0.5		%
V_{IN}	Input Voltage Range		●	2.5		5.5	V
I_S	Input DC Bias Current Burst Mode Operation Active Mode Shutdown	(Note 4) I_{LOAD} = 0A V_{OUT} = 90%, I_{LOAD} = 0A V_{RUN} = 0V, V_{IN} = 5.5V			 34 280 0.1	 60 400 1	 µA µA µA
f_{OSC}	Nominal Oscillator Frequency	V_{OUT} = 100% V_{OUT} = 0V	●	0.7	1 160	1.3	MHz kHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 100mA, Wafer Level			0.32		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = –100mA, Wafer Level			0.22		Ω
I_{LSW}	SW Leakage	V_{RUN} = 0V, V_{SW} = 0V or 5V, V_{IN} = 5V			±0.1	±1	µA
FB	Optional Start-Up Feedback Voltage	Regulated Feedback Voltage			0.6		V
I_{FB}	Feedback Input Current				2.5	10	nA
SCL_{THR}	I^2C Clock Logic Threshold	(Note 5)			$V_{CCD/2}$		V
SCL_{HYST}	I^2C Clock Logic Hysteresis	(Note 5)			300		mV
SDA_{THR}	I^2C Data Logic Threshold	(Note 5)			$V_{CCD/2}$		V
SDA_{HYST}	I^2C Data Logic Hysteresis	(Note 5)			300		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
I²C Interface Timing						
$f_{I2C, MAX}$	Maximum I²C Operating Frequency	(Note 5)			400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	(Note 5)	1.3			µs
$t_{HD,RSTA}$	Hold Time After (Repeated) Start Condition	(Note 5)	0.6			µs
$t_{SU,RSTA}$	Repeated Start Condition Setup Time	(Note 5)	0.6			µs
$t_{SU,STOP}$	Stop Condition Setup Time	(Note 5)	20			µs
$t_{HD,DIN}$	Data Hold Time, Input	(Note 5)	0			ns
$t_{HD,DOUT}$	Data Hold Time, Output	(Note 5)	280	410	670	ns
$t_{SU,DAT}$	Data Setup Time	(Note 5)	50			ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter	(Note 5)			150	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3447E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature, T_A, and the power dissipation, P_D, according to the following formula:

$$T_J = T_A + P_D \bullet 43°C/W$$

This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

Note 5: Determined by design, not production tested.

Note 6: The LTC3447 is tested in a proprietary test mode that connects V_{OUT} to FB.

TIMING DIAGRAM

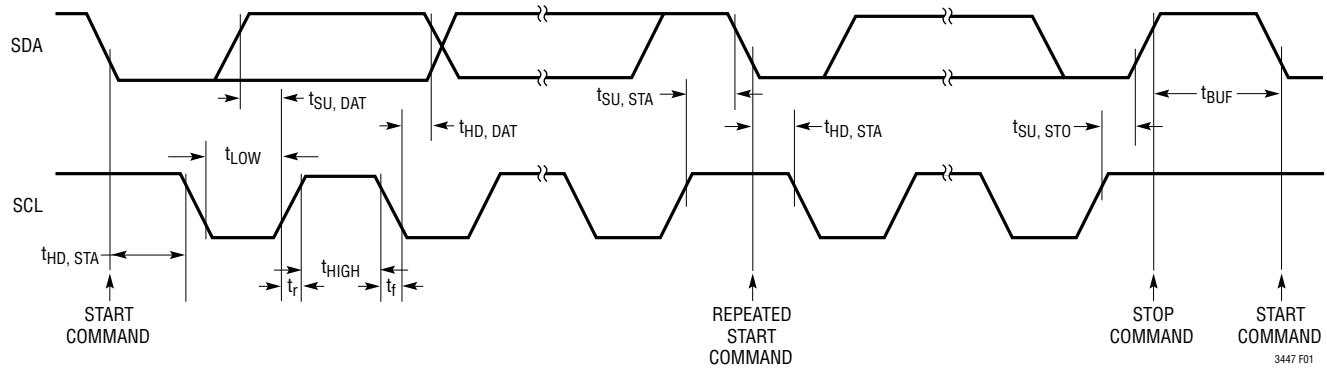
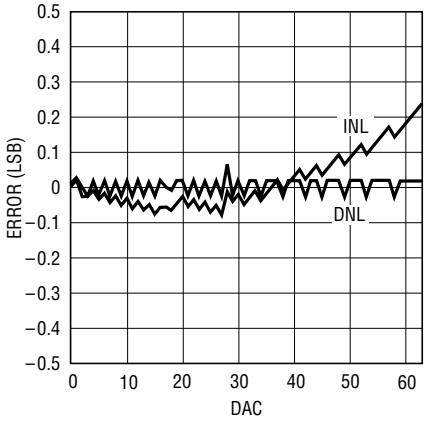


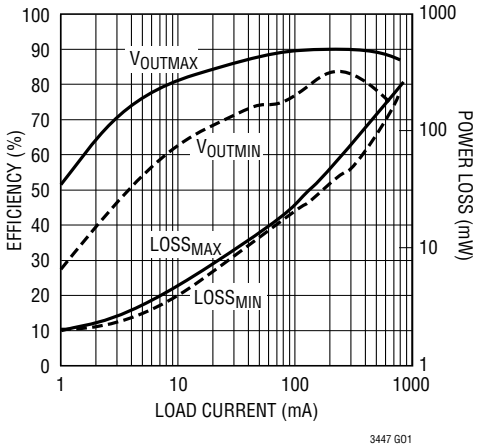
Figure 1. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

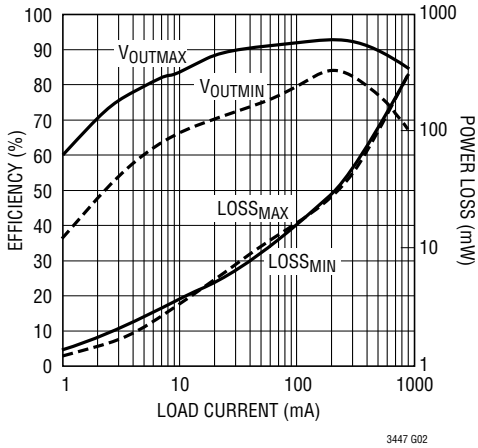
DAC Nonlinearity



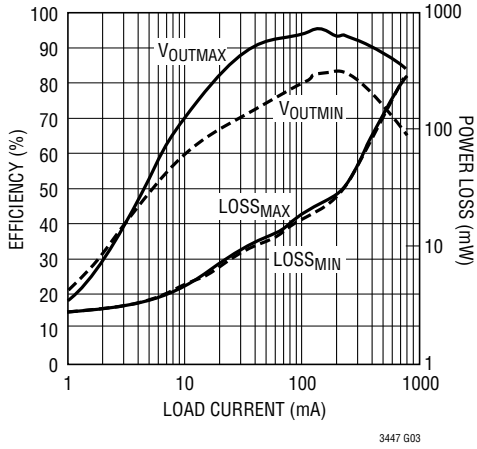
Efficiency and Power Loss vs Load Current (V_{IN} = 5.5V)



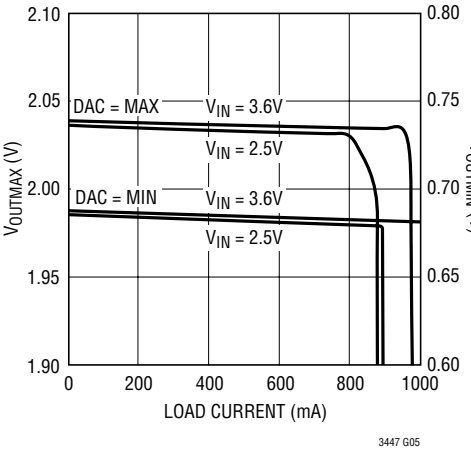
Efficiency and Power Loss vs Load Current (V_{IN} = 3.6V)



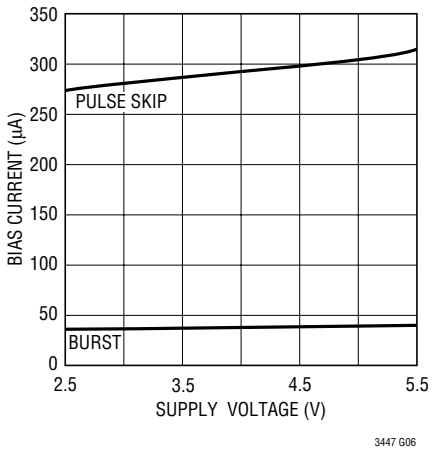
Efficiency and Power Loss vs Load Current (V_{IN} = 2.5V)



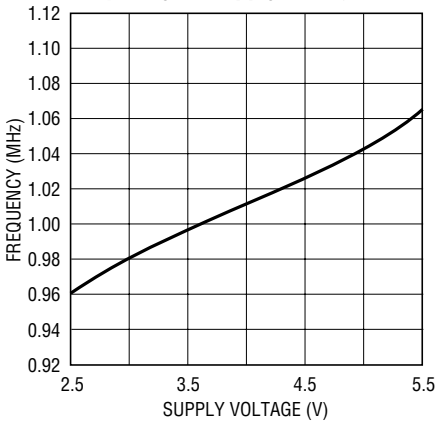
Output Voltage vs Load Current



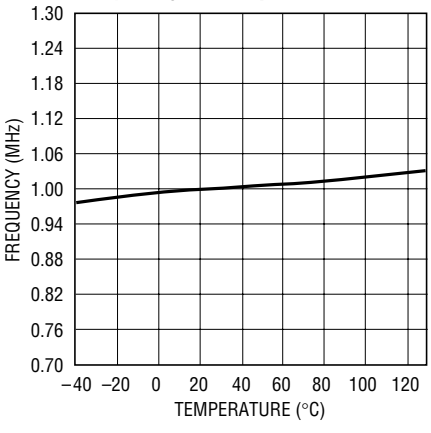
Bias Current vs Supply Voltage



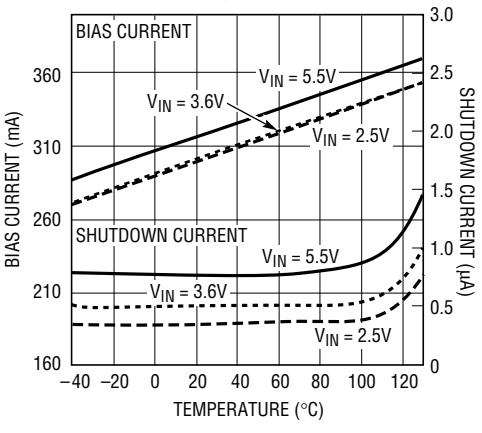
Frequency vs Supply Voltage



Frequency vs Temperature

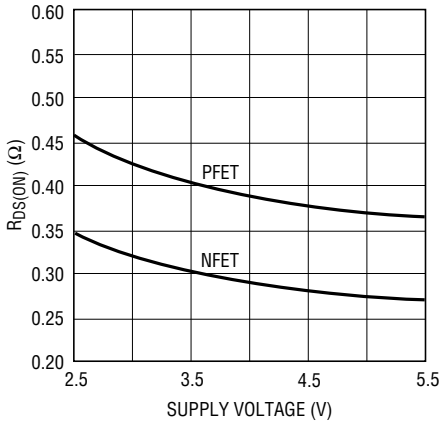


Bias Current and Shutdown Current vs Temperature

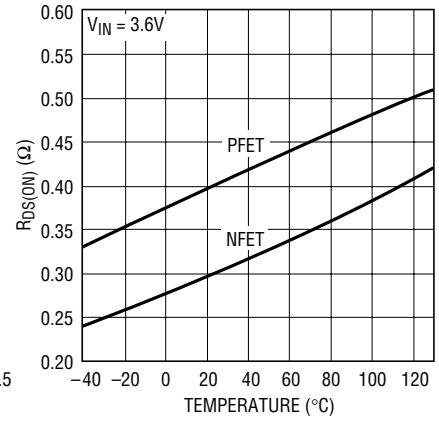


TYPICAL PERFORMANCE CHARACTERISTICS

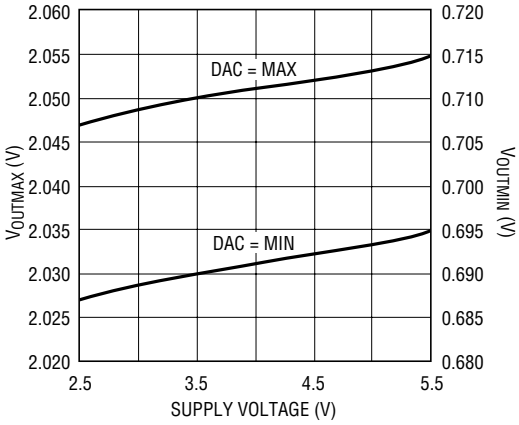
$R_{DS(ON)}$ vs Supply Voltage



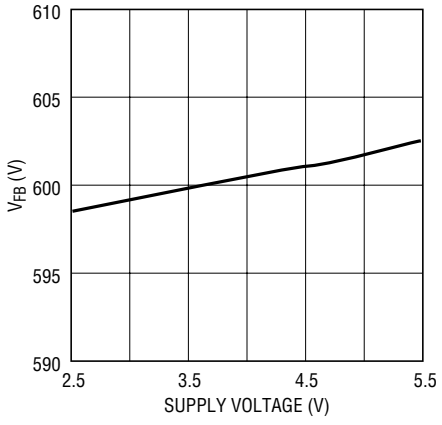
$R_{DS(ON)}$ vs Temperature



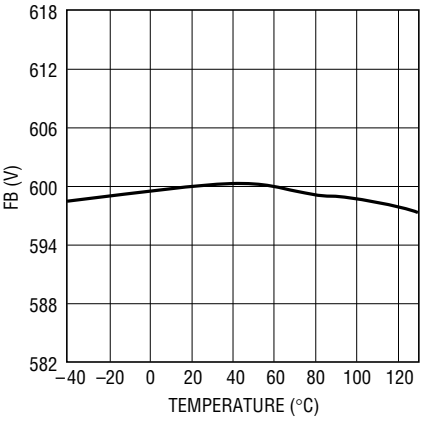
Output Voltage vs Supply Voltage



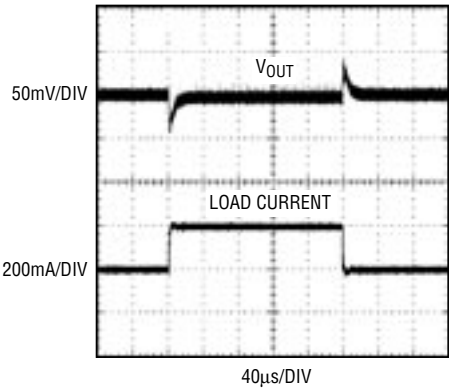
Feedback Reference vs Supply Voltage



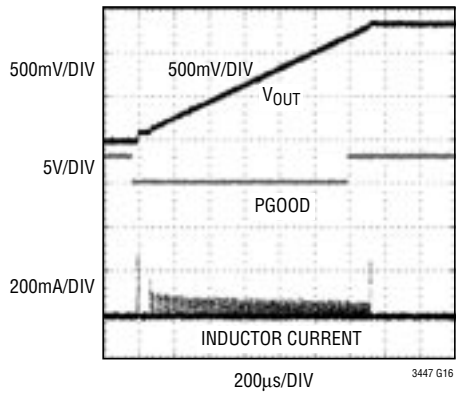
Feedback Voltage vs Temperature



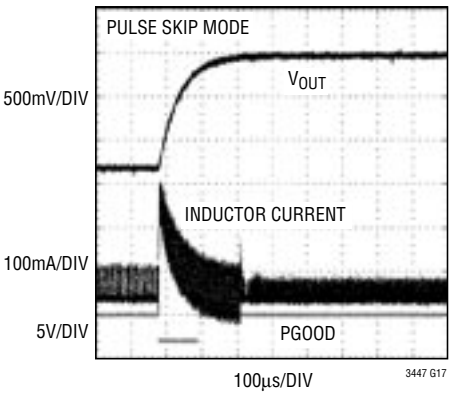
Load Step (200mA to 400mA)



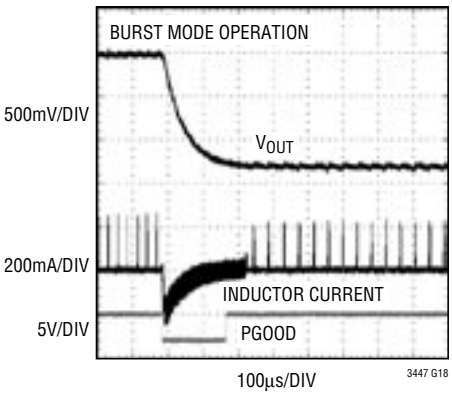
Soft-Start with No Load



$V_{OUT(MIN)}$ to $V_{OUT(MAX)}$ Transition



$V_{OUT(MAX)}$ to $V_{OUT(MIN)}$ Transition



PIN FUNCTIONS

V_{OUT} (Pin 1): Output Voltage Sensing Pin. An internal resistor divider provides the divided down feedback reference for comparison.

GND (Pin 2): Ground for all Circuits Excluding the Internal Synchronous Power NFET.

FB (Pin 3): Feedback Sensing Pin for the Optional External Feedback Resistors. Must be tied to V_{IN} if there are no external feedback resistors.

PGOOD (Pin 4): Fault Report. Open drain driver sinks current when V_{OUT} is 10% out of tolerance. Blanking during DAC changes can be enabled via the I^2C.

V_{IN} (Pin 5): Main Supply Pin. Must be closely decoupled to GND with a 2.2µF or greater capacitor.

SW (Pin 6): Switch Node Connector to Inductor. This pin connects the drains of the internal main and synchronous power MOSFET switches.

RUN (Pin 7): Run Control Input. Forcing pin above 1.5V enables the part. Forcing the pin below 0.3V shuts down the device. In shutdown, all functions are disabled drawing <1µA of supply current. Do not leave the RUN pin floating.

SCL (Pin 8): I^2C Clock Input.

V_{CCD} (Pin 9): I^2C Power Rail.

SDA (Pin 10): I^2C Data Input.

Exposed Pad (Pin 11): Ground. Must be connected to PCB ground for electrical contact and optimized thermal performance.

BLOCK DIAGRAM

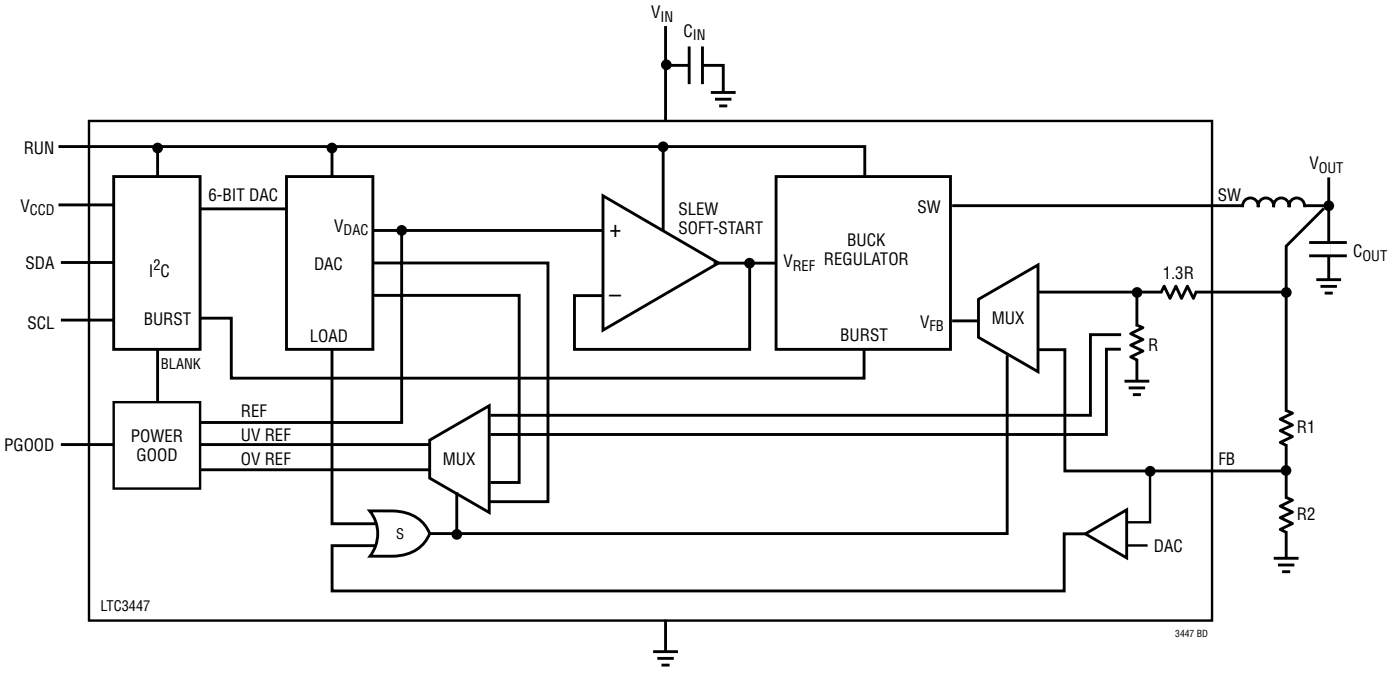


Figure 2. LTC3447 High Level Block Diagram

OPERATION

BUCK OPERATION

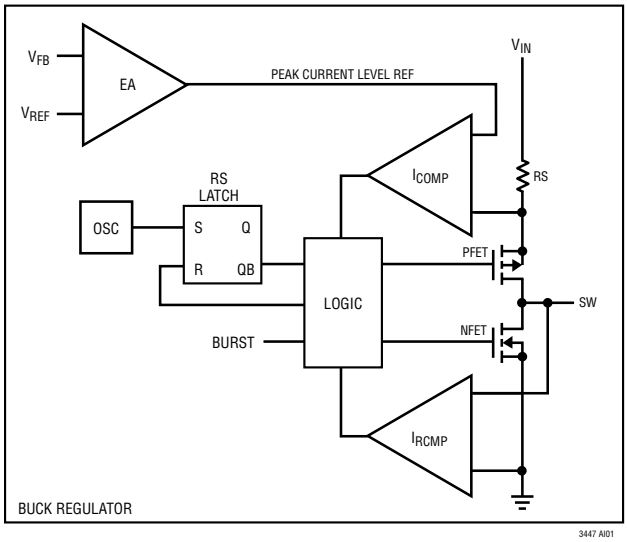


Figure 3. LTC3447 Buck Regulator Diagram

Main Control Loop

The LTC3447 uses current mode step-down architecture with both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, I_{COMP}, resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch, is controlled by the output of error amplifier EA. When the load current increases, it causes a slight decrease in the feedback voltage, FB, relative to an internal reference voltage, which in turn, causes the EA amplifier's output voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator I_{RCMP}, or the beginning of the next clock cycle.

Burst Mode Operation

The LTC3447 is capable of Burst Mode operation in which the internal power MOSFETs operate intermittently based on load demand. Burst Mode operation can be disabled via the I^2C interface. When Burst Mode operation is disabled, the regulator is in pulse skipping mode operation.

During Burst Mode operation, the LTC3447's internal circuits sense when the inductor peak current falls below 50mA. When below this level, the power MOSFETs and any unneeded circuitry are turned off, reducing the quiescent current to 33µA, and the peak current level reference level is held at 150mA. The LTC3447 remains in this sleep state until the output voltage falls below the output voltage setting. Once this occurs, the regulator wakes up and allows the inductor to develop 150mA current pulses. For light loads, this will cause the output voltage to increase and the internal peak current reference to decrease. When the peak current reference falls to below 50mA, the part re-enters sleep mode and the cycle is repeated. This process repeats at a rate that is dependent on the load demand.

Pulse Skipping Mode Operation

At light loads, the inductor current may reach zero or reverse on each pulse. The bottom MOSFET is turned off by the current reversal comparator, I_{RCMP}, and the switch voltage will ring. This is discontinuous mode operation, and is normal behavior for a switching regulator. At very light loads, the LTC3447 will automatically skip pulses in pulse skipping mode operation to maintain output regulation. This feature is enabled when the Burst Mode operation is disabled.

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator is reduced to about 160kHz. This frequency foldback ensures that the inductor current has more time to decay, thereby preventing thermal runaway. The oscillator's frequency will progressively increase to 1MHz when V_{OUT} rises above 0V.

Dropout Operation

When using the optional external feedback resistors, it is possible for V_{IN} to approach the output voltage level. As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor.

An important detail to remember is that at low input supply voltages, the $R_{DS(ON)}$ of the P-channel switch increases (see Typical Performance Characteristics). Therefore,

OPERATION

the user should calculate the power dissipation when the LTC3447 is used at 100% duty cycle with low input voltage (See Thermal Considerations in the Applications Information section).

Low Supply Operation

The LTC3447 will operate with input supply voltages as low as 2.5V, but the maximum allowable output current is reduced at this low voltage. Figure 4 shows the reduction in the maximum output current as a function of input voltage for various output voltages.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles >40%; however, the LTC3447 uses a patent-pending scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

DAC

The I^2C interface is used to control the internal voltage DAC for the buck regulator. The output voltage range is 0.69V to 2.05V in 21.6mV steps. The default DAC setting is 100000 which equates to a 1.38V output voltage. Output voltage transitions begin once the I^2C interface receives the STOP command.

Slew Rate

The LTC3447 has a slew rate of approximately 11mV/µs. The slew rate is controlled by the RC time constant of a low pass filter at the voltage DAC output. Figure 5 shows a typical transition from min to max DAC settings.

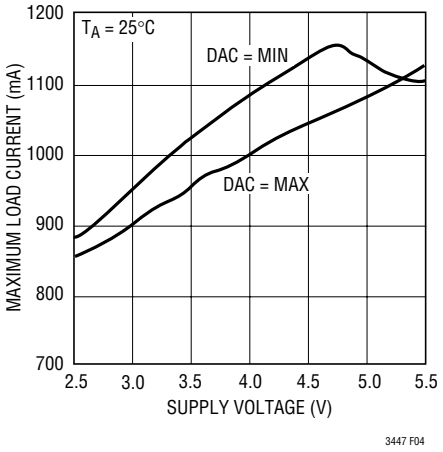


Figure 4. Maximum Load Current vs Supply Voltage

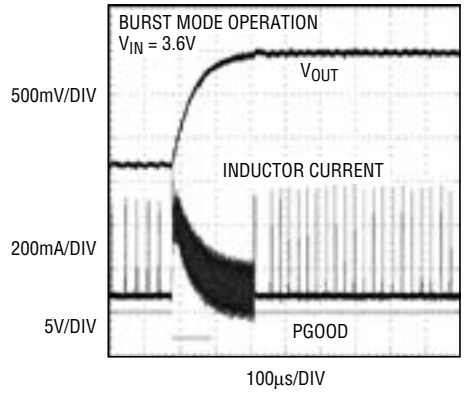


Figure 5.Transition from DAC = MIN to DAC = MAX

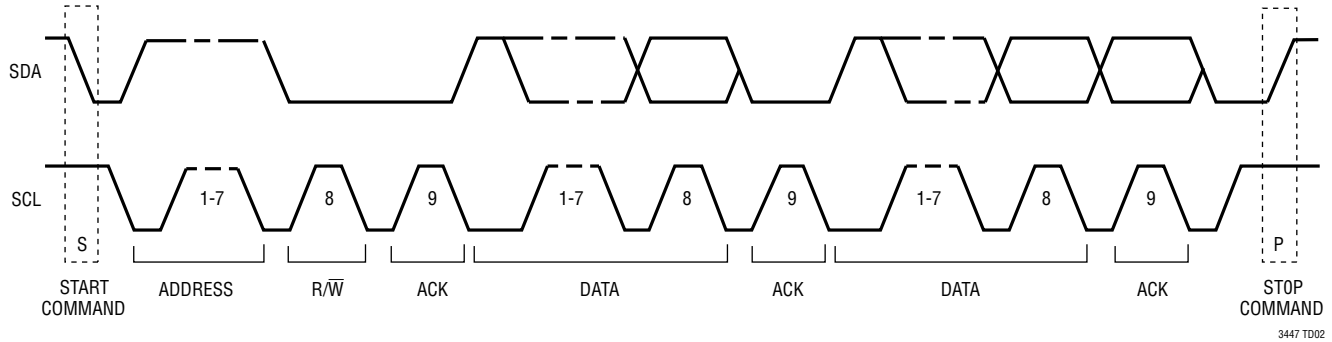


Figure 6. Typical I^2C Write Protocol

OPERATION

External Start-Up Option

The LTC3447 allows for the use of optional external resistors to determine the start-up voltage. Using this option, the start-up voltage can be set to levels inside or outside the DAC output's operating range. The output voltage will be regulated at this value until the internal DAC is updated and a STOP command is received. Once the STOP command is received, the internal DAC will retain control of the output voltage until the part is disabled then enabled again.

If this feature is not used, the feedback pin must be tied to V_{IN}.

I²C OPERATION

- Typical 2-wire serial I²C
- Serial interface
- Simple 2-wire interface
- Multiple devices on same bus
- Idle bus must have SDA and SCL lines high
- LTC3447 is write only
- Master controls bus
- Devices listen for unique address that precedes data

General I²C Bus/SMBus Description

I²C Bus and SMBus are reasonably similar examples of two wire, bidirectional, serial communications busses. Calling them two wire is not strictly accurate, as there is an implied third wire, which is the ground line. Large ground drops or spikes between the grounds of different parts on the bus can interrupt or disrupt communications, as the signals on the two wires are both inherently referenced to a ground which is expected to be common to all parts on the bus. Both bus types have one data line and one clock line which are externally pulled to a high voltage when they are not being controlled by a device on the bus. The devices on the bus can only pull the data and clock lines low, which makes it simple to detect if more than one device is trying to control the bus; eventually, a device will release a line and it will not pull high because another device is still holding it low. Pull-ups for the data and clock lines are usually provided by external discrete resistors, but external current sources can also be used. Since there are no dedicated lines to use to tell a given device if another device is trying to communicate with it, each device must have a unique address to which it will respond. The first part of any communication is to send out an address on the bus and wait to see if another device responds to it. After a response is detected, meaningful data can be exchanged between the parts.

Typically, one device will control the clock line at least most of the time and will normally be sending data to the other parts and polling them to send data back to it, and this device is called the master. There can certainly be more than one master, since there is an effective protocol to resolve bus contentions, and nonmaster (slave) devices can also control the clock to delay rising edges and give themselves more time to complete calculations or communications (clock stretching). Slave devices need to be able to control the data line to acknowledge communications from the master, and some devices will need to able to send data back to the master; they will be in control of the data line while they are doing so. Many slave devices will have no need to stretch the clock signal and will have no ability to pull the clock line low, which is the case with the LTC3447.

Data is exchanged in the form of bytes, which are 8-bit packets. Every byte needs to be acknowledged by the slave (data line pulled low) or not acknowledged by the master (data line left high), so communications are broken up into 9-bit segments, one byte followed by one bit for acknowledging. For example, sending out an address consists of 7-bits of device address, 1-bit that signals whether a read or write operation will be performed, and then 1 more bit to allow the slave to acknowledge. There is no theoretical limit to how many total bytes can be exchanged in a given transmission.

I²C and SMBus are very similar specifications, SMBus having been derived from I²C. In general, SMBus is targeted toward low power devices (particularly battery powered ones) and emphasizes low power consumption, while I²C is targeted toward higher speed systems where the power consumption of the bus is not so critical. I²C has three different specifications for three different maximum speeds, these being standard mode (100kHz max), fast mode (400kHz max), and HS mode (3.4MHz max). Standard and fast mode are not radically different, but HS mode is very different from a hardware and software perspective and requires an initiating command at standard or fast speed before data can start transferring at HS speed. SMBus simply specifies a 100kHz maximum speed.

OPERATION

The START and STOP Commands

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START command by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP command by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. An acknowledge signal (LOW active) is generated by the slave lets the master know that the latest byte of information was received. The acknowledge-related clock pulse is generated by the master. The transmitter master releases the SDA line (HIGH) during the acknowledge clock pulse. The slave receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

When a slave receiver doesn't acknowledge the slave address (for example, it's unable to receive because it's performing some real-time function), the data line must be left HIGH by the slave. The master can then generate a STOP command to abort the transfer.

If a slave receiver does acknowledge the slave address but, some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP command. The data line is also left high by the slave and master after a slave has transmitted a byte of data to the master in a read operation, but this is a not acknowledge that indicates that the data transfer is successful.

Commands Supported

The LTC3447 supports only write byte commands to a single register. During ACK bit periods, the LTC3447 will pull the data line low to acknowledge the master device. See Figure 7.

Data Transfer Timing for Write Commands

In order to help assure that bad data is not written into the part, data from a write command is only stored after a valid STOP command has been performed.

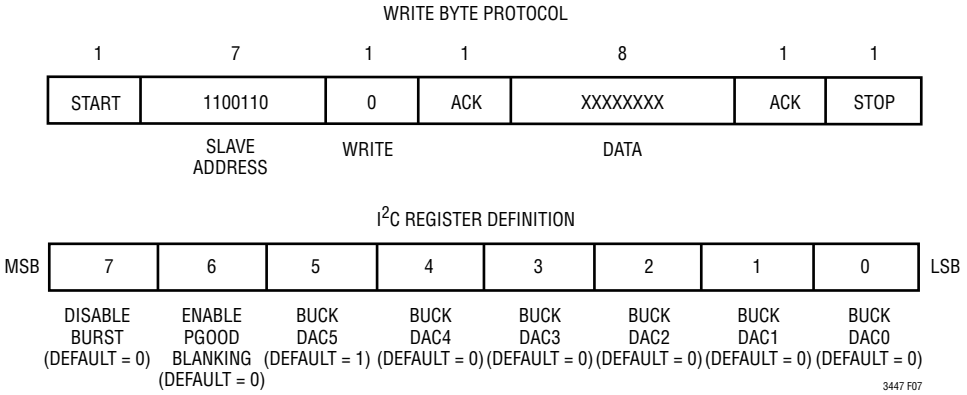


Figure 7. LTC3447's Write I²C Protocol

OPERATION

Table 1. I^2C Fast-Mode Timing Specifications (for Reference)

f_{I2C}	I^2C Operating Frequency			0		400	kHz
t_{BUF}	Bus free time between Stop and Start Condition			1.3			µs
$t_{HD,RSTA}$	Hold Time after (Repeated) Start Condition			0.6			µs
$t_{SU,RSTA}$	Repeated Start Condition Setup Time			0.6			µs
$t_{SU,STOP}$	Stop Condition Setup Time			0.6			µs
$t_{HD,DAT}$	Data Hold Time			0		0.9	ns
$t_{SU,DAT}$	Data Setup Time			100			ns
t_{LOW}	Clock Low Period			1.3			µs
t_{HIGH}	Clock High Period			0.6			µs
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter			0		50	ns
t_f	Clock, Data Fall Time			$20 + 0.1 \cdot C_B$		300	ns
t_r	Clock, Data Rise Time			$20 + 0.1 \cdot C_B$		300	ns

C_B = Capacitance of one bus line.

APPLICATIONS INFORMATION

The basic LTC3447 application circuit is shown on the front page of the data sheet. External component selection is driven by the load requirement and begins with the selection of L1 followed by C_{IN} and C_{OUT}.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1µH to 4.7µH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in Equation 1. A reasonable starting point for setting ripple current is ΔI_L = 240mA (40% of 600mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 920mA rated inductor should be enough for most applications (800mA + 120mA). For better efficiency, choose a low DC resistance inductor.

The inductor value also has an effect on Burst Mode operation. The transition to low current operation begins when the inductor current peaks fall to approximately 50mA. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered-iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price versus size requirements and any radiated field/EMI requirements than on what the LTC3447 requires to operate. Table 2 shows some typical surface mount inductors that work well in LTC3447 applications.

Table 2.

Manufacturer Part Number	Value (µH)	DCR (mΩ max)	Max DC Current (A)	Size W x L x H (mm^3)
Sumida CDRH3D16/HP3R3	3.3	85	1.4	4.0 x 4.0 x 1.8
Sumida CR434R7	4.7	109	1.15	4.0 x 4.5 x 3.5
Murata LQH55DN2R2M03	2.2	29	3.2	5.0 x 5.0 x 4.7
Toko D52LC-A914BYW-2R2M	2.2	59	1.63	5.0 x 5.0 x 2.0

APPLICATIONS INFORMATION

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}} \quad (2)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right) \quad (3)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3447's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN}, large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

The LTC3447 has an internal resistor divider network tied to the OUT pin. The output voltage is controlled by a DAC (6-bit register) whose setting is programmed via the I^2C interface. The DAC controls the V_{OUT} range of 0.69V to 2.05V in 21.6mV steps. The default value for V_{OUT} is 1.38V and is reset to this value whenever V_{IN} comes up.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in LTC3447 circuits: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R

APPLICATIONS INFORMATION

loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence as illustrated in Figure 8.

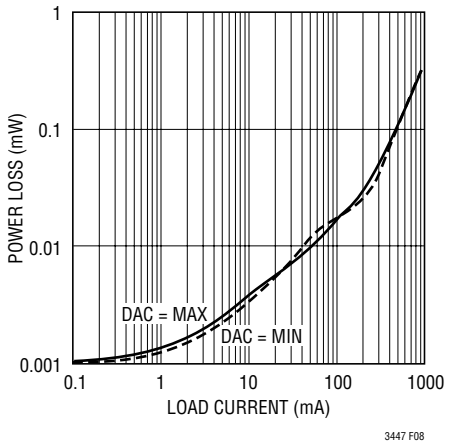


Figure 8. Power Loss vs Load Current

The V_{IN} quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(QT + QB)$ where QT and QB are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{LOAD} • ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal.

The regulator loop then acts to return V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. For a detailed explanation of switching control loop theory, see Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25 • C_{LOAD}). Thus, a 10µF capacitor charging to 3.3V would require a 250µs rise time, limiting the charging current to about 130mA.

Thermal Considerations

In most applications the LTC3447 does not dissipate much heat due to its high efficiency. But, in applications where the LTC3447 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3447 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum

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junction temperature of the part. The temperature rise is given by:

$$T_R = \theta_{JA} \bullet P_D$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the temperature.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider the LTC3447 when using an input voltage of 3.6V, an ambient temperature of 70°C, and a buck load current of 500mA. From the typical performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 70°C is approximately 0.45Ω. Therefore, power dissipated by the part is:

$$P_D = I_{LOAD}^2 \bullet R_{DS(ON)} = 112.5mW$$

For the DFN-10 package, the θ_{JA} is 43°C/W. Thus, the junction temperature of the regulator is:

$$T_J = 70°C + (0.1125)(43) = 74.8°C$$

which is well below the maximum junction temperature of 150°C. Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3447. These items are also illustrated graphically in Figures 9 and 10. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace, and the V_{IN} trace should be kept short, direct and wide.

2. Does the V_{OUT} pin connect directly to the output voltage reference? Ensure that there is no load current running from the output voltage and the V_{OUT} sense pin.

3. Does the FB pin connect directly to the feedback voltage reference? Ensure that there is no load current running from the feedback reference voltage and the FB pin.

4. Does the (+) plate of C_{IN} connect to V_{IN} as closely as possible? This capacitor provides the AC current to the internal power MOSFETs.

5. Keep the switching node, SW, away from the sensitive V_{OUT} and FB nodes.

6. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.

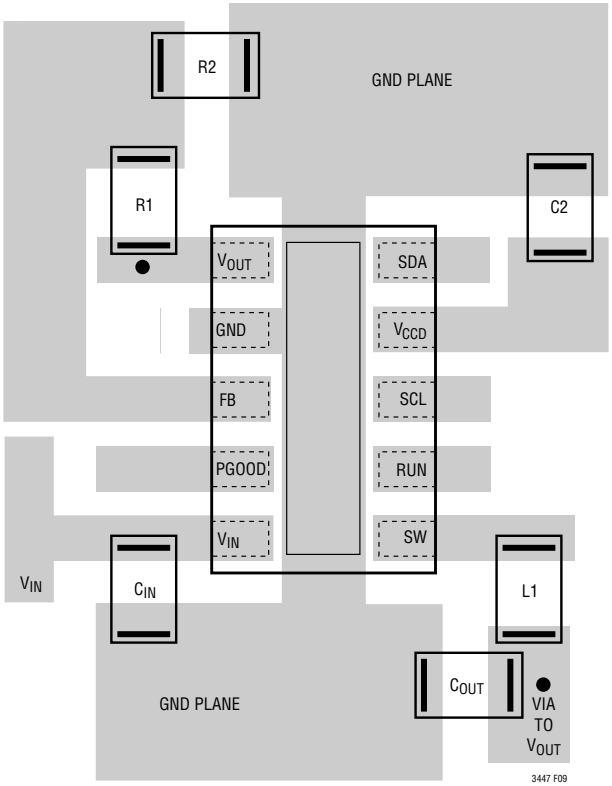


Figure 9. LTC3447 Suggested Layout

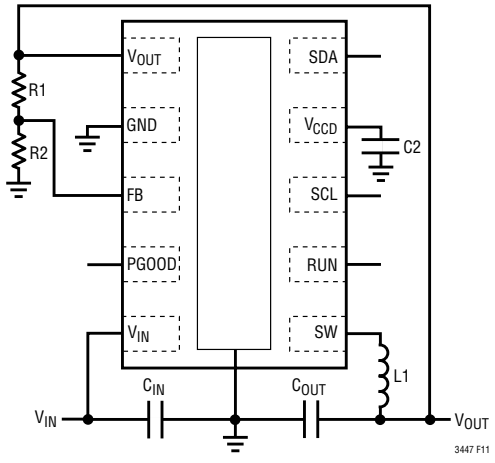


Figure 10. LTC3447 Layout Diagram

APPLICATIONS INFORMATION

Design Example

As a design example, assume the LTC3447 is used in a single lithium-ion battery-powered cellular phone application. The V_{IN} will be operating from a maximum of 4.2V down to about 2.7V. The normal load current requirement is a maximum of 500mA at 1.4V, but most of the time it will be in standby mode, requiring only 200µA at 1V. Efficiency at both low and high load currents is important.

To ensure that the ripple currents and voltages do not exceed desired expectations over the DAC output range, calculations with maximum V_{IN} and minimum V_{OUT} should be used. Note that either increasing the output voltage or decreasing V_{IN} will result in a decrease of ripple current and voltage. Choosing a maximum ripple current, ΔI_L, of 280mA, Equation 1 can be used to determine the size of the inductor that should be used.

$$L = \frac{1}{(1MHz)(280mA)} \bullet 1.4V\left(1-\frac{1.4V}{4.2V}\right) = 3.3\mu H$$

A 3.3µH inductor works well for this application. For best efficiency choose a 640mA or greater inductor with less than 0.2Ω series resistance.

C_{IN} will require an RMS current of at least 0.25A, approximately $I_{LOAD(MAX)}/2$, overtemperature (see Equation 2). For C_{OUT}, selecting a 4.7µF capacitor with an ESR of 0.25Ω yields the following ripple voltage using Equation 3.

$$\Delta V_{OUT} = 0.280A\left(0.25\Omega + \frac{1}{8(1MHz)(4.7\mu F)}\right) =$$

$$70mV + 7.4mV = 77.4mV$$

Note that the majority of the ripple voltage is generated by the capacitor's ESR. Most ceramic capacitors will have a typical ESR of 10mΩ or less. Selecting capacitors with low ESRs will significantly reduce the ripple voltage.

Efficiency can be improved by taking advantage of the LT3447's Burst Mode operation. When entering the standby mode, ensure that the burst disable bit is set to 0 when the output voltage DAC is updated. Likewise, when entering a heavy current load mode, ensure the burst disable bit is set to 1 when the output voltage DAC is updated. Figure 11 shows the advantage of utilizing the Burst Mode function.

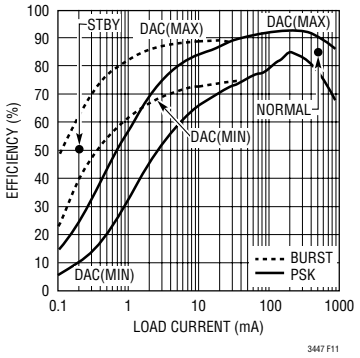
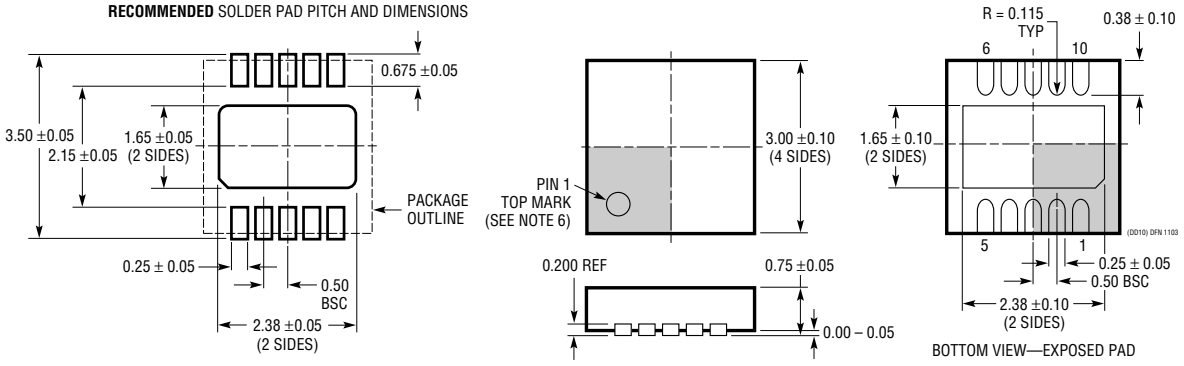


Figure 11. Efficiency vs Load Current (V_{IN} = 4.2V)

PACKAGE DESCRIPTION

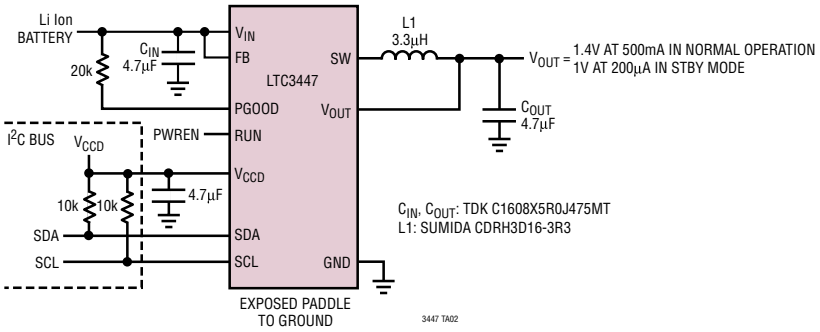
DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Li-Ion Battery to 1.4V/1V Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1761	100mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, Dropout Voltage = 0.30V, I_Q = 20µA, I_{SD} < 1µA, V_{OUT} = Adj, 1.5V, 1.8V, 2V, 2.5V, 2.8V, 3V, 3.3V, 5V, ThinSOT™ Package. Low Noise < 20µ$V_{RMS(P-P)}$, Stable with 1µF Ceramic Capacitors
LT1762	150mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, Dropout Voltage = 0.30V, I_Q = 25µA, I_{SD} < 1µA, V_{OUT} = Adj, 2.5V, 3V, 3.3V, 5V, MS8 Package. Low Noise < 20µ$V_{RMS(P-P)}$
LT1763	500mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, Dropout Voltage = 0.30V, I_Q = 30µA, I_{SD} < 1µA, V_{OUT} = 1.5V, 1.8V, 2.5V, 3V, 3.3V, 5V, S8 Package. Low Noise < 20µ$V_{RMS(P-P)}$
LTC1844	150mA, Very Low Dropout LDO	V_{IN}: 6.5V to 1.6V, $V_{OUT(MIN)}$ = 1.25V, Dropout Voltage = 0.08V, I_Q = 40µA, I_{SD} < 1µA, V_{OUT} = Adj, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V, ThinSOT Package. Low Noise < 30µ$V_{RMS(P-P)}$, Stable with 1µF Ceramic Capacitors
LT1962	300mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, Dropout Voltage = 0.27V, I_Q = 30µA, I_{SD} < 1µA, V_{OUT} = 1.5V, 1.8V, 2.5V, 3V, 3.3V, 5V, MS8 Package. Low Noise < 20µ$V_{RMS(P-P)}$
LT3020	Low V_{IN} (0.9V) Low V_{OUT} (0.2V) VLDO™	V_{IN}: 0.9V to 10V, $V_{OUT(MIN)}$ = 0.20V, Dropout Voltage = 0.15V, I_Q = 120µA, I_{SD} < 1µA, V_{OUT} = Adj, DFN Package
LTC3405/LTC3405A	300mA (I_{OUT}), 1.5MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3406/LTC3406B	600mA (I_{OUT}), 1.5MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3407	Dual 600mA, 1.5MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS10E, QFN Packages
LTC3411	1.25A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, MS10 Package
LTC3412	2.5A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converter,	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, TSSOP16E Package
LTC3445	600mA, 1.5MHz Synchronous Step-Down DC/DC Converter with Two LDOs and PowerPath™ Manager	V_{IN}: 2.5V to 5.5V, V_{OUT} = 0.85V to 1.55V, I_Q = 27µA, I_{SD} < 1µA, Two LDOs I^2C Interface, Back-Up Battery Management, QFN24
LTC3455	Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger	V_{IN}: 3V to 5.5V, Seamless Transition Between Input Sources and Li-Ion Battery, USB, 5V Wall Adapter, QFN24 Package
LTC4055	USB Power Manager and Li-Ion Battery Charger	Standalone Charger, Automatic Switchover when Input Supply is Removed
LTC4411/LTC4412	PowerPath Controllers in ThinSOT	More Efficient than Diode ORing

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