M65818AFP

Digital Amplifier Processor of S-Master* Technology

REJ03F0019-0100Z
Rev.1.00
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Description

The M65818AFP is a S-Master technique processor for digital amplifier enable to convert from multi liner-PCM digital input signal to high precise switching-pulse digital output without analog processing.

The M65818AFP has built-in 24bit sampling rate converter and digital-gain-controller.

The M65818AFP enables to realize high precise (X`tal oscillation precision) fully digital amplifier systems combining with power driver IC.

Features

- Built-in 24bit Sampling Rate Converter.
  Input Signal Sampling Rate
  from 32KHz to 192KHz(24bit Maximum).
  4 kinds of Digital Input Format.
- Built-in L/R Independent Digital Gain Control.
- Built-in Soft Mute Function with Exponential Approximate-Curve.
- Correspondence for SACD signal (64Fs 1bit,Fs=44.1KHz).
- Direct Output from Sampling Rate Converter.
- 3.3V and 5.0V Power Supply Operation at Output Clock, Input Data, and Control Signal Port

Main Applications

- Master Clock
  Primary Clock: 256Fsi/512Fsi Secondary Clock: 1024Fso/512Fso
- Input Signal Format:
  MSB First Right Justified(16/20/24bit),MSB First Left Justified(24bit)
  LSB First Right Justified(24bit),I2S(24bit)
- Input Signal Sampling Rate from 32kHz to 192kHz.
- 8Fs Input Mode: Correspondence for External Digital Filter, Sampling Rate Converter Outputs.
- Gain Control Function:
  +30dB~ -∞dB(0.1dB Step until -96dB, -138dB Minimum)
- Third Order ΔΣ (16Fso:6bit/5bit,32Fso: 5bit)
- Sampling Rate Converter Output :MSB First Left justified /Lch,Rch Independent/32BCK

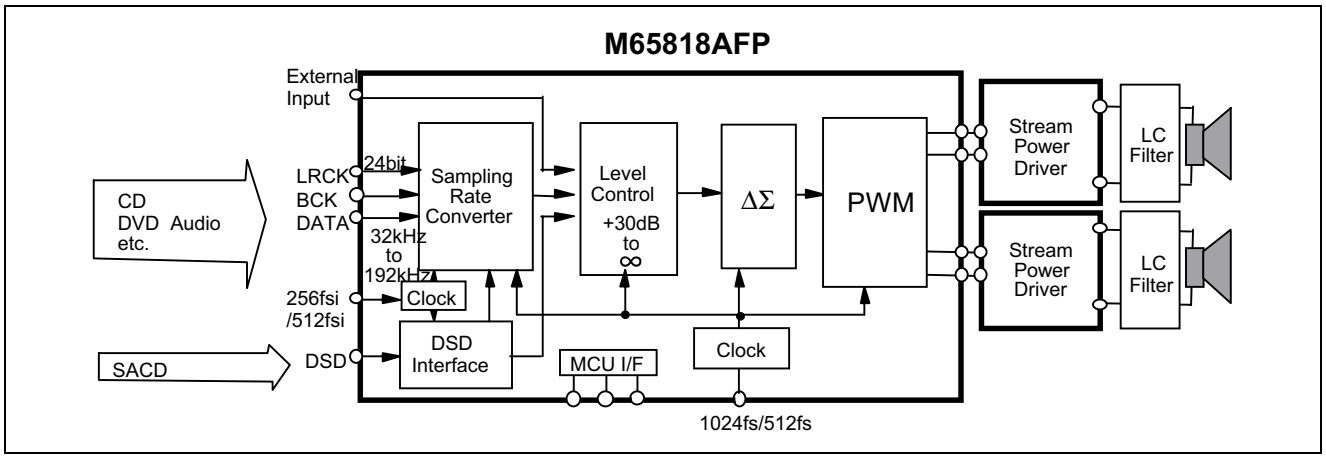
Recommended Operating Conditions

Logic Block:3.3V±10%, PWM Buffer Block : 5.0V±10%

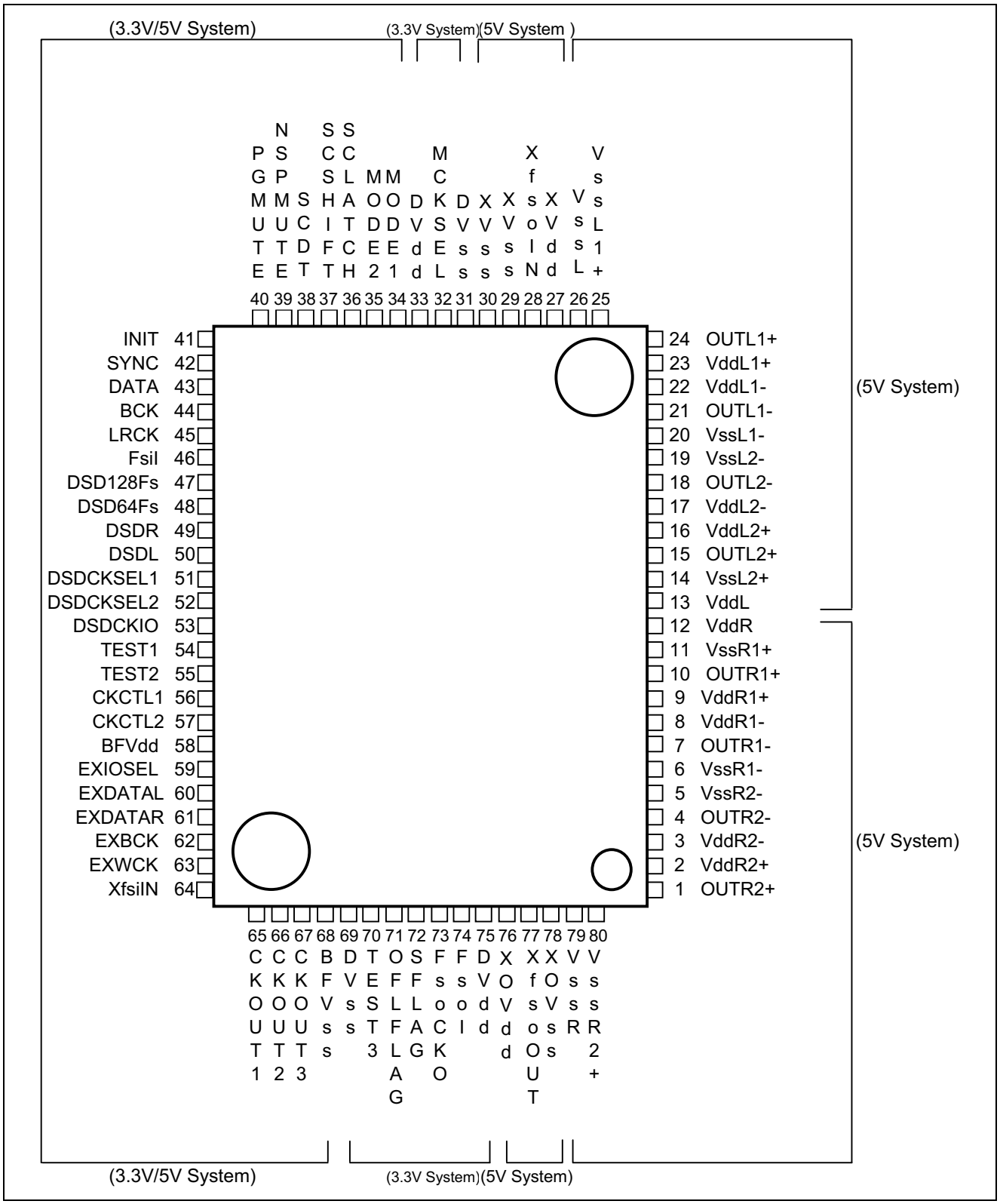
(** "S-Master" is the digital amplifier technology developed by Sony Corporation.

"S-Master" is a trademark of Sony Corporation.

System Block Diagram



1. Pin Configuration (Top View)

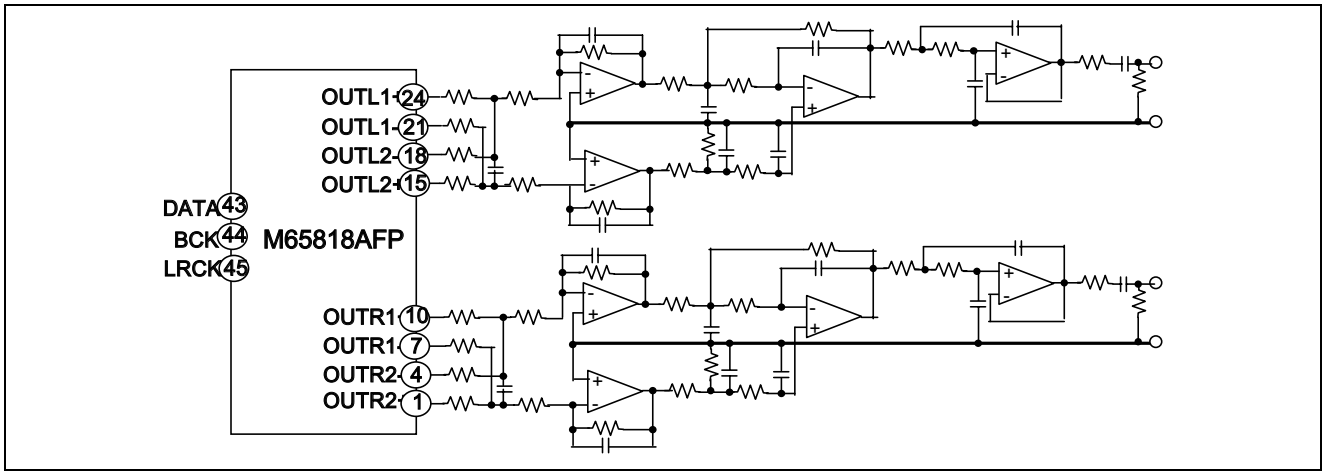


A-1 Difference between M65818AFP and M65817AFP

M65818AFP has added the following functions to M65817AFP.

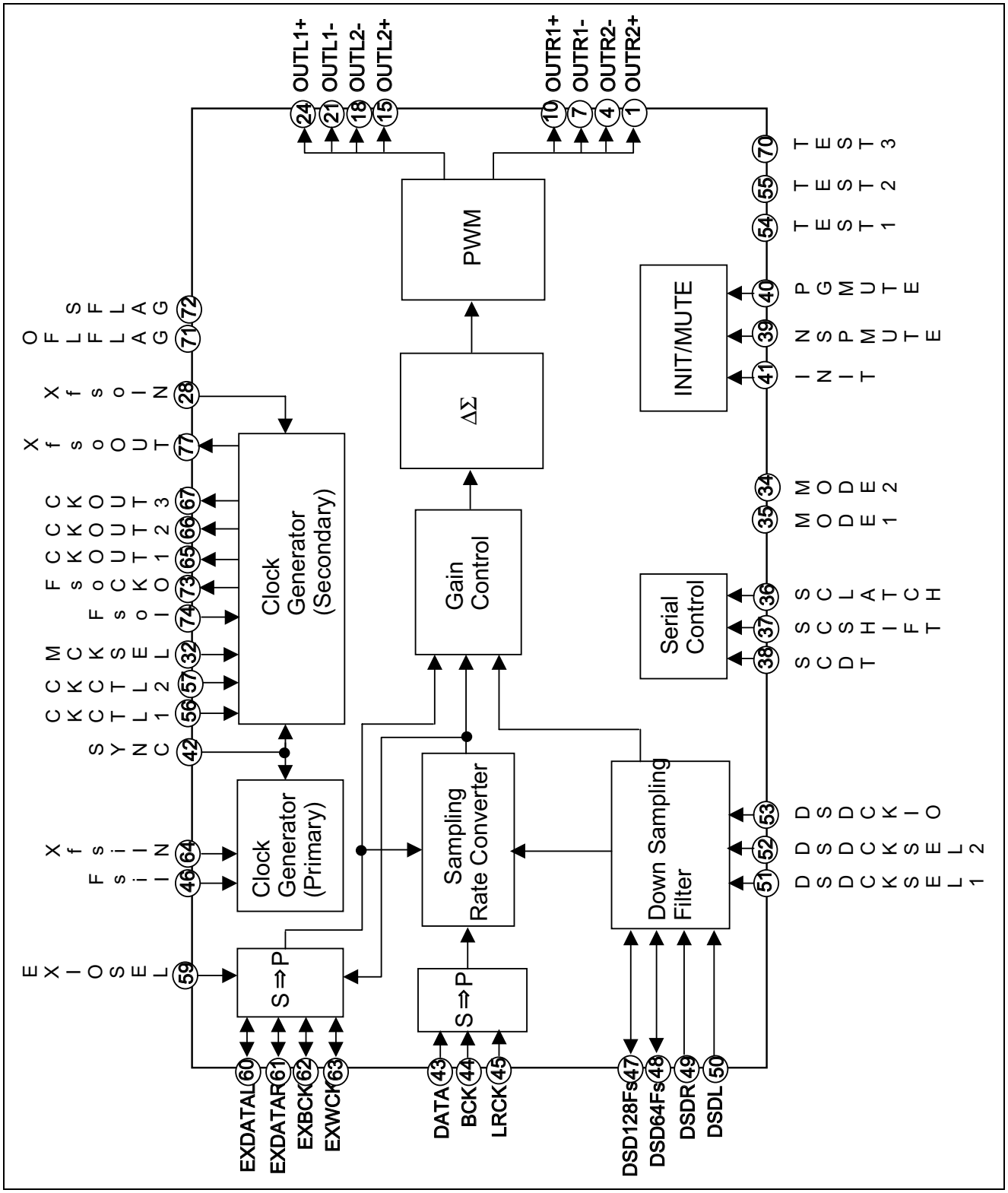
	M65817AFP	M65818AFP
PWM Output Form	General Pulse Width Modulation	Selectable 4 kind of Output Form (Refer to M65818AFP Data Sheet: P28/38 System1Mode bit22,23)
Reverse Output Pins Function of PWM Output "OUTL1-/R1-"	Reverse Phase between OUTL1+/R1+ and OUTL1-/R1-	Selectable phase between OUTL1+/R1+ and OUTL1-/R1- to Same/Reverse (Refer to M65818AFP Data Sheet: P28/38 System1Mode bit24)
ΔΣOperation Ratio	16fso Fixed	Selectable operation ratio to 16fso/32fso (Refer to M65818AFP Data Sheet: P31/38 System2 Mode bit16)
Selection of Muting operation at Primary Side Asynchronous Detection	PWM Output Duty 50% Mute at primary side asynchronous detection	Selectable PWM Output Duty 50% Mute On/Off at primary side asynchronous detection (Refer to M65818AFP Data Sheet: P28/38 System1Mode bit20)
Selection of External 8Fs Data Input Mode	Only synchronize to secondary side clock (Input the data to Gain Control Block)	Added the function of synchronization to primary side clock: Input the data to Sampling Rate Converter (Refer to M65818AFP Data Sheet: P28/38 System1Mode bit21)

A-2 The Example of Evaluation Circuit



Reference Characteristics		Condition
S/N	104dB(typ)	• Input Signal : 1kHz 0dB Full scale sine wave • Fs : Primary Clock 44.1kHz, Secondary Clock 48kHz • PWM Output Format1 • AC dithering E • DC dithering 0.1% • Gain Data Setting:(Index)10000b/(Mantissa)10000000b • THD+N : Filter 20kHz LPF S/N : Filter 20kHz LPF + JIS-A
THD+N	0.0014%(typ)	

2. Block Diagram



3. Pin Descriptions

Pin No.	Name	I/O	Description	Output Current 5V/3.3V	Signal Level
1	OUTR2+	O	Rch PWM2(+) Output		5V
2	VddR2+		Power Supply for Rch PWM2(+) (5V)	—	—
3	VddR2-		Power Supply for Rch PWM2(-) (5V)	—	—
4	OUTR2-	O	Rch PWM2 (-) Output		5V
5	VssR2-		GND for Rch PWM2(-)	—	—
6	VssR1-		GND for Rch PWM1(-)	—	—
7	OUTR1-	O	Rch PWM1 (-) Output		5V
8	VddR1-		Power Supply for Rch PWM1(-) (5V)	—	—
9	VddR1+		Power Supply for Rch PWM1(+) (5V)	—	—
10	OUTR1+	O	Rch PWM1 (+) Output		5V
11	VssR1+		GND for Rch PWM1(+)	—	—
12	VddR		Power Supply for Rch PWM (5V)	—	—
13	VddL		Power Supply for Lch PWM (5V)	—	—
14	VssL2+		GND for Lch PWM2(+)	—	—
15	OUTL2+	O	Lch PWM2 (+) Output		5V
16	VddL2+		Power Supply for Lch PWM2(+) (5V)	—	—
17	VddL2-		Power Supply for Lch PWM2(-) (5V)	—	—
18	OUTL2-	O	Lch PWM2 (-) Output		5V
19	VssL2-		GND for Lch PWM2(-)	—	—
20	VssL1-		GND for Lch PWM1(-)	—	—
21	OUTL1-	O	Lch PWM1 (-) Output		5V
22	VddL1-		Power Supply for Lch PWM1(-) (5V)	—	—
23	VddL1+		Power Supply for Lch PWM1(+) (5V)	—	—
24	OUTL1+	O	Lch PWM1 (+) Output		5V
25	VssL1+		GND for Lch PWM1(+)	—	—
26	VssL		GND for Lch PWM	—	—
27	XVdd		Power Supply for Master Clock Buffer	—	—
28	XfsoIN	I	Secondary Master Clock Input:1024Fso/512Fso	—	5V
29	XVss		GND for Master Clock Buffer	—	—
30	XVss		GND for Master Clock Buffer	—	—
31	DVss		GND for Digital Block	—	—
32	MCKSEL	I	Secondary Master Clock Selection; L:1024Fso, H:512Fso	—	3.3V
33	DVdd		Power Supply for Digital Block (3.3V)	—	—
34	MODE1	I	Input Mode Selection 1	—	5V/3.3V
35	MODE2	I	Input Mode Selection 2	—	5V/3.3V
36	SCLATCH	I	Serial Control•Latch Signal Input	—	5V/3.3V
37	SCSHIFT	I	Serial Control•Shift Clock Input	—	5V/3.3V
38	SCDT	I	Serial Control•Data Input	—	5V/3.3V
39	NSPMUTE	I	PWM Duty 50% Mute (L :Active)	—	5V/3.3V
40	PGMUTE	I	PWM G-MUTE (L :Active)	—	5V/3.3V

Pin No.	Name	I/O	Description	Output Current 5V/3.3V	Signal Level
41	INIT	I	Initialize Input(Power Supply Reset): ; L:Reset, H:Release	—	5V/3.3V
42	SYNC	I	Synchronous Set of System Clock (at Rising Edge)	—	5V/3.3V
43	DATA	I	DATA Input (CD/MD / DVD audio mode) PCM Signal	—	5V/3.3V
44	BCK	I	BCK Input (CD/MD / DVD audio mode) PCM Signal	—	5V/3.3V
45	LRCK	I	LRCK Input (CD/MD / DVD audio mode) PCM Signal	—	5V/3.3V
46	FsiI	I	Primary Fsi Clock Input (SACD mode)	—	5V/3.3V
47	DSD128Fs	I/O	SACD Interface Clock(128Fs)	2mA/1.5mA	5V/3.3V
48	DSD64Fs	I/O	SACD Interface Clock(64Fs)	2mA/1.5mA	5V/3.3V
49	DSDR	I	SACD Rch Data Input	—	5V/3.3V
50	DSDL	I	SACD Lch Data Input	—	5V/3.3V
51	DSDCKSEL1	I	SACD Interface Selection 1	—	5V/3.3V
52	DSDCKSEL2	I	SACD Interface Selection 2	—	5V/3.3V
53	DSDCKIO	I	I/O Selection for SACD(64Fs,128Fs)Clock L:input,H:output	—	5V/3.3V
54	TEST1	I	TEST1 must be connected to GND.	—	5V/3.3V
55	TEST2	I	TEST2 must be connected to GND.	—	5V/3.3V
56	CKCTL1	I	fso System Clock(CKOUT1,2,3) Output Selection 1	—	5V/3.3V
57	CKCTL2	I	fso System Clock(CKOUT1,2,3) Output Selection 2	—	5V/3.3V
58	BFVdd		Power Supply for Input/Output (3.3V/5V)Buffer	—	—
59	EXIOSEL	I	8Fs Data Input/Output Selection L:Input H:Output	—	5V/3.3V
60	EXDATAL	I/O	8Fs Data Lch	2mA/1.5mA	5V/3.3V
61	EXDATAR	I/O	8Fs Data Rch	2mA/1.5mA	5V/3.3V
62	EXBCK	I/O	BCK for 8fs Data (32BCK=1WCK)	2mA/1.5mA	5V/3.3V
63	EXWCK	I/O	Word Clock for 8fs Data (1WCK=32BCK)	2mA/1.5mA	5V/3.3V
64	XfsiIN	I	Primary Master Clock Input (256fsi/512fsi)	—	5V/3.3V
65	CKOUT1	O	fso System Clock Output 1	4mA/3mA	5V/3.3V
66	CKOUT2	O	fso System Clock Output 2	4mA/3mA	5V/3.3V
67	CKOUT3	O	fso System Clock Output 3	4mA/3mA	5V/3.3V
68	BFVss		GND for Digital Block Input/Output Buffer	—	—
69	DVss		GND for Digital Block	—	—
70	TEST3	I	TEST3 must be connected to GND.	—	3.3V
71	OFLFLAG	O	Overflow Detector Flag of Digital Operation (H :Active)	2mA	3.3V
72	SFLAG	O	Asynchronous Flag (H :Active)	2mA	3.3V
73	FsoCKO	O	Secondary Fso Clock Output	4mA	3.3V
74	FsoI	I	Secondary Fso Clock Input	—	3.3V
75	DVdd		Power Supply for Digital Block(3.3V)	—	—
76	XOVdd		Power Supply for Secondary Master Clock Buffer(5V)	—	—

Pin No.	Name	I/O	Description	Output Current 5V/3.3V	Signal Level
77	XfsoOUT	O	Buffered Output of Secondary Master Clock (1024/512fso)	2mA	5V
78	XOVss		GND for Secondary Master Clock Buffer	—	—
79	VssR		GND for Rch PWM	—	—
80	VssR2+		GND for Rch PWM2(+)	—	—

4. Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions
Supply Voltage	PWMVdd	–0.3	—	6.0	V	5V XVdd, XOVdd, and Vdd (PWM).
	BFVdd	–0.3	—	6.0	V	5.0V System
	DVdd	–0.3	—	4.2	V	3.3V System
Input Voltage Range	Vi (5.0V)	–0.3	—	Vdd+0.3V	V	
	Vi (3.3V)	–0.3	—	Vdd+0.3V	V	
Power Dissipation	Pd		600		mW	Ta=60 °C
Storage Temperature	Tstg	–40	—	125	°C	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions
Supply Voltage	PWMVdd	4.5	5.0	5.5	V	5V XVdd, XOVdd, and Vdd (PWM).
	BFVdd	4.5	5.0	5.5	V	5.0V function
		3.0	3.3	3.6	V	3.3V function
	DVdd	3.0	3.3	3.6	V	
Operating Temperature	Ta	–20	—	75	°C	
Operating Frequency	XFsoIN	16	—	50	MHz	
	XFsiIN	8	—	25	MHz	

DC Characteristics

(Ta=25°C, PWMVdd=5V, DVdd=3.3V: Unless otherwise specified.)

Parameter		Symbol	Min.	Typ.	Max	Unit	Conditions
H Level Input Voltage		VIH5	0.75Vdd	—	—	V	BFVdd=4.5 to 5.5V
		VIH3	0.75Vdd	—	—	V	BFVdd=3.0 to 3.6V
L Level Input Voltage		VIL5	—	—	0.25Vdd	V	BFVdd=4.5 to 5.5V
		VIL3	—	—	0.25Vdd	V	BFVdd=3.0 to 3.6V
Input Leak Current		Ileak	—	—	10	μA	
"H"Level Output Voltage	DSD128Fs DSD64Fs EXDATAL EXDATAR EXBCK EXWCK	VOH5	Vdd – 0.5	—	—	V	BFVdd=4.5 to 5.5V IOH5=–2.0mA
		VOH3	Vdd – 0.5	—	—	V	BFVdd=3.0 to 3.6V IOH3=–1.5mA
	CKOUT1 CKOUT2 CKOUT3	VOH5	Vdd – 0.5	—	—	V	BFVdd=4.5 to 5.5V IOH5=–4.0mA
		VOH3	Vdd – 0.5	—	—	V	BFVdd=3.0 to 3.6V IOH3=–3.0mA
	XfsoOUT	VOH5	Vdd – 0.5	—	—	V	BFVdd=4.5 to 5.5V IOH5=–2.0mA
	OFLFAG SFLAG FsoCKO	VOH3	Vdd – 0.5	—	—	V	BFVdd=3.0 to 3.6V IOH3=–2.0mA
	OUTLXX OUTRXX	VOH5	Vdd – 0.5	—	—	V	VddLXX/RXX=4.5V to 5.5V IOH5=–4.0mA
"L" Level Output Voltage	DSD128Fs DSD64Fs EXDATAL EXDATAR EXBCK EXWCK	VOL5	—	—	0.5	V	BFVdd=4.5 to 5.5V IOH5=2.0mA
		VOL3	—	—	0.5	V	BFVdd=3.0 to 3.6V IOH3=1.5mA
	CKOUT1 CKOUT2 CKOUT3	VOL5	—	—	0.5	V	BFVdd=4.5 to 5.5V IOH5=4.0mA
		VOL3	—	—	0.5	V	BFVdd=3.0 to 3.6V IOH3=3.0mA
	XfsoOUT	VOL5	—	—	0.5	V	BFVdd=4.5 to 5.5V IOH5=2.0mA
	OFLFAG SFLAG FsoCKO	VOL3	—	—	0.5	V	BFVdd=3.0 to 3.6V IOH3=2.0mA
	OUTLXX OUTRXX	VOL5	—	—	0.5	V	VddLXX/RXX=4.5V to 5.5V IOH5=4.0mA
Power Supply Current		Idd		33		mA	BFVdd=5V

5. Explanation of Operation

5.1. MODE1, MODE2 34 35

The states of **MODE1** and **MODE2** pins select input signal mode.

MODE1 and **MODE2** are control pins for input signal mode (Normal / SACD / External 8fs Input).

These are selectable as follows.

Pin	Name / MODE	Normal	External 8fs Data	SACD-fsi	SACD-fso
34	MODE1	L	L	H	H
35	MODE2	L	H	L	H

- Normal mode
  The Normal is data input mode from CD,MD,DVD etc.
  Input pins are **DATA,BCK**, and **LRCK**.

- External 8fs Data mode
  In this mode, the 8fs rate data inputted from external device.
  Input pins are **EXDATAL**,**EXDATAR,EXBCK** and **EXWCK**.
  The data synchronized with the clock of **EXBCK**,**EXWCK** pins are inputted into **EXDATAL,EXDATAR** pins .
  Selectable "Input for primary side synchronization" and "Input for secondary side synchronization"
  by the serial control System1 mode bit21(EXMODE)
  In the case of primary side synchronization, the data inputted to the Sampling Rate Converter block.
  In the case of secondary side synchronization, the data inputted to Gain Control block.

- SACD-fsi mode
  In this mode, SACD format data inputted.
  Input pins are **DSDL,DSDR,DSD128Fs** and **DSD64Fs**.
  The clock of a Down Sampling Filter is given from a *primary side, and down sampled data are
  inputted into the Sampling Rate Converter block.
  The data synchronized with the clock of **DSD128Fs,DSD64Fs** pins are inputted into **DSDL,DSDR** pins.

- SACD-fso mode
  In this mode, SACD format data inputted.
  Input pins are **DSDL,DSDR,DSD128Fs** and **DSD64Fs**.
  The clock of a Down Sampling Filter is given from a *secondary side, and down sampled data are
  inputted into the Gain Control block.
  The data synchronized with the clock of **DSD128Fs,DSD64Fs** pins are inputted into **DSDL,DSDR** pins.

* primary clock: This clock means input side clock System of the sampling rate converter.
  secondary clock: This clock means output side clock System of the sampling rate converter. The block after Sampling Rate Converter (Gain Control Block, .ΔΣ Block, and PWM Block) operate with secondary clock

"fsi", "fso", and "fs" are defined as follows in this data sheet.

fsi: The primary side Sampling Frequency

fso: The secondary side Sampling Frequency

fs: The sampling frequency which can be set as both by the side of primary and secondary .

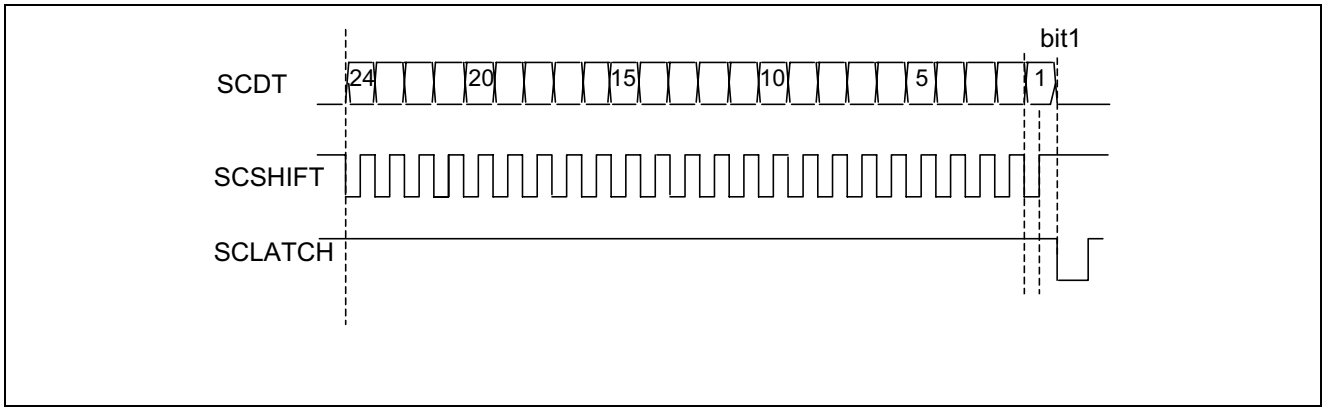
(External 8fs Data , SACD Data etc.)

5.2. SCDT, SCSHIFT, SCLATCH 38 37 36

SCDT,SCSHIFT,and **SCLATCH** are input pins for setting M65818AFP's operation.

Input format of **SCDT, SCSHIFT** and **SCLATCH** is shown below.

- Input format of **SCDT**, **SCSHIFT**, and **SCLATCH**.



- Mode Setting

The operating Mode are classified in four and assigned by bit1and bit2. These four functions are shown below.

(bit1 and bit2) = ("L" and "L") Gain control mode: Gain control.
(bit1 and bit2) = ("L "and "H") System1 Mode: Primary block initialization, etc.
(bit1 and bit2) = ("H" and "L") System2 Mode : Secondary block initialization, etc.
(bit1 and bit2) = ("H" and "H") Test mode (setting prohibition)
Refer to Chapter 6 about these four setting in detail.

5.3. DATA, BCK, LRCK 43 44 45

DATA, BCK and **LRCK** are input pins under condition of `Normal ` mode.

Input formats are supported by following 4 ways, and are set by Serial Control, "System1 Mode, bit3 and bit4".

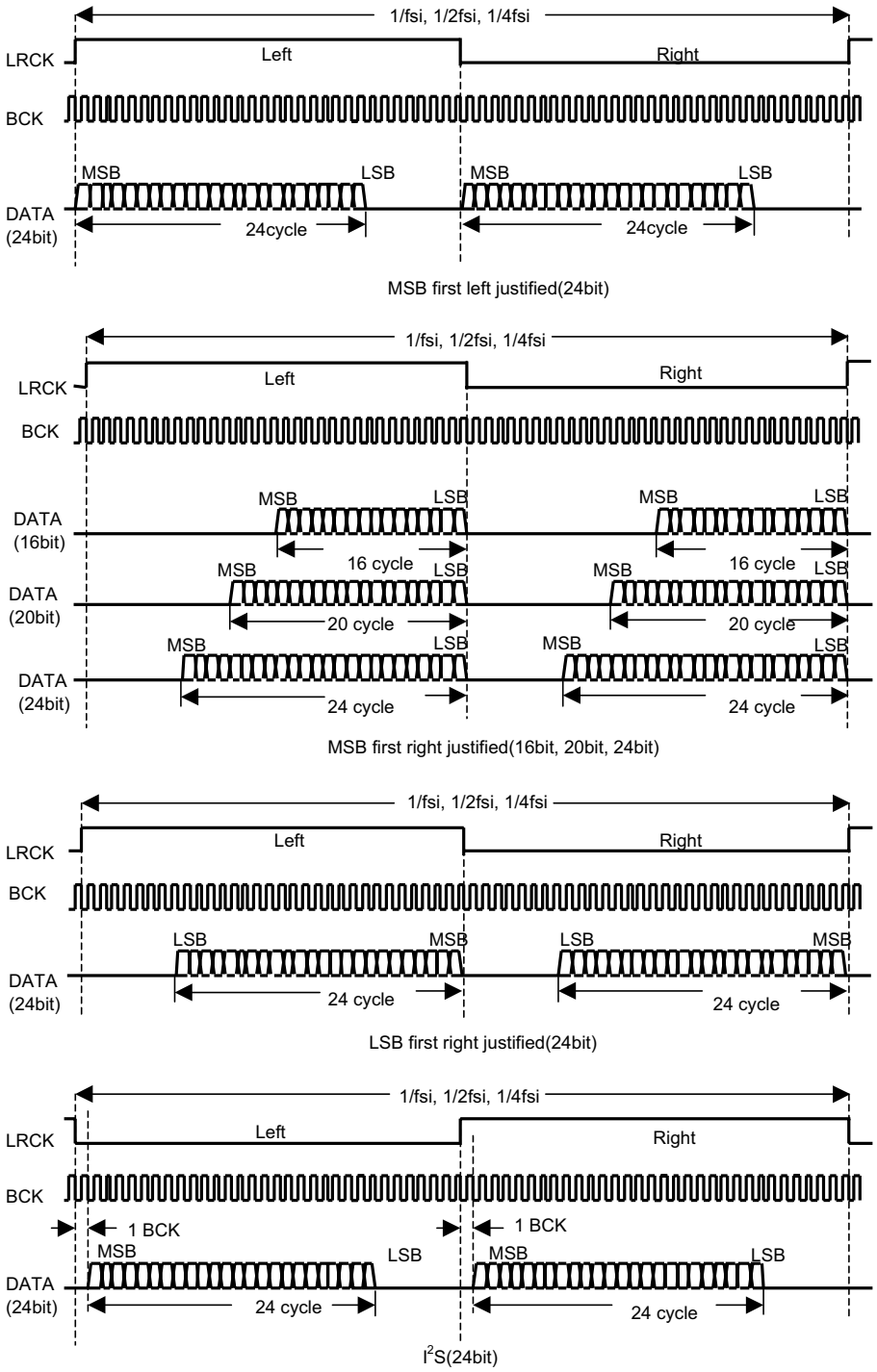
Input data length are selectable in the case of "MSB First Right Justified"

(Serial Control "System1 Mode, bit5, 6").

and Input Signal Sampling Rate(1/2/4fsi) are set by Serial Control,"System1 Mode, bit7,8"

Input formats are shown in following figures.

- Input Formats of **DATA, BCK**, and **LRCK**



5.4. EXBCK, EXWCK, EXDATAL, EXDATAR, EXIOSEL 62 63 60 61 59

When "input signal mode" is "external 8fs data mode", regardless of a setup of **EXIOSEL** pin, the data of 8fs rate are inputted from **EXDATAL**, **EXDATAR** pins.

By setup of serial control "System1 mode:bit21", Primary Side Synchronous Input or Secondary Side Synchronous Input can be selected.

In case an external 8fs data input is secondary side synchronous , the data is inputted to Gain Control Block.

In case an external 8fs data input is primary side synchronous , the data is inputted to Sampling Rate Converter Block.

When "input signal mode" is except a "external 8fs data mode", the output data of sampling rate converter are outputted from **EXDATAL,EXDATAR** pins setting up EXIOSEL pin into "H".

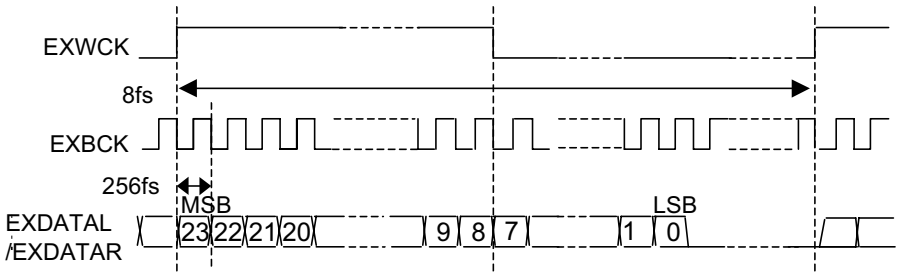
When "input signal mode" is except a "external 8fs data mode", **EXBCK, EXWCK, EXDATAL, EXDATAR** pins serve as input terminals by setting up **EXIOSEL** pin into "L" .

Therefore, when not using "external 8fs data mode", **EXIOSEL** can be set to "L" and other four pins (**EXBCK, EXWCK, EXDATAL, EXDATAR**) can be fixed to "L" or "H".

EXDATAL,EXDATAR,EXBCK, and **EXWCK** pin's input/output format is following figure.

Input Signal Mode	EXIOSEL pin	EXMODE Flag	EXWCK,EXBCK,EXDATAL,EXDATAR Input / Output
"External 8fs Mode" (MODE1,2=L,H)	X	L	Secondary Side Synchronous 8fs Data Input (24 bit effective)
		H	Primary Side Synchronous 8fs Data Input (Upper 20bit effective)
Except "External 8fs Mode" (Except MODE1,2=L,H)	L	X	Input ("L" or "H" fixed)
	H		Internal Sampling Rate Converter Output

- **EXDATAL**, **EXDATAR**, **EXBCK**, and **EXWCK** input/output format



MSB first left justified (24bit)

5.5. DSDL, DSDR, DSD128Fs, DSD64Fs, DSDCKSEL1, DSDCKSEL2, DSDCKIO 50 49 47 48 51 52 53

When "input signal mode" is "SACD-fsi Mode" or "SACD-fso Mode", the data is inputted to **DSDL,DSDR** pins.

Under `SACD-fsi ` mode, the clock of a Down Sampling Filter is given from a primary side, and down sampled data are inputted into the Sampling Rate Converter block.

Under `SACD-fso ` mode, the clock of a Down Sampling Filter is given from a *secondary side, and down sampled data a inputted into the Gain Control block.

The states of **DSDCKSEL1,DSDCKDEL2** pins select 4 "SACD timing mode".

DSDCKIO pin select input or output pin-type of **DSD128Fs/DSD64Fs** clock for data fetch.

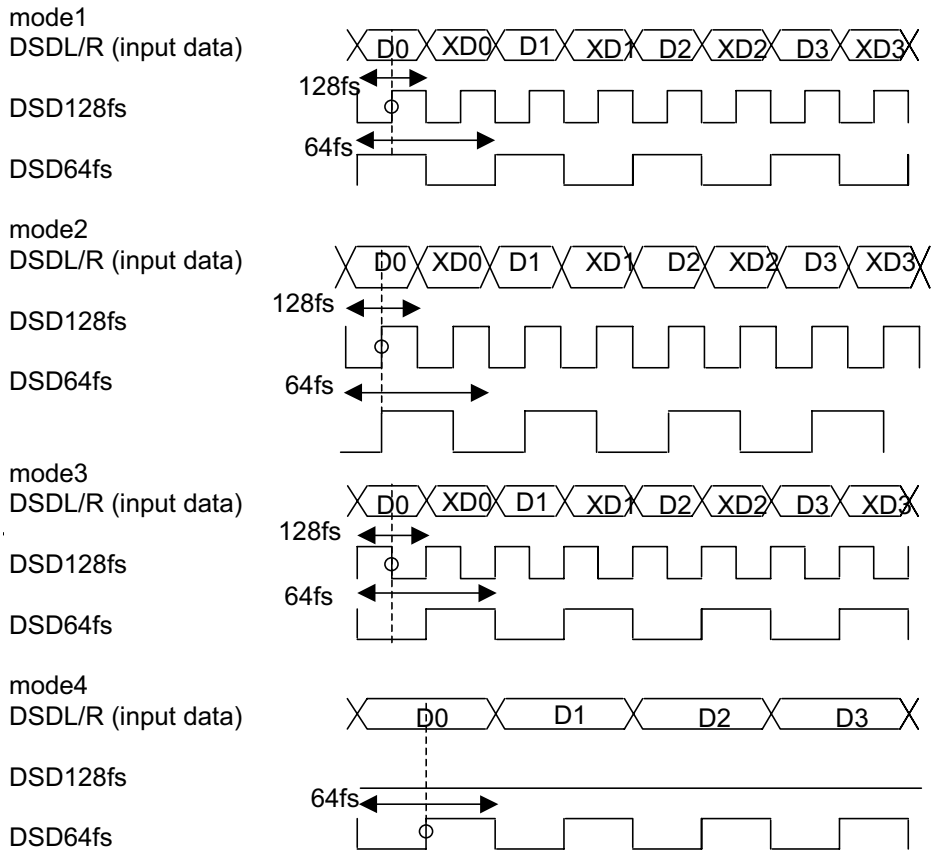
The relations of **DSDCKSEL1** and **DSDCKSEL2** pins and SACD input format mode setting are following figures.

DSDCKSEL1	DSDCKSEL2	SACD timing mode
L	L	mode1
L	H	mode2
H	L	mode3
H	H	mode4

Setting of **DSDCKIO** is following table.

DSDCKIO	Selection of DSD64fs and DSD128fs I/O
L	Input mode
H	Output mode

- SACD Input Format



* D0:Positive phase data, XD0:Negative phase data (reversal)
Positive phase data are fetched at the timing of "O" marks in upper figure.

5.6. MCKCEL, XfsoIN, XfsoOUT 32 28 77

XfsoIN pin is secondary master clock input.

The state of **MCKSEL** pin selects secondary master clock.

MCKSEL	XfsoIN
L	1024fso
H	512fso

XfsoOUT pin is buffered-output from **XfsoIN** pin's input clock.

5.7. XfsiIN 64

XfsiIN pin is primary master clock input.

Frequency of primary master clock must be selected by the serial control "System2 mode:bit3".

bit3(IMCKSEL)	XfsiIN
H	512fsi
L	256fsi

- The relations between input signal sampling rate and master clock frequency.

Input sampling rate	Primary clock 512fsi/256fsi[Hz]	Secondary clock 1024fso/512fso[Hz]
1fsi: 32k / 2fsi: 64k / 4fsi: 128k	16.384M/8.192M	32.768M/16.384M
1fsi: 44.1k / 2fsi: 88.2k / 4fsi: 176.4k	22.579M/11.290M	
1fsi: 48k / 2fsi: 96k / 4fsi: 192k	24.576M/12.288M	49.152M/24.576M

Input signal and primary clock are related to synchronization. The primary clock frequency are 512 or 256 times as much as the input signal fsi (32k, 44.1k and 48k.)

The primary and secondary clock are related to independence. (asynchronization)

At 1024fso setting, secondary clock= frequency range from 32.768MHz to 49.152MHz.
At 512fso setting, secondary clock = frequency range from 16.384MHz to 24.576MHz.

5.8. CKCTL1, CKCTL2, CKOUT1, CKOUT2, CKOUT3 56 57 65 66 67

CKOUT1, CKOUT2, and **CKOUT3** pins are divided-clock output from secondary clock.

At power on, these frequency is free-running.

The states of **CKCTL1** and **CKCTL2** pins selects clock frequency of **CKOUT1**,**CKOUT2,**and **CKOUT3** pins.

The setting table of **CKCTL1** and **CKCTL2** pins is shown below.

CKCTL1	CKCTL2	CKOUT1	CKOUT2	CKOUT3
L	L	L	L	L
L	H	256Fso	16Fso	8Fso
H	L	512Fso	256Fso	16Fso
H	H	512Fso	256Fso	8Fso

5.9. FsoCKO 73

FsoCKO is clock output pin of 1fso frequency. The output is divided-clock of **XfsoIN**, and frequency is free-running

at power on. **FsoCKO** pin's clock is utilized for a synchronization in case that have used plural M65818AFP,take a synchronization between M65818AFP and other external devices.

Detail explanation is shown in next paragraph, "**SYNC**".

5.10. SYNC, FsoI, FsiI, SFLAG 42 74 46 72

M65818AFP synchronizes in clock input from the external source devices. So it makes synchronized operation between source devices or another M65818AFP (in case of Multi channel Operation)

The clock which can be set as the object of an synchronization is a clock of **FsoI** (1fso), **FsiI** (1fsi), **LRCK** (1/2/4 fsi), and **EXWCK** (8fs). The object clock changes by input signal mode setting.

These relations are shown in following table.

M65818AFP detects rise edge of these synchronized clock in normal operation, and the M65818AFP does operation of resynchronization in case that the cycle has changed.

In addition, the M65818AFP re-synchronizes for a synchronized clock, in case that M65818AFP detects SYNC pin's rises edge, too.

This SYNC function exists also in serial control "System2 mode:bit6" under the same name.

While re-synchronizing, SFLAG pin outputs "H" and data is muted inside.

		`Synchronization detection` clock	
Input Signal Mode		**Primary Side**	**Secondary Side**
Normal		LRCK	FsoI
External 8fs Data	Primary Side Synchronization	EXWCK *	FsoI
	Secondary Side Synchronization		FsoI
SACD-fsi		FsiI	FsoI
SACD-fso			FsoI

* Internal 8 dividing clock

In the case of using Multiplex(for multi channel application) and Single (for 2ch application) , detail explanation is shown according to each "signal input mode" below.

- Normal Mode

<Multiplex use>

The primary side: It synchronizes with **LRCK**. All ICs synchronize with an input device by connecting common **LRCK**.
The Secondary side: It synchronizes with FsoCKO of Master IC. One of M65818AFP becomes a master IC, and the synchronization between ICs is carried out by FsoCKO of Master IC.
FsoCKO pin outputted from this master IC is entered each FsoI pins of master and slave ICs.

<Single use>

The primary side: It synchronizes with **LRCK**. Therefore M65818AFP synchronizes with source devices.
The secondary side: there is no need for external devices and other ICs to synchronize, therefore FsoCKO is connected to FsoI, In other way, By setting secondary side asynchronous detection to "disable" with "ASYNCEN2" flag(Serial Control,System2 mode,bit8), FsoI can also be considered as fixation.

In this mode, M65818AFP always perform synchronous detection between **LRCK** pin's clock in primary side.

Therefore with regardless to a setup by the serial control "System1 mode:bit16(ASYNCEN1)", the synchronous detection perform as ` forced-enable`.

- External 8fs Data Mode (The case of primary side synchronization)

<Multiplex use>

The primary side: M65818AFP synchronizes with **EXWCK** (internal 8 dividing clock). All ICs synchronize with an input device by connecting common **EXWCK**.
The secondary side: M65818AFP synchronizes with FsoCKO of Master IC. One of M65818AFP becomes a master IC, and the synchronization between ICs is carried out by FsoCKO of Master IC.
FsoCKO pin outputted from this master IC is entered each FsoI pins of master and slave ICs.

<Single use>

The primary side: M65818AFP synchronizes with **EXWCK** (internal 8 dividing clock).
Thereby it synchronize with an input device.
The secondary side: there is no need for external devices and other ICs to synchronize, therefore FsoCKO is connected to FsoI, In other way,
By setting secondary side asynchronous detection to "disable" with "ASYNCEN2" flag(Serial Control,System2 mode,bit8), FsoI can also be considered as fixation.
In this mode, M65818AFP always perform synchronous detection between **EXWCK** pin's clock in primary side.
Therefore with regardless to a setup by the serial control "System1 mode:bit16(ASYNCEN1)", the synchronous detection perform as ` forced-enable`.

- External 8fs Data Mode (The case of secondary side synchronization)

<Multiplex use and Single use> (common)

The primary side: Synchronous operation does not carry out since internal sampling rate converter is not used.
In this mode, asynchronous detection by the primary side is set to disable by force.
Therefore with regardless to a setup by the serial control "System1 mode:bit16(ASYNCEN1)", the synchronous detection perform as ` forced-disable`.
The Secondary Side: M65818AFP synchronizes with **FsoCKO** of Master IC (in single use, it is own IC).
One of the M65818AFP becomes a master, and the synchronization between ICs is carried out by FsoCKO of Master IC.FsoCKO pin outputted from this master IC is entered each FsoI pins of master and slave ICs.
Moreover, the rise edge of **FsoCKO** sent from M65818AFP and the rise edge of **EXWCK** (8fs) which comes from the external device need to be with a synchronous phase.

- SACD-fsi Mode

<Multiplex use>

The primary side: M65818AFP synchronizes with **FsiI** inputted in common to each IC. And primary side synchronous **DSD128Fs/DSD64Fs** are used as a clock in common to all ICs.
Thus, **DSD128 Fs/DSD64Fs** in common to all ICs is inputted (all IC DSDCKIO=L) or the **DSD128 Fs/DSD64Fs** output (**DSDCKIO**="H") generated by dividing of the primary side master clock within Master IC is inputted Into the **DSD128 Fs/DSD64Fs** (**DSDCKIO**="L") of other slaves IC. The synchronous operation of the SACD input in the case of multi is possible by doing in this way.
The secondary side: M65818AFP synchronizes with FsoCKO of Master IC. One of M65818AFP becomes a master IC, and the synchronization between ICs is carried out by FsoCKO of Master IC.
FsoCKO pin outputted from this master IC is entered each FsoI pins of master and slave ICs.

<Single use>

The primary side: Input to **FsiI** pin or set **FsiI** as fixed by setting primary side asynchronous detection to disable by serial control "System1 mode:bit16 (ASYNCEN1)".
The secondary side: there is no need for external devices and other ICs to synchronize, therefore FsoCKO is connected to FsoI, In other way, By setting secondary side asynchronous detection to "disable" with "ASYNCEN2" flag(Serial Control,System2 mode,bit8), FsoI can also be considered as fixation.

- SACD-fso Mode

<Multiplex use>

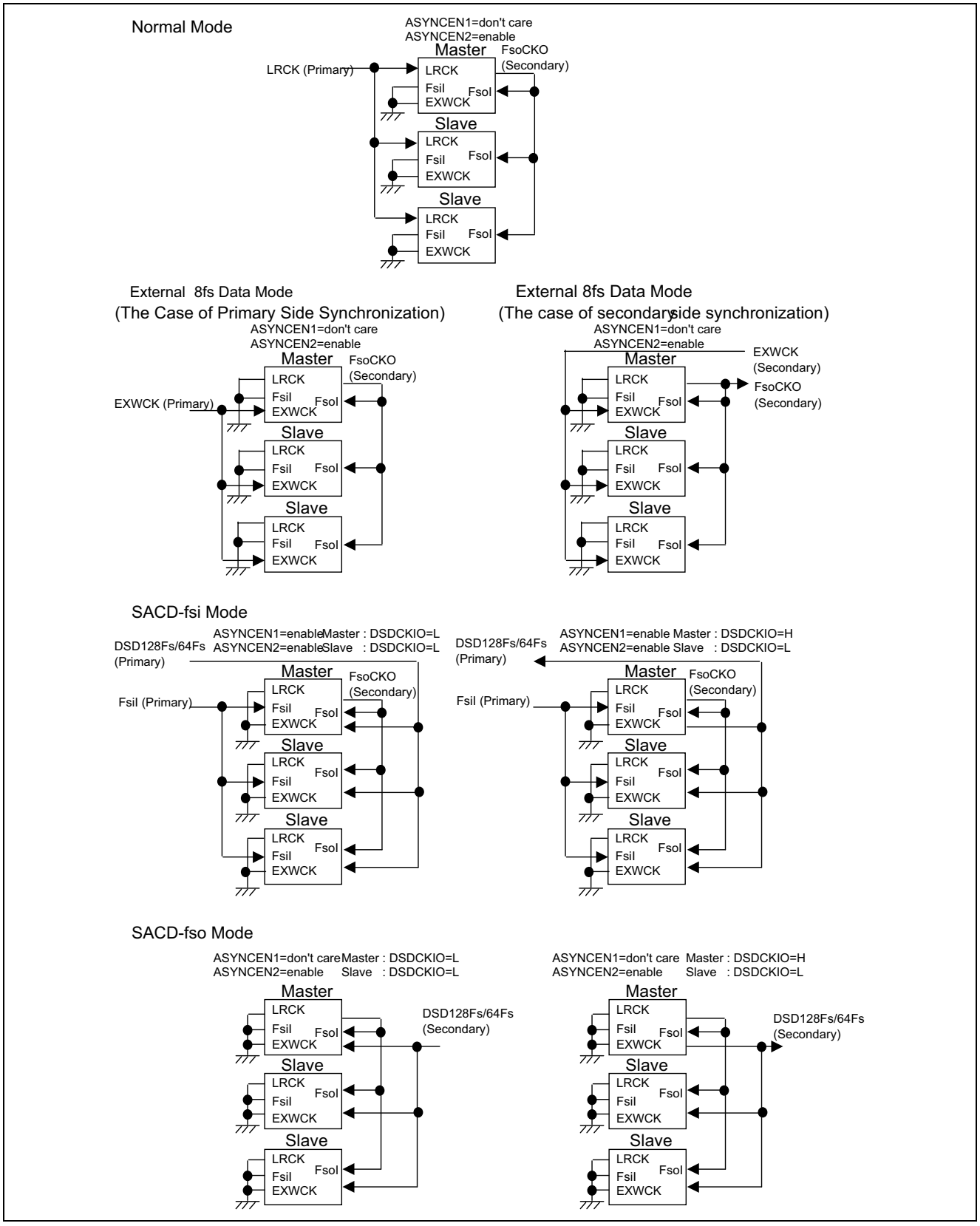
The primary side: Synchronous operation does not carry out since internal sampling rate converter is not used.
In this mode, asynchronous detection by the primary side is set to disable by force.
Therefore with regardless to a setup by the serial control "System1 mode:bit16(ASYNCEN1)", the synchronous detection perform as ` forced-disable`.
The secondary side: M65818AFP synchronizes with FsoCKO of Master IC. One of M65818AFP becomes a master IC, and the synchronization between ICs is carried out by FsoCKO of Master IC.
FsoCKO pin outputted from this master IC is entered each FsoI pins of master and slave ICs.
And **DSD128Fs/DSD64Fs** for secondary synchronization are connected as a clock in common to all ICs. Thus, **DSD128 Fs/DSD64Fs** in common to all ICs is inputted (all IC **DSDCKIO**="L") or the **DSD128 Fs/DSD64Fs** output (**DSDCKIO**="H") generated by dividing of the primary side master clock within Master IC is inputted into the **DSD128 Fs/DSD64Fs** (**DSDCKIO**="L") of other slaves IC.
The synchronous operation of the SACD input in the case of multi is possible by doing in this way.

<Single use>

The primary side: Synchronous operation does not carry out since internal sampling rate converter is not used.
In this mode, asynchronous detection by the primary side is set to disable by force.
Therefore with regardless to a setup by the serial control "System1 mode:bit16(ASYNCEN1)", the synchronous detection perform as ` forced-disable`.
The secondary side: there is no need for external devices and other ICs to synchronize, therefore FsoCKO is connected to FsoI, In other way, By setting secondary side asynchronous detection to "disable" with "ASYNCEN2" flag(Serial Control,System2 mode,bit8), FsoI can also be considered as fixation.

The examples of a connection diagram

The case of the multi use (6ch) in each input mode are shown in the following figure.

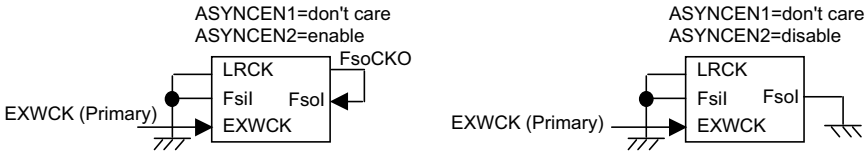


The examples of a connection diagram

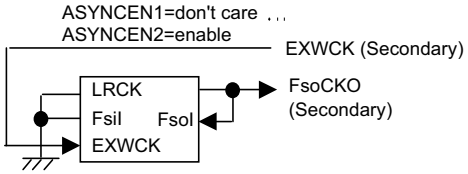
The case of the single use (2ch) in each input mode are shown in the following figure.

Normal Mode

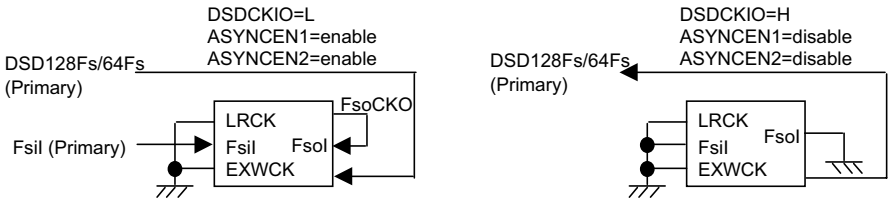
External 8fs Data Mode (The Case of Primary Side Synchronization)



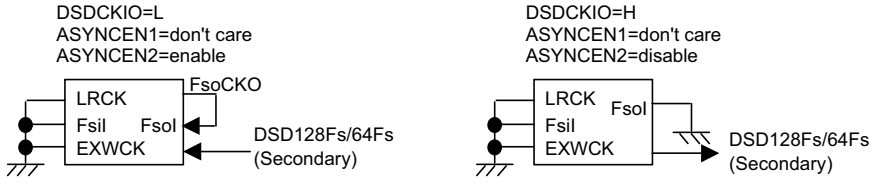
External 8fs Data Mode (The case of secondary side synchronization)



SACD-fsi Mode



SACD-fso Mode



5.11. OFLFLAG 71

OFLFLAG pin is output the 'over flow flag' in the operation. **OFLFLAG** pin outputs "H" level by detection of over flow from Gain Control Block and others.

The "H" level width is over 0.6msec, so detection result is held.

5.12. OUTL1+, OUTL1-, OUTL2+, OUTL2-, OUTR1+, OUTR1-, OUTR2+, OUTR2-

OUTL1+, OUTL1-, OUTL2+, OUTL2-, OUTR1+, OUTR1-, OUTR2+, and OUTR2- pins are pulse output modulated ΔΣ output signal to PWM signal.

These pins are connected to external Power Driver ICs.

PWM Output Form 1, 2, 3 and 4 can be selected by serial control data(System1 mode:bit22,23).

PWM Output Form1 : General Modulation
PWM Output Form2 : Symmetrical Modulation
PWM Output Form3 : Modulation returned with time domain.
(The rise and fall edge of Lch and Rch in a term are reverse.)
PWM Output Form4: Modulation returned with time domain.
(The rise and fall edge of Lch and Rch in a term are same timing.)

In each 4 forms, the operating rate and bit length of PWM Output can be changed following the setting of ΔΣ And the output mute function and the output pins reverse function, can be controlled by the pin setting or serial control.

The PWM output control is shown in the following table.

Item	Operation	Setting Operation
Output Form	Output Form Selection 1,2,3,4	Set up by the serial control system 1 mode bit 22,23 (PWM MODE 0 and 1). (Refer to Chapter 6.2. system 1 mode for details)
Operating Rate and Data Bit Length	Select to 16fso/6bit ,16fso/5bit ,32fso/5bit from operating rate and data bit length of ΔΣ. PWM operation are synchronized by this setting.	Set up by the serial control system 2 mode bit16 and bit17. (Refer to Chapter 6.3. system 2 mode for details.)
Output Muting	Duty 50% Mute	Set **NSPMUTE** pin "L" or set up by serial control System 2 mode bit14 (**NSPMUTE**) "H". (Refer to Chapter 5.13.NSPMUTE pin description and 6.3.system2 mode for details)
	Absolute Zero Mute	Set **PGMUTE** pin "L" or set up by serial control system2 mode bit15(PGMUTE) "H". (Refer to Chapter 5.14.**PGMUTE** pin description and 6.3 system2 mode for details)
Reverse Output Pins Function	Reverse on Lch and Rch of output pins.	Set up by serial control system2 mode bit9 (CHSEL).
	Reverse for **OUTL1**- and **OUTR1**- of output pins.(Output **OUTL1**+ **/R1**+ data to **OUTL1**- **/OUTR1**- data.)	Set up by serial control system1 mode bit124(PWMHP). (Refer to Chapter 6.2. system1 mode for details.)

5.13. NSPMUTE 39

NSPMUTE pin is input to make for PWM output to 50% duty mute.

"L": PWM output 50% duty Mute. '"H": Mute release.

5-14. PGMUTE 40

PGMUTE pin is input to make PWM output to absolute zero mute.

"L": PWM output mute.

The case of System1 mode:bit24,PWMHP = "L"
OUTL1 (+), OUTL2 (+), OUTR1 (+), OUTR2 (+) : "L" fixed
OUTL1 (-), OUTL2 (-), OUTR1 (-), OUTR2 (-) : "H" fixed
The case of System1 mode:bit24,PWMHP = "H"
OUTL1 (+), OUTL2 (+), OUTR1 (+), OUTR2 (+) ,OUTL1(-),OUTR1(-) : "L" fixed
OUTL2 (-), OUTR2 (-) : "H" fixed
"H": MUTE release.

5.15 INIT 41

INIT is the pin for reset to all functions of M65818AFP.

"L" level : (1). Clear of data memory. (2). Initialization of Serial Control.

(3). PWM output Duty 50 %.
"L" period needs more than 5 msec.
"H" level : usual operation.

"L">"H" rise edge: Resynchronization treatment, which is same at SYNC function.

5.16. TEST1, TEST2, TEST3

TEST1,TEST2, and **TEST3** pins are test input for factory shipping test of M65818AFP.

TEST1,TEST2, and **TEST3** pins must be tied to "L" level on usual operation.

5.17. Power Supply and GND

Power supply and GND routes have 5 isolated lines.

(1)**VddL1+, VssL1+, VddL1-, VssL1-, VddL2+, VssL2+, VddL2-, VssL2-, VddR1+, VssR1+, VddR1-, VssR1-, VddR2+, VssR2+, VddR2-, VssR2-, VssL, VddL, VssR, VddR**
These pins are Power supply and GND for PWM output buffer block.
It has a pair of independent Power Supply, and GND to each 8 output pin. Power Supply voltage must be fixed at 5.0V.
(2)**XVdd, XVss** 27 29 30
These pins are Power supply and GND for **XfsoIN** clock input block.
Power Supply voltage must be fixed at 5.0V.
(3)**XOVdd, XOVss** 76 78
These pins are Power supply and GND for **XfsoOUT** clock output block.
Power Supply voltage must be fixed at 5.0V.
(4)**DVdd, DVss** 75 69
These pins are Power supply and GND for digital block and fixed input/output
buffer only for 3.3V (32,70-74 pins). Power Supply voltage must be fixed at 3.3V

(5)**BFVdd, BFVss** 58 68

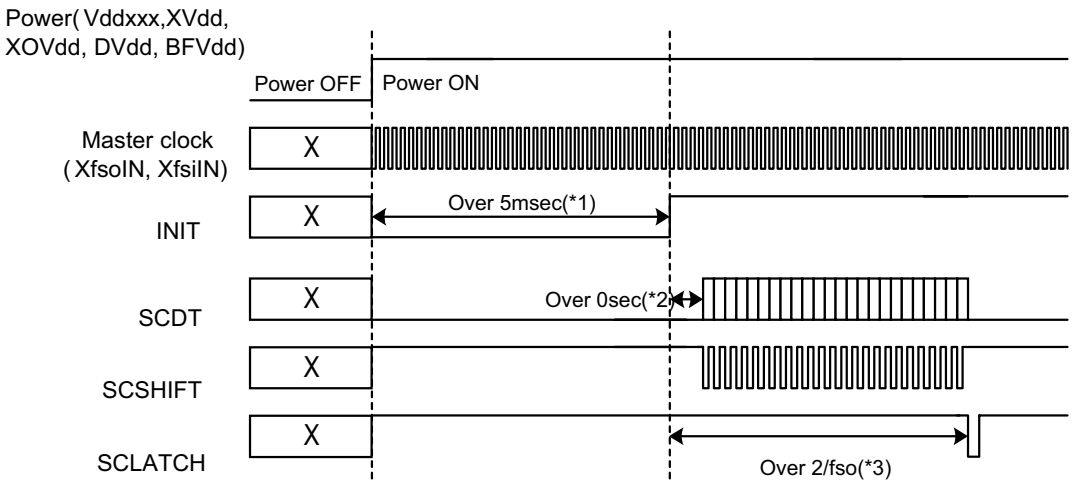
These pins are Power supply and GND for input/output buffer (3.3V/5V). In a case that **BFVdd** pin is applied at 5.0V, input/output voltage level of 34-67pins becomes 5.0V signal level. In another case that **BFVdd** pin is supplied at 3.3V, input/output pins (34-67 pins) becomes 3.3V signal level.

5.18. Power sequences

System power-on sequencing

* Refer to following figure.

System power-on sequencing * Refer to following figure.



*1 After a power supply and Master clock become to stable, **INIT** pin must be "L" over 5 msec.
*2 Data transfer is possible right after **INIT** release.
*3 Until **SCLATCH** is operated, a period over 2/fso (fso=48kHz, over 42usec) is necessary after **INIT** release.

6. Serial Control

6.1. Gain Control Mode

No setting bits means "Don't care".

bit	Flag Name	Functional Explanation	H	L	INIT
1	MODE1	Mode Setting 1		"L" fixed	—
2	MODE2	Mode Setting 2		"L" fixed	—
3	TEST1	Test Mode 1		"L" fixed	L
4	TEST2	Test Mode 2		"L" fixed	L
5	NSLMT1	Output Limit 1	Refer to Table 6-1-2.		L
6	NSLMT2	Output Limit 1			L
7	GCONT1	Channel selection for Gain Control Block 1	L / R independence	L/R common	L
8	GCONT2	Channel selection for Gain Control Block 2	Lch	Rch	L
9					—
10					—
11					—
12	GAIN0	Gain Data Index (MSB)			H
13	GAIN1	Gain Data Index			L
14	GAIN2	Gain Data Index			L
15	GAIN3	Gain Data Index			L
16	GAIN4	Gain Data Index (LSB)			L
17	GAIN5	Gain Data Mantissa (MSB)			H
18	GAIN6	Gain Data Mantissa			L
19	GAIN7	Gain Data Mantissa			L
20	GAIN8	Gain Data Mantissa			L
21	GAIN9	Gain Data Mantissa			L
22	GAIN10	Gain Data Mantissa			L
23	GAIN11	Gain Data Mantissa			L
24	GAIN12	Gain Data Mantissa (LSB)			L

- Output Limit (bit5,bit6:NSLMT1 ,NSLMT2)

The M65818AFP has Over Flow Limit function which detects by input signal level and limit gain control.

Limit value is set by Gain Control Mode :bit5,bit6 ”NSLMT1, NSLMT2” and System2 Mode:bit17"NSOBIT".

The limit value setting of Gain control block and PWM output.

Table (6-1-1a). Limit Value [In the case of 6bit mode, System2 mode:bit17(NSOBIT)="L"]

DSLMT1	DSLMT2	Gain Block	PWM Output (Limit Value from DS Block)
L	L	±0.9375	63 values (±31)
H	L	±0.90625	61 values (±30)
L	H	±0.875	59 values (±29)
H	H	±0.84375	57 values (±28)

Table (6-1-1b). Limit Value [In the case of 5bit mode System2 mode:bit17(NSOBIT)="H"]

DSLMT1	DSLMT2	Limit Value of Gain	PWM Output Value (Limit Value from ΔΣ Block)
L	L	±0.90625	31 values (±15)
H	L	±0.875	31 values (±15)
L	H	±0.84375	29 values (±14)
H	H	±0.8125	29 values (±14)

- Channel Selection for Gain Control Block (bit7,bit8:GCONT1 ,GCONT2)

These bit selection enable to control gain data "L/R common" or "L/R independence".

GCONT1 :"L"…L/Rch common, "H"…L/Rch independence.
GCONT2 :"L"…Rch only, "H"…Lch only.
Bit8 is available only the case of `bit7 = "H"`.

- The index and Mantissa part of Gain Data. (bit12 -bit24,: GAIN0 -GAIN12)

The Gain value is set from bit12 to bit24.

Index part: bit12 (MSB) to bit16(LSB)
Mantissa part: bit17 (MSB) to bit24 (LSB)

The Gain Data is assigned 13bits, composed of Index part 5bits and of Mantissa part 8bits,

The range of Index parts is following statements.

Index part: 10100b(16.0) to 10000b(1.0) to 00000b(2^{-16})

The range of mantissa part is following as statement.

Index part; 10100b to 00001b: Mantissa part; 11111111b to 10000000b (128 step/1 Index).
Index part;00000b: Mantissa part; 11111111b to00000000b (256 step).

Initial value: Index part: 10000b Mantissa part:10000000b
infinity zero: Index part: 00000b Mantissa part:00000000b

Notice of GAIN value Setting continuously

In the case of GAIN value Setting continuously, for example of Setting L/Rch independently, please take the interval time (pulse interval time of SCLATCH signal) more than 1/fso.For example, in the case of fso=48kHz, please take the interval time more than 21μsec.

- The Gain Data and Audio Output Level.

Gain data consists of 13bits (Index part; 5bit, Mantissa part; 8bit).

e.g. 10000b(1.0)/10000000b(0.5) means 0.5(0dB).

Table (6-1-2). The Gain Data and Output Level

Gain Data	Polarity	Absolute Output Value	Output Level
10100/11111111 (b)	+	15.9375	+30.069dB
to		to	to
10001/10000000 (b)		1.0	+6.021dB
to		to	to
10000/10000000 (b)		0.5	0dB
01111/11111111 (b)		0.498046875	-0.0340dB
to		to	to
00000/10000000 (b)		0.5^{*-16}	-96.330dB
to		to	to
00000/00000001 (b)		0.00390625^{*2-16}	-138.474dB
00000/00000000 (b)		infinity zero	-∞

- Calculation method of Gain value.

The way to calculation of Gain value from Gain Data is following equation.

$$\text{Gain value} = 20\log\left[\, 2^{\text{<Index data (decimal value)-16>}} \times \frac{\text{Mantissa data (decimal value)}}{128} \,\right] \text{dB}$$

- Soft Mute.

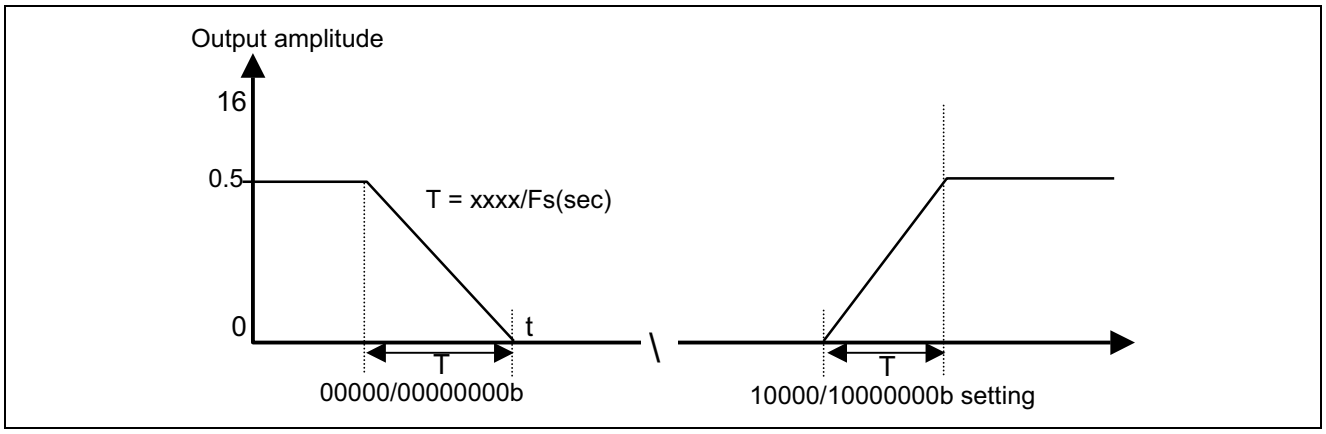
The Soft Mute function is executed by setting of Gain Data as 00000/00000000b

("/" :means dividing point between index part and mantissa part).

The release from Soft Mute function must be executed by setting the gain data before soft mute.

The Soft Mute function and release from there don't have linear curve but

have characteristics of approximate exponential curve.



- Operating time of Soft Mute

Total steps from Maximum value(10100b/11111111b) to Minimum value(00000b/00000000b)

(128steps/1 index) × (20index (10100b-10000b)) +256steps = 2816steps.

The transition term of up and down depend on 2fso clock.

Therefore, in case of fso=48kHz, T=1/2fso=10.416µsec/step, transition term are following.

From Maximum value (10100b/11111111b) to Minimum value (00000b/00000000b) : 2816T=29.333msec.
From 0dB value (10000b/10000000b) to Minimum value (00000b/0000000b) : 2304T=24msec
6dB transition term (when over 00000b/10000000b (=-96dB) value) : 128T=1.333msec.

- Soft Attenuate.

Transition from older Gain Attenuation to newer Gain Attenuation always operates with Soft Mute function.

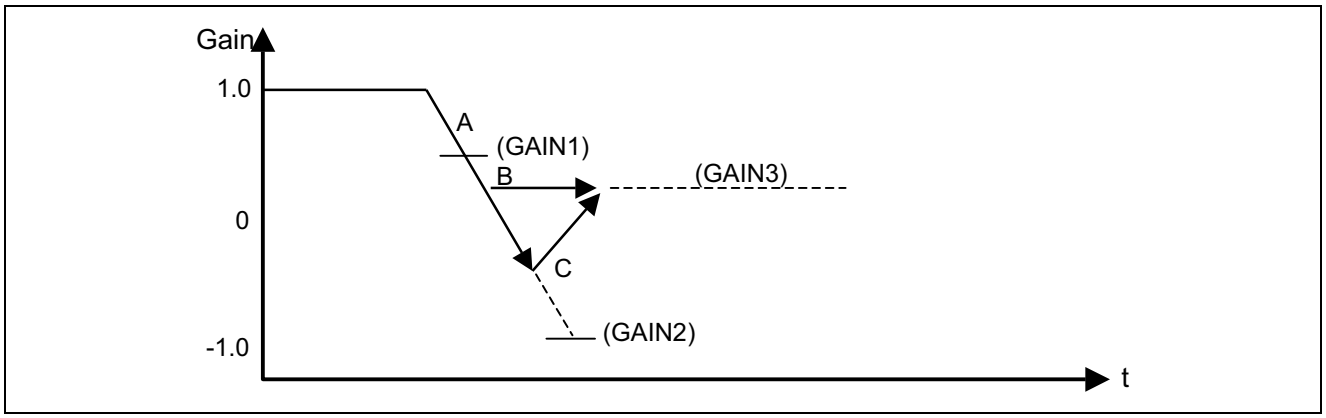
For example, in case of Gain1 > Gain3 > Gain2, transition process is shown below.

At first, GAIN1 is operated, then second, GAIN2 is operated.

In case that GAIN2 is operated faster than GAIN1 of transition completion (refer to "A" situation in figure)

GAIN1 is ignored and data approaches at GAIN2.

Further, GAIN3 is operated faster than GAIN2 of transition completion(Refer to "B" or "C" situation in figure), GAIN2 is ignored and data approaches at GAIN3.



6.2. System1 Mode

bit	Flag Name	Functional Explanation	H	L	INIT
1	MODE1	Mode Setting 1		"L" fixed	—
2	MODE2	Mode Setting 2	"H" fixed		—
3	IFMT0	Input Format Selection	Refer to Table 6-2-1.		L
4	IFMT1				L
5	IBIT0	Setting for Input Word Length	Refer to Table 6-2-2.		L
6	IBIT1				L
7	ISF0	Input Sampling Rate Selection	Refer to Table 6-2-3.		L
8	ISF1				L
9	EMPFS1	Fs selection for De-emphasis Filter	Refer to Table 6-2-4.		L
10	EMPFS2				L
11	DF1IMUTE	Zero Mute of DATA input	Active	Non-active	L
12	DF2IMUTE	Zero Mute at sampling rate converter input	Active	Non-active	—
13			don't care		—
14			don't care		—
15			don't care		—
16	ASYNCEN1	synchronous Detection Flag for Primary Side	enable	disable	L
17			don't care		
18			don't care		
19			don't care		
20	ASYNC1MODE	Select process under asynchronization in primary side	Zero Mute	PWM:duty 50%	L
21	EXMODE	Mode select of external 8fs data input	Sync. by primary side	Sync. by secondary side	L
22	PWMMODE0	Selection of Output PWM Form	Refer to Table 6-2-5		L
23	PWMMODE1				L
24	PWMHP	Reverse Phase of OUTL1-/R1-	Active	Non-active	L

Table 6-2-1 Input Format

bit	Flag Name	MSB First Left Justified	MSB First Right Justified	LSB First Right Justified	I^2S
3	IFMT0	L	H	L	H
4	IFMT1	L	L	H	H

Table 6-2-2 Setting for Input Data Word Length

bit	Flag Name	16bit	20bit	24bit	Don't use
5	IBIT0	L	H	L	H
6	IBIT1	L	L	H	H

Table 6-2-3 Input Sampling Rate Selection (fsi: 32k to 48kHz 2fsi: 64k to 96kHz, 4fsi: 128k to 192kHz)

bit	Flag Name	fsi	2fsi	4fsi	Don't use
7	ISF0	L	H	L	H
8	ISF1	L	L	H	H

Table 6-2-4 Fs Selection for De-emphasis filter (De-emphasis is "ON" except for bit9=L and bit10=L)

bit	Flag Name	32.0K	44.1K	48.0K	OFF
9	EMPFS1	H	L	H	L
10	EMPFS2	H	H	L	L

Table 6-2-5 Selection of PWM Output form

bit	Flag Name	PWM Output Form	PWM Output Form	PWM Output Form	PWM Output Form
22	PWMMODE0	L	H	L	H
23	PWMMODE1	L	L	H	H

*Output Form 2 is available only under following conditions.
MCKSEL="L" (Secondary Side Master Clock 1024fso) , Serial Control System2 mode,
bit17(NSOBIT) = "H" (5bit), bit16(NSSPEED) = "L" (16fso).
In case of the setting and release for PWM Output Form 2,
Refer to "The NOTE1 at setting PWM output Form 2" on next page.

- Selection of Input format (bit3,bit4:IFMT0,IFMT1) Refer to Table 6-2-1

Selection of Input format function is available only condition of `Normal` mode.

Otherwise, Selection of Input format function is unavailable under conditions of `External 8fs Input`

and `SACD Input` modes (Interlocked with **MODE1** and **MODE2** pins).

Detail setting of `External 8fs Input` and `SACD` modes are shown in Chapter **5-4** and **5-5**.

- Setting of Input Word Length (bit5,bit6:IBIT0,IBIT1). Refer to Table 6-2-2.

Setting of Input Data Word Length is available only MSB First Right Justified.

- Selection of Input Sampling Rate (bit7,bit8:ISF0,ISF1). Refer to Table 6-2-3.

- Fs Selection for De-emphasis Filter on/off (bit9, bit10 : EMPFS1, EMPFS2). Refer to Table 6-2-4.
  (bit9,bit10): ("L","L")… De-emphasis Filter is "off".
  except ("L","L")… De-emphasis Filter on (Fs setting).

- Zero Mute at data input (bit11: DF1IMUTE).

DF1IMUTE : "L"…Mute release.

"H"…Mute.

The input data from **DATA** pin under normal mode is muted in this setting.

- Zero Mute at Sampling Rate Converter Input (bi12: DF2IMUTE).

DF2IMUTE : "L"…Mute release.

"H"…Mute.

DF2IMUTE is available for sampling rate converter input data.

DF2IMUTE executes zero mute of input data from **DATA** pin under condition of `Normal` mode and

from **DSDL/DSDR** pins under condition of `SACD-fsi ` mode.

- "Enable" of Primary Side Asynchronous Detection Flag (bi16: ASYNCEN1).

Bit16 controls "enable"/"disable" of primary-side-asynchronous-detection-circuit.

ASYNCEN1 : "L"…disable.

"H"…enable.

Under condition of ASYNCEN1 ="L", primary side asynchronous detection is unavailable whether the clock is not inputted to **FsiI** pin, thereby M65818AFP does not operate function under asynchronization, for instance mute operation. However, Primary Side Asynchronous Detection is available only condition of `SACD-Fsi` mode.

- Selection of Muting operation at primary Side Asynchronous Detection (bit20:ASYNC1MODE)

"L" …Duty 50% Mute of PWM output at primary side asynchronous detection.

"H"… Input Zero Mute of the gain control at primary side asynchronous detection.

(PWM Output 50% Mute doesn't be operated in this setting.)

- Selection of Data Input Mode for external 8fs.(bit21: EXMODE)

"L"…A setup in case an external 8fs data input is secondary side synchronous.

(Data is inputted to Gain Control Block)

"H"…A setup in case an external 8fs data input is primary side synchronous.

(Data is inputted to Sampling Rate Converter Block)

- Selection of PWM output form (bit22, 23:PWMMODE 0 and 1) Refer to Table 6-2-5.

The selection of PWM output form 1, 2, 3, and 4 , refer to Chapter 5-12 for the details.

*NOTE1 : At the setting of PWM Output Form2

PWM Output Form2 enable to operate the following conditions.

bit17 NSOBIT) "H" (5bit), bit16(NSSPEED)="L"(16 fso)

Only in terminal **MCKSEL**="L" (secondary side master clock 1024 fso)

In the case of setting and release for PWM Output Form2, set both flags as follows.

- Serial Control System1 Mode, bit 22, 23 (PWMMODE0,1)
- Serial Control System2 Mode: bit16 (NSSPEED), bit17 (NSOBIT)

<The case of the setting for PWM output form2>

(1) Set to Serial Control System2 mode : bit17(NSOBIT)="H"
bit16(NSSPEED)="L".
(To be set as MCKSEL="L" in advance is required.)

(2) Serial control System1 mode:bit22, 23(PWMMODE0,1)="H","L"
When a setup of both (1) and (2) is completed, it changes to Form2. When (2) is set up before (1), The term until a setup of (1) holds the last PWM Output Form.

<The case of release for PWM output form2>

(1) Serial control System1 mode:bit22, bit 23 (PWMMODE 0 , 1) is set as the Form to be used.

(2) Serial Control System2 mode:bit17(NSOBIT),bit16(NSSPEED) is set the condition to be used.
When a setup of (1) is completed, PWM Output Form changes. When (2) is set up before (1), a term until a setup of (1) is worked keeps the Form 2 in the state of serial control System2 mode:bit17(NSOBIT) ="H", bit16(NSSPEED) ="L".

*NOTE2; Selection of PWM output form

Pay attention in selection and setting above-mentioned that a noise may occur by internal clock changes when setting of MCKSEL pin is changed and the serial control System2 mode:
bit17 (NSOBIT) and bit16 (NSSPEED).
Since especially **MCKSEL** pin sets up an internal master clock, use with a fixed value recommended.
In changing **MCKSEL**, initialization with **INIT** pin and a re-setup of all the bits by serial control are needed after changing **MCKCEL**.

- Reverse Phase of PWM Output **OUTL1(-) / OUTR1(-)** (bit24:PWMHP)
  "L"…PWM Output **OUTL1(-) / OUTR1(-)** are reverse phase as the PWM output **OUTL1(+) / OUTR1(+)** .
  "H"…PWM Output **OUTL1(-) / OUTR1(-)** are same phase as the PWM output **OUTL1(+) / OUTR1(+)** .
  In this mode, the signal which added **OUTL1(-) / OUTR1(-)** and **OUTL2(-) / R2(-)** by external resistance can be given to LPF / Headphone Amplifier.

6.3. System2 Mode (Secondary side)

bit	Flag Name	Functional Explanation	H	L	INIT
1	MODE1	Mode Setting 1	"H" fixed		—
2	MODE2	Mode Setting 2		"L" fixed	—
3	IMCKSEL	Input Master Clock Selection	512fsi	256fsi	L
4	DSDFCO0	Filter Coefficient of Down Sampling	Refer to Table 6-3-1.		L
5	DSDFCO1				L
6	SYNC	Resynchronization	L->H : Resynchronization.		L
7	XFsoOEN	XfsoOUT pin output "enable"	disable	enable	L
8	ASYNCEN2	Asynchronous Detection Flag for secondary Side	enable	disable	L
9	CHSEL	L / R inversion of PWM output	Active	Non-active	L
10	DRPOL	ΔΣBlock: Rch Input Phase	Negative-phase	Positive-phase	L
11	SRCRST	Sampling Rate Converter Reset	Active	Non-active	L
12			don't care		—
13	GIMUTE	Zero Mute at Gain Control Input Clock	Active	Non-active	L
14	NSPMUTE	Duty 50 percent Mute of PWM Output	Active	Non-active	L
15	PGMUTE	G_MUTE of PWM Output Data	Active	Non-active	L
16	NSSPEED	ΔΣ Block: Operation Speed	32fso	16fso	L
17	NSOBIT	ΔΣ Block: Setting of Output Bit Number	5 bits (31 value)	6 bits (63 value)	L
18	DCDRPOL	ΔΣ Block: Rch Phase of DC dithering	Negative-phase	Positive-phase	L
19	DCDSEL0	ΔΣBlock: DC dithering Selection	Refer to Table 6-3-2		L
20	DSDSEL1				L
21	ACDRPOL	ΔΣ Block: Rch Phase of AC dithering	Negative-phase	Positive-phase	L
22	ACDSEL0	ΔΣ Block: AC dithering selection	Refer to Table 6-3-3		L
23	ACDSEL1				L
24	ACDSEL2				L

Table 6-3-1 Setting of Down Sampling Filter Coefficient

bit	Flag Name	ROM1	ROM2	ROM3	ROM4
4	DSDFCO0	L	H	L	H
5	DSDFCO1	L	L	H	H

Table 6-3-2 DC dithering Selection at ΔΣ Block

bit	Flag Name	Non-dithering	DC dithering 0.1%	DC dithering 0.2%	DC dithering0.4%
19	DCDSEL0	L	H	L	H
20	DCDSEL1	L	L	H	H

Table 6-3-3 AC dithering Selection at ΔΣ Block

bit	Flag Name	Non-dithering	AC dithering A	AC dithering C	AC dithering E
22	ACDSEL0	don't care	L	L	L
23	ACDSEL1	L	H	L	H
24	ACDSEL2	L	L	H	H

Table 6-3-4 Setup Operating Rate & Bit Length of ΔΣ Block

bit	Flag / Pin Name	16fso,6bit	16fso,5bit	16fso,5bit	32fso,5bit
16	NSSPEED	L	L	X	H
17	NSOBIT	L	H	X	H
pin	MCKSEL	L(Secondary Clock1024fso)	L(Secondary Clock1024fso)	L(Secondary Clock512fso)	L(Secondary Clock1024fso)

- Input Master Clock Selection (bit3:IMCKSEL).

"L":256fsi

"H":512fsi ("512fsi" are divided into half "256fsi" and operate as primary master clock.)

- Selection of Down Sampling Filter Coefficient for SACD input (bi4, bit5: DSFCO 0,DSFCO 1).

Refer to Table 6-3-1.

- Resynchronization (bit6: SYNC).

Resynchronization function is same at **SYNC** pin's function. Refer to Operation Explanation, Chapter 5.10.

Resynchronization process starts by **SYNC** rise edge,

therefore SYNC level must be fixed to "L" just before SYNC operation.

- "Enable" of **XfsoOUT** pin Output(bit7: XfsoOEN).

"L": Clock Output (enable), "H": L fixed (disable)

- Flag to "Enable" Asynchronous Detection for Secondary Block (bit8: ASYNCEN2).

ASYNCEN2 : "L"…disable.

"H"…enable.

Under condition of ASYNCEN2="L", secondary side asynchronous detection is in-effective under asynchronous position, whether Fsol Clock is not inputted, there by M65818AFP does not operate function for instance mute operation.

- Reverse Lch/Rch for PWM Output pins(bit9: CHSEL).
  "L": Lch/Rch no reverse, "H": Lch/Rch reverse.

- ΔΣ: Rch Input Phase (bit10: DRPOL).
  "L"…. Same phase ("Through")
  "H"…..This setting makes ΔΣ Rch Input in reverse, further makes PWM block input phase reverse, ultimately phase becomes positive phase (Input pin and Output pin's phase is same).

- Sampling Rate Converter Block Reset (Initialize function) (bit11: SRCRST).
  "L" …..normal operation
  "H" to "L" edge…..Reset (Initialize function)

- Zero Mute of Gain Control Input (bit13: GIMUTE).
  "L"…Mute release, "H"…Mute.

- Duty 50% Mute of PWM Output (bit14: NSPMUTE).
  Fixed PWM duty 50% Mute
  "L"…..Mute release
  "H"….. Mute

This function exists also in a pin by the same name.(This Mute function can be set either NSPMUTE flag or NSPMUTE pin.)

- G-Mute for PWM Output Data (bit15: PGMUTE)
  At G-MUTE flag = H , PGMUTE pin fixes each PWM Output as followings.
  "L"….. Mute release "H"….. Fixed Mute for PWM Output (Fixed value as follows)
  <Serial Control (System1 Mode :bit24) PWMHP="L" >
  OUTL1(+) and OUTR1(+) ="L" , OUTL2(+) and OUTR2(+) = "L"
  OUTL1(-) and OUTR1(-) ="H" , OUTL2(-) and OUTR2(-) = "H"
  <Serial control (system1 mode; bit24) PWMHP="H">
  OUTL1(+) and OUTR1(+) ="L" , OUTL2(+) and OUTR2(+) = "L"
  OUTL1(-) and OUTR1(-) ="L" , OUTL2(-) and OUTR2(-) = "H"
  This function exists also in a pin by the same name.(This Mute function can be set either PGMUTE flag or PGMUTE pin.)

- ΔΣBlock : operating rate (bit16: NSSPEED). Refer to Table 6-3-4.
  "L"…16fso
  "H"…32fso *Enable only MCKSEL="L"(1024fso), NSOBIT="H" only.
  (Except for this condition, Operating rate automatically becomes 16fso.)

- ΔΣ Block : The setting of bit length (bit17: NSOBIT). Refer to Table 6-3-4.
  NSOBIT selects bit length for ΔΣ operation. This is set by force as 5bit at MCKSEL="H".
  "L"…6bit (63 value)
  "H"…5bit (31value)

- ΔΣBlock: DC dithering Rch Phase (bit18: DCDRPOL).
  "L"…Same phase "H"…Reverse phase

- ΔΣ Block: DC dithering Selection (bit19,bit20: DCDSEL0,DCDSEL1). Refer to Table 6-3-2.

- ΔΣBlock: AC dithering Rch Phase (bit21: ACDRPOL).
  "L"…Same phase "H"…Reverse phase

- ΔΣ Block: AC dithering Selection (bit22,bit23,bit24: ACDSEL0,ACDSEL1,ACDSEL2). Refer to Table 6-3-3.

7.1. AC Characteristics Lists.

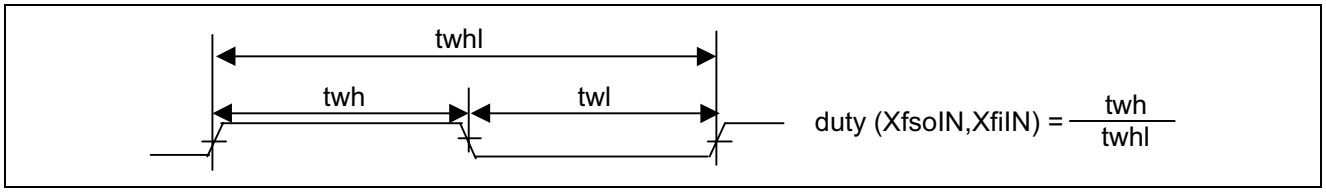
(Ta=25 °C, PWM Vdd=5V, DVdd=3.3V)

AC Characteristics

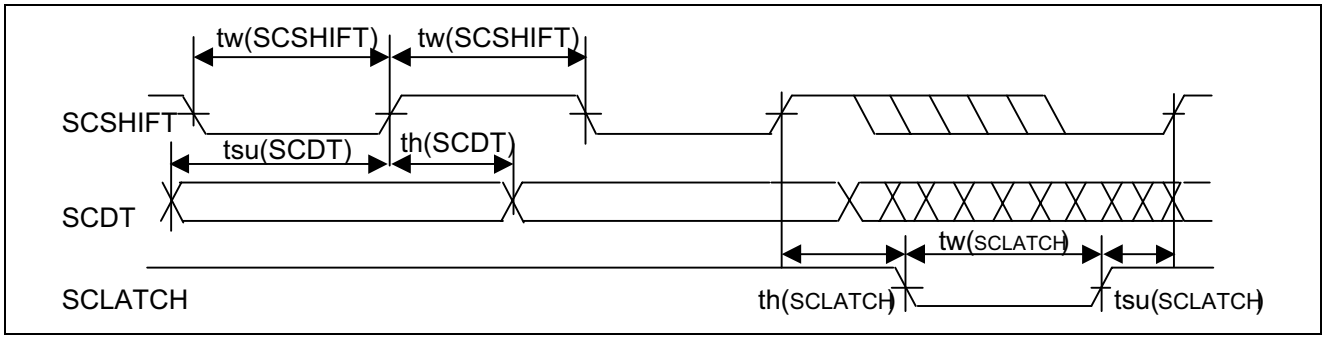
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
XfsoIN duty ratio	duty(XfsoIN)		40	50	60	%
XfsiIN duty ratio	duty(XfsiIN)	512fsi	30	50	70	%
		256fsi	40	50	60	nsec
SCSHIFT pulse time	tw(SCSHIFT)		160			nsec
SCDT setup time	tsu(SCDT)		80			nsec
SCDT hold time	th(SCDT)		80			nsec
SCLATCH pulse width	tw(SCLATCH)		160			nsec
SCLATCH setup time	tsu(SCLATCH)		160			nsec
SCLATCH hold time	th(SCLATCH)		160			nsec
BCK pulse width	tw(BCK)		35			nsec
DATA setup time	tsu(DATA)		20			nsec
DATA hold time	th(DATA)		20			nsec
LRCK setup time	tsu(LRCK)		20			nsec
LRCK hold time	th(LRCK)		20			nsec
EXBCK pulse time	tw(EXBCK)		35			nsec
EXWCK setup time	tsu(EXWCK)		20			nsec
EXWCK hold time	th(EXWCK)		20			nsec
EXDATA L / R setup time	tsu(EXDATA)		20			nsec
EXDATA L / R hold time	th(EXDATA)		20			nsec
EXDATA L / R output delay time	tpd(EXDATA)	Output load capacity 10 [pF]		1.0		nsec
EXWCK output delay time	tpd(EXWCK)	Output load capacity 10 [pF]		1.0		nsec
DSD128fs pulse width	tw(DSDCK128)		70			nsec
DSD64fs pulse width	tw(DSDCK64)		140			nsec
DSD64fs setup time	tsu(DSDCK64)	mode 1, 3	40			nsec
DSD64fs hold time	th(DSDCK64)	mode 1, 3	40			nsec
DSD L / R setup time	tsu(DATA)	mode 1, 2, 3, and 4	40			nsec
DSD L / R hold time	th(DATA)	mode 1, 2, 3, and 4	40			nsec
SYNC pulse width	tw(SYNC)		160			nsec

7.2. AC Characteristics Timing Chart

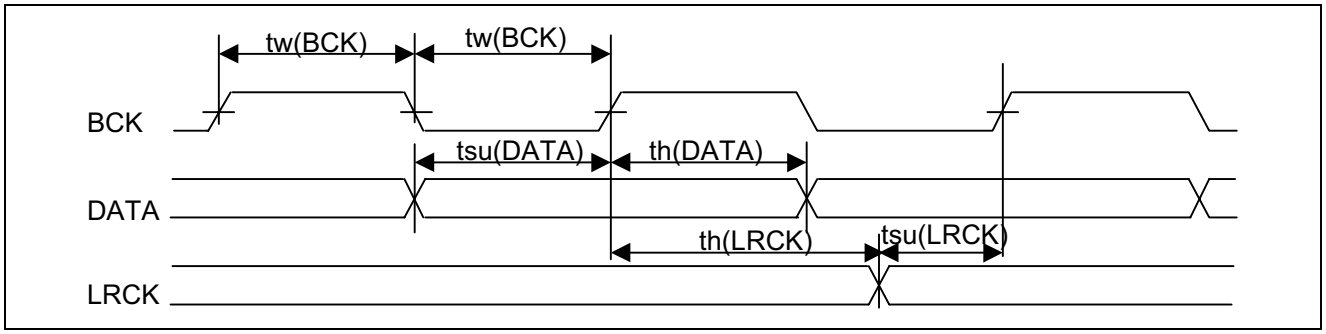
(1) XfsoIN, XfsiIN Duty Ratio



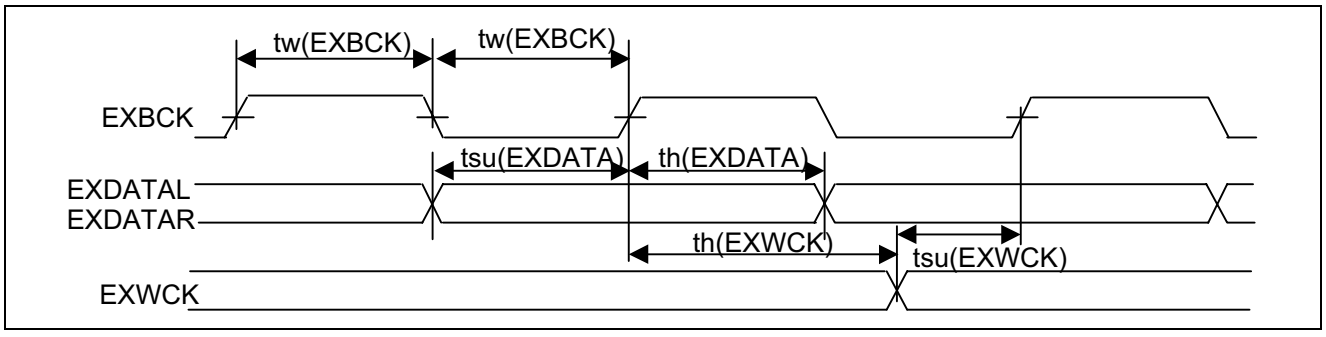
(2) SCSHIFT, SCDT, SCLATCH input timing Chart



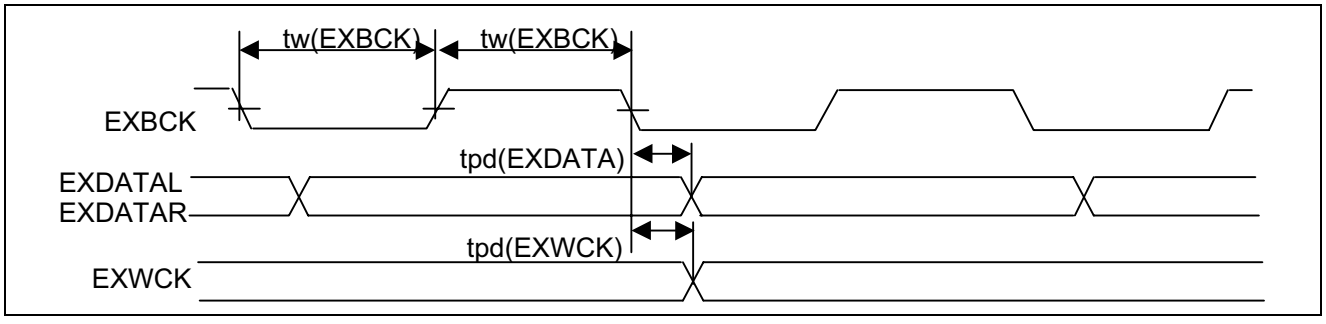
(3) BCK, DATA, and LRCK Input timing Chart



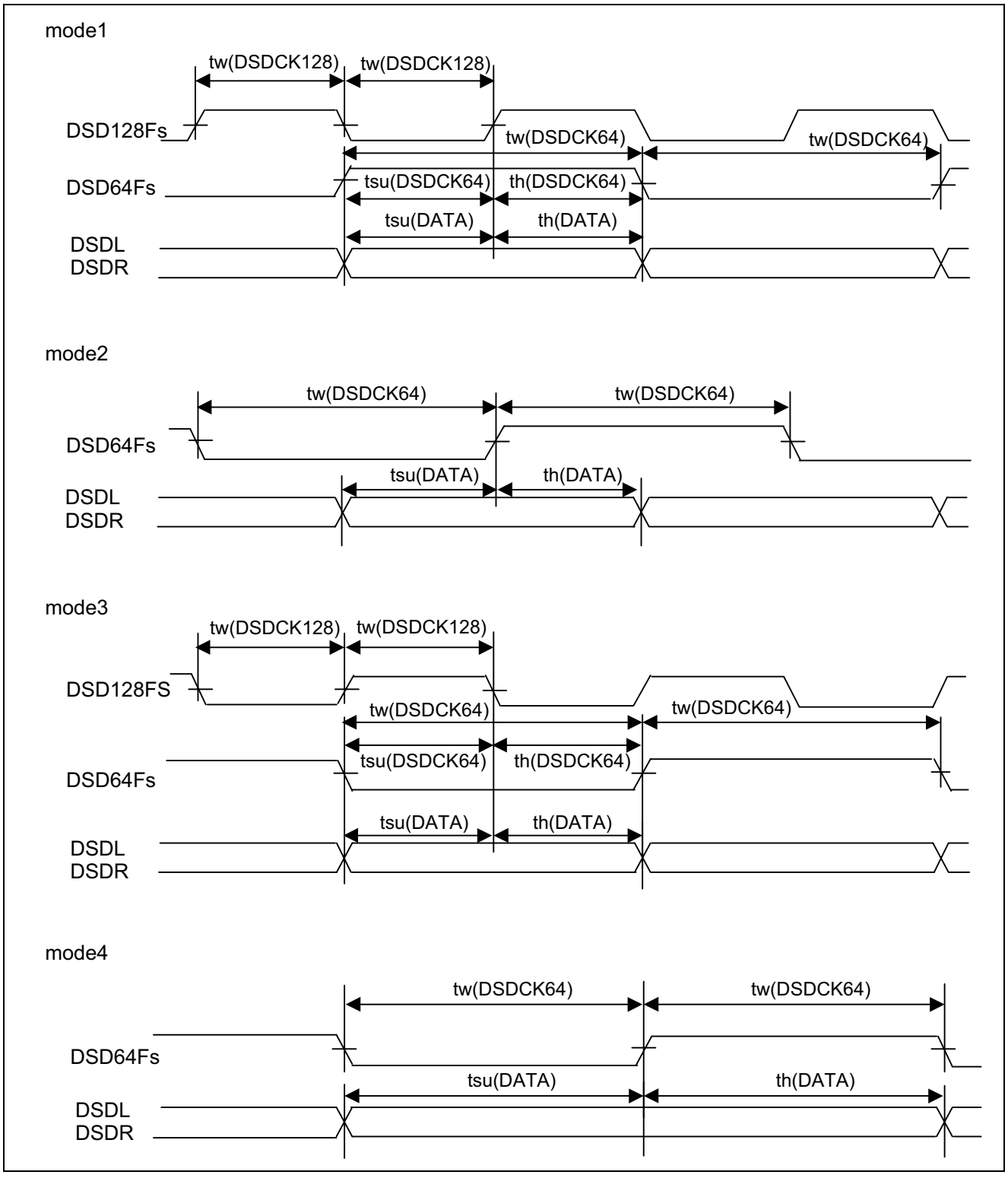
(4) EXBCK, EXDATAL, EXDATAR, EXWCK input timing Chart



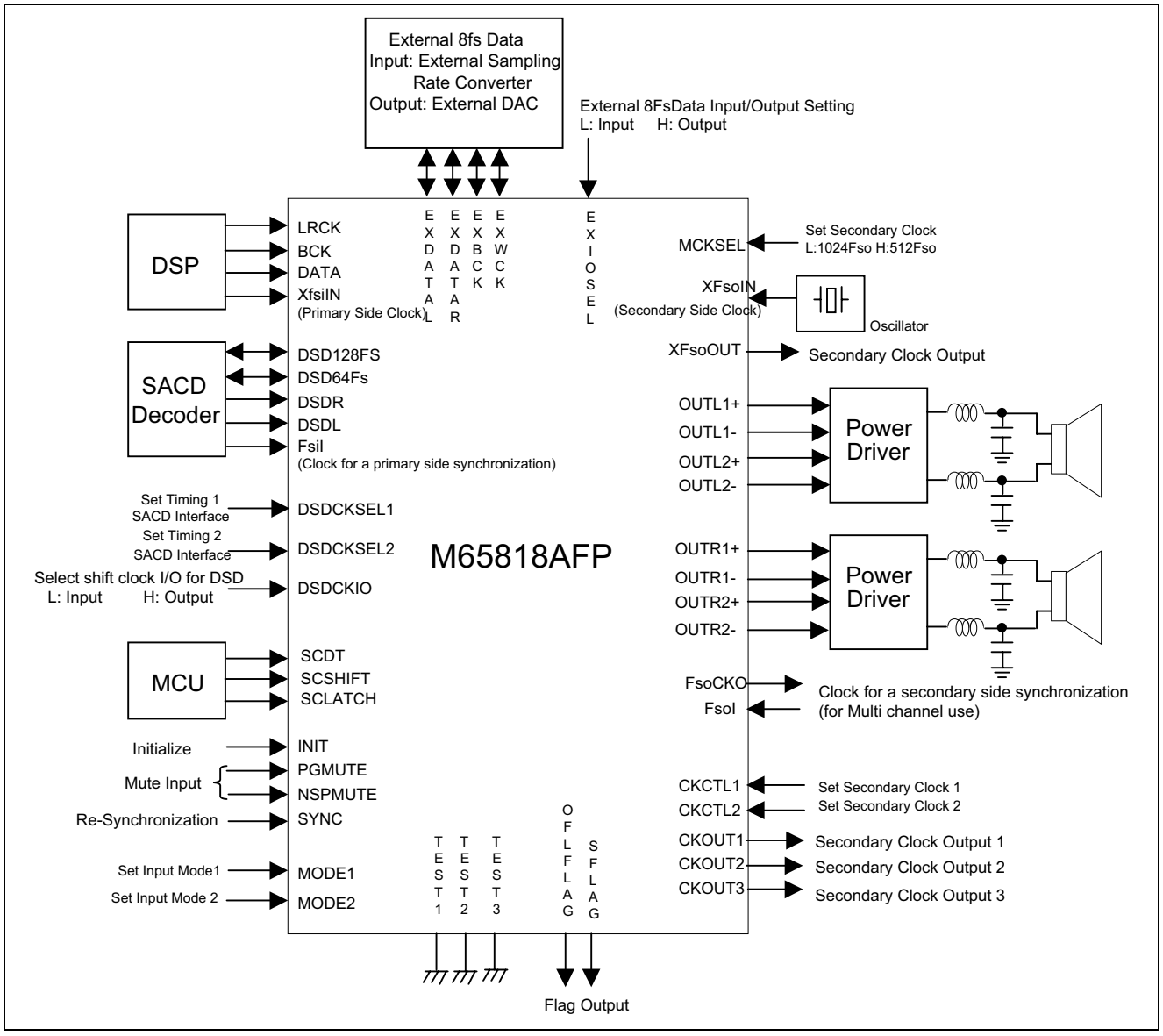
(5) EXBCK, EXDATAL, EXDATAR, EXWCK output timing Chart



(6) DSD64Fs, DSD128Fs, DSDL, DSDR Input Timing Chart



8. Application Example



Package Dimensions

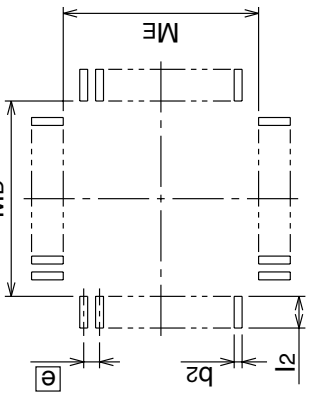
Plastic 80pin 14×20mm body QFP

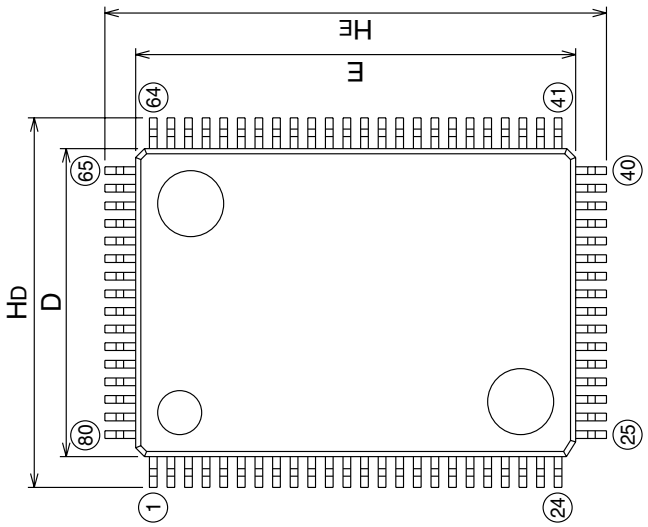
80P6N-A (MMP)

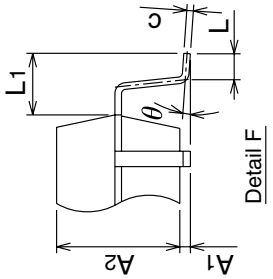
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1420-0.80	—	1.58	Alloy 42

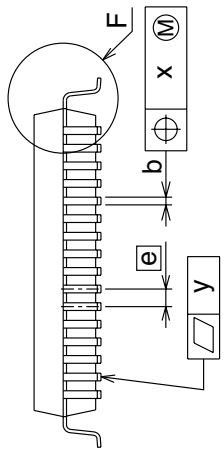
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A_1	0	0.1	0.2
A_2	—	2.8	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	—	0.8	—
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	—	1.4	—
x	—	—	0.2
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.5	—
l_2	1.3	—	—
M_D	—	14.6	—
M_E	—	20.6	—

Recommended Mount Pad









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