Advance Information

MAC7100EC/D
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MAC7100 Microcontroller Family Hardware Specifications

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32-bit Embedded Controller Division

This document provides electrical specifications, pin assignments, and package diagrams for MAC7100 family of microcontroller devices. For functional characteristics of the family, refer to the *MAC7100 Microcontroller Family Reference Manual* (MAC7100RM/D).

This document contains the following topics:

1 Overview

The MAC7100 Family of microcontrollers (MCUs) are members of a pin-compatible family of 32-bit Flash-memory-based devices developed specifically for embedded automotive applications. The pin-compatible family concept enables users to select between different memory and peripheral options for scalable designs. All MAC7100 Family members are composed of a 32-bit central processing unit (ARM7TDMI-S), up to 512Kbytes of embedded Flash EEPROM for program storage, up to 32Kbytes of embedded Flash for data and/or program storage, and up to 32Kbytes of RAM. The family is implemented with an enhanced DMA (eDMA) controller to improve performance for transfers between memory and many of the on-chip peripherals. The peripheral set includes asynchronous serial communications interfaces (eSCI), serial peripheral interfaces (DSPI), inter-integrated circuit (I^2C) bus controllers, FlexCAN interfaces, an enhanced modular I/O subsystem (eMIOS), 10-bit analog-to-digital converter (ATD) channels, general-purpose timers (PIT) and two special-purpose timers (RTI and SWT). The peripherals share a large number of general purpose input-output (GPIO) pins, all of which are bidirectional and available with interrupt capability to trigger wake-up from low-power chip modes.

The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. The operating frequency of devices in the family is up to a maximum of 50 MHz. The internal data paths between the CPU core, eDMA, memory and peripherals are all 32 bits wide, further improving performance for 32-bit applications. The

MAC7111 and MAC7131 also offer a 16-bit wide external data bus with 22 address lines. The family of devices is capable of operating over a junction temperature range of -40° C to 150° C.

Table 1 provides a comparison of members of the MAC7100 Family and the availability of peripheral modules on the various devices.

Table 1. MAC7100 Family Device Derivatives

Module Options	MAC7101	MAC7111	MAC7121	MAC7131	MAC7141
Program Flash	512Kbytes	512Kbytes	512Kbytes	512Kbytes	512Kbytes
Data Flash	32Kbytes	32Kbytes	32Kbytes	32Kbytes	32Kbytes
SRAM	32Kbytes	32Kbytes	32Kbytes	32Kbytes	32Kbytes
External Bus	No	Yes	No	Yes	No
ATD Modules	2	1	1	2	1
CAN Modules	4	4	4	4	2
eSCI Modules	4	4	4	4	2
DSPI Modules	2	2	2	2	2
I^2C Modules	1	1	1	1	1
eMIOS Module	16 channels, 16-bit	16 channels, 16-bit	16 channels, 16-bit	16 channels, 16-bit	16 channels, 16-bit
Timer Module	10 channels, 24-bit	10 channels, 24-bit	10 channels, 24-bit	10 channels, 24-bit	10 channels, 24-bit
GPIO Pins (max.)	111	111	84	127	71
Package	144 LQFP	144 LQFP	112 LQFP	208 MAP BGA	100 LQFP

2 Ordering Information

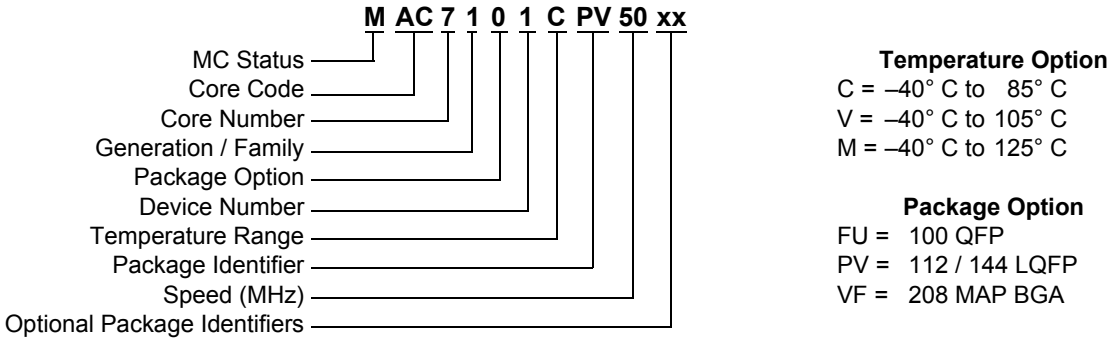


Figure 1. Order Part Number Example

3 Electrical Characteristics

This section contains electrical information for MAC7100 Family microcontrollers. The information is preliminary and subject to change without notice.

MAC7100 Family devices are specified and tested over the 5 V and 3.3 V ranges. For operation at any voltage within that range, the 3.3 V specifications generally apply. However, no production testing is done to verify operation at intermediate supply voltage levels.

3.1 Parameter Classification

The electrical parameters shown in this appendix are derived by various methods. To provide a better understanding to the designer, the following classification is used. Parameters are tagged accordingly in in the column labeled "C" of the parametric tables, as appropriate.

Table 2. Parametric Value Classification

P	Parameters guaranteed during production testing on each individual device.
C	Parameters derived by the design characterization and by measuring a statistically relevant sample size across process variations.
T	Parameters derived by design characterization on a small sample size from typical devices under typical conditions (unless otherwise noted). All values shown in the typical column are within this classification, even if not so tagged.
D	Parameters derived mainly from simulations.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. Functional operation outside these maximums is not guaranteed. Stress beyond these limits may affect reliability or cause permanent damage to the device.

MAC7100 Family devices contain circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either $V_{SS}5$ or $V_{DD}5$).

Table 3. Absolute Maximum Ratings

Num	Rating	Symbol	Min	Max	Unit
A1	I/O, Regulator and Analog Supply Voltage	$V_{DD}5$	–0.3	+6.0	V
A2	Digital Logic Supply Voltage [1]	$V_{DD}2.5$	–0.3	+3.0	V
A3	PLL Supply Voltage [1]	$V_{DD}PLL$	–0.3	+3.0	V
A4	ATD Supply Voltage	$V_{DD}A$	–0.3	+6.5	V
A5	Analog Reference	V_{RH}, V_{RL}	–0.3	+6.0	V
A6	Voltage difference $V_{DD}X$ to $V_{DD}A$	Δ_{VDDX}	–0.3	+0.3	V
A7	Voltage difference $V_{SS}X$ to $V_{SS}A$	Δ_{VSSX}	–0.3	+0.3	V
A8	Voltage difference $V_{RH} - V_{RL}$	$V_{RH} - V_{RL}$	–0.3	+6.5	V
A9	Voltage difference $V_{DD}A - V_{RH}$	$V_{DD}A - V_{RH}$	–6.5	+6.5	V
A10	Digital I/O Input Voltage	V_{IN}	–0.3	+6.0	V

Table 3. Absolute Maximum Ratings (continued)

Num	Rating	Symbol	Min	Max	Unit
A11	XFC, EXTAL, XTAL inputs	V_{ILV}	–0.3	+3.0	V
A12	TEST input	V_{TEST}	–0.3	+10.0	V
	Instantaneous Maximum Current [2]				
A13	Single pin limit for XFC, EXTAL, XTAL [3]	I_{DL}	–25	+25	mA
A14	Single pin limit for all digital I/O pins [4]	I_D	–25	+25	mA
A15	Single pin limit for all analog input pins [4]	I_{DA}	–25	+25	mA
A16	Single pin limit for TEST [5]	I_{DT}	–0.25	0	mA
A17	Storage Temperature Range	T_{stg}	–65	+155	°C

1 The device contains an internal voltage regulator to generate the logic and PLL supply from the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
2 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DD}A + 0.3$ V and $V_{NEGCLAMP} = –0.3$ V, then use the larger of the calculated values.
3 These pins are internally clamped to V_{SS}PLL and V_{DD}PLL.
4 All I/O pins are internally clamped to V_{SS}X and V_{DD}X, V_{SS}R and V_{DD}R or V_{SS}A and V_{DD}A.
5 This pin is clamped low to V_{SS}X, but not clamped high, and must be tied low in applications.

3.3 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise.

Table 4. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulses per pin positive negative	—	— 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	—	— 3 3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 5. ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
B1	C	Human Body Model (HBM)	V_{HBM}	2000	—	V
B2	C	Machine Model (MM)	V_{MM}	200	—	V
B3	C	Charge Device Model (CDM)	V_{CDM}	500	—	V
B4	C	Latch-up Current at T_A = 125°C positive negative	I_{LAT}	 +100 –100	—	mA
B5	C	Latch-up Current at T_A = 27°C positive negative	I_{LAT}	 +200 –200	—	mA

3.4 Operating Conditions

Unless otherwise noted, the following conditions apply to all parametric data. Refer to the temperature rating of the device (C, V, M) with respect to ambient temperature (T_A) and junction temperature (T_J). For power dissipation calculations refer to Section 3.5, “Power Dissipation and Thermal Characteristics.”

Table 6. MAC7100 Family Device Operating Conditions

Num	Rating		Symbol	Min	Typ	Max	Unit
C1	I/O, Regulator and Analog Supply Voltage		$V_{DD}5$	4.5	5	5.5	V
C2	Digital Logic Supply Voltage [1]		$V_{DD}2.5$	2.35	2.5	2.75	V
C3	PLL Supply Voltage [1]		$V_{DD}PLL$	2.35	2.5	2.75	V
C4	Voltage Difference $V_{DD}X$ to $V_{DD}A$		$\Delta_{VDD}X$	–0.1	0	0.1	V
C5	Voltage Difference $V_{SS}X$ to $V_{SS}A$		$\Delta_{VSS}X$	–0.1	0	0.1	V
C6	Oscillator Frequency		f_{osc}	0.5	—	16	MHz
C7	Bus Frequency		f_{bus}	0.5	—	50	MHz
C8a	MAC7100**C**	Operating Junction Temperature Range	T_J	–40	—	110	°C
C8b		Operating Ambient Temperature Range [2]	T_A	–40	25	85	°C
C9a	MAC7100**V**	Operating Junction Temperature Range	T_J	–40	—	130	°C
C9b		Operating Ambient Temperature Range [2]	T_A	–40	25	105	°C
C10a	MAC7100**M**	Operating Junction Temperature Range	T_J	–40	—	150	°C
C10b		Operating Ambient Temperature Range [2]	T_A	–40	25	125	°C

1 The device contains an internal voltage regulator to generate the logic and PLL supply from the I/O supply. The absolute maximum ratings apply when this regulator is disabled and the device is powered from an external source.

2 Please refer to Section 3.5, “Power Dissipation and Thermal Characteristics,” for more details about the relation between ambient temperature T_A and device junction temperature T_J.

3.4.1 5 V I/O Pins

The I/O pins operate at a nominal level of 5 V. This class of pins is comprised of the clocks, control and general purpose/peripheral pins. The internal structure of these pins is identical; however, some functionality may be disabled (for example, for analog inputs the output drivers, pull-up/down resistors are permanently disabled).

3.4.2 Oscillator Pins

The pins XFC, EXTAL, XTAL are dedicated to the oscillator and operate at a nominal level of 2.5 V.

3.5 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded.

Note that the JEDEC specification reserves the symbol $R_{\theta JA}$ or θ_{JA} (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment. $R_{\theta JMA}$ or θ_{JMA} (Theta-JMA) will be used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated that the generic name, θ_{JA}, will continue to be commonly used.

The average chip-junction temperature (T_J) in °C is obtained from:

$$T_J = T_A + (\Theta_{JA})$$

T_J = Junction Temperature (°C)

T_A = Ambient Temperature (°C)

P_D = Total Chip Power Dissipation (W)

Θ_{JA} = Package Thermal Resistance (°C/W)

The total power dissipation is calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation (W)

$$P_{INT} = (I_{DD} \times V_{DD}) + (I_{DD}PLL \times V_{DD}PLL) + (I_{DD}A \times V_{DD}A)$$

Two cases for P_{IO}, with the internal voltage regulator enabled and disabled, must be considered:

1. Internal Voltage Regulator disabled:

   $$P_{IO} = \sum_i R_{DSON} \cdot (I_{IO_i})^2$$

   P_{IO} is the sum of all output currents on I/O ports associated with $V_{DD}X$ and $V_{DD}R$.

   $$R_{DSON} = \frac{V_{OL}}{I_{OL}} \text{ (for outputs driven low)}$$

   or

   $$R_{DSON} = \frac{V_{DD}5 - V_{OH}}{I_{OL}} \text{ (for outputs driven high)}$$

2. Internal voltage regulator enabled:

   $$P_{INT} = (I_{DD}R \times V_{DD}R) + (I_{DD}A \times V_{DD}A)$$

   $I_{DD}R$ is the current shown in Table 12 and not the overall current flowing into $V_{DD}R$, which additionally contains the current flowing into the external loads with output high.

3.5.1 Power Dissipation Simulation Details

Table 7. Thermal Resistance for 100 lead 14x14 mm LQFP, 0.5 mm Pitch [1]

Rating			Value	Unit	Comments
Junction to Ambient (Natural Convection)	Single layer board (1s)	$R_{\theta JA}$	44	°C/W	1, 2
Junction to Ambient (Natural Convection)	Four layer board (2s2p)	$R_{\theta JMA}$	34	°C/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Single layer board (1s)	$R_{\theta JMA}$	37	°C/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Four layer board (2s2p)	$R_{\theta JMA}$	29	°C/W	1, 3
Junction to Board		$R_{\theta JB}$	18	°C/W	4
Junction to Case		$R_{\theta JC}$	7	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6

1 100 LQFP, Case Outline: 983–02

Table 8. Thermal Resistance for 112 lead 20x20 mm LQFP, 0.65 mm Pitch [1]

Rating			Value	Unit	Comments
Junction to Ambient (Natural Convection)	Single layer board (1s)	$R_{\theta JA}$	42	°C/W	1, 2
Junction to Ambient (Natural Convection)	Four layer board (2s2p)	$R_{\theta JMA}$	34	°C/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Single layer board (1s)	$R_{\theta JMA}$	35	°C/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Four layer board (2s2p)	$R_{\theta JMA}$	30	°C/W	1, 3
Junction to Board		$R_{\theta JB}$	22	°C/W	4
Junction to Case		$R_{\theta JC}$	7	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6

1 112 LQFP, Case Outline: 987–01

Table 9. Thermal Resistance for 144 lead 20x20 mm LQFP, 0.5 mm Pitch [1]

Rating			Value	Unit	Comments
Junction to Ambient (Natural Convection)	Single layer board (1s)	$R_{\theta JA}$	42	°C/W	1, 2
Junction to Ambient (Natural Convection)	Four layer board (2s2p)	$R_{\theta JMA}$	34	°C/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Single layer board (1s)	$R_{\theta JMA}$	35	°C/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Four layer board (2s2p)	$R_{\theta JMA}$	30	°C/W	1, 3
Junction to Board		$R_{\theta JB}$	22	°C/W	4
Junction to Case		$R_{\theta JC}$	7	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6

1 144 LQFP, Case Outline: 918–03

Table 10. Thermal Resistance for 208 lead 17x17 mm MAP, 1.0 mm Pitch [1]

Rating			Value	Unit	Comments
Junction to Ambient (Natural Convection)	Single layer board (1s)	$R_{\theta JA}$	46	°C/W	1, 2
Junction to Ambient (Natural Convection)	Four layer board (2s2p)	$R_{\theta JMA}$	29	°C/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Single layer board (1s)	$R_{\theta JMA}$	38	°C/W	1, 3
Junction to Ambient (@ 200 ft./min.)	Four layer board (2s2p)	$R_{\theta JMA}$	26	°C/W	1, 3
Junction to Board		$R_{\theta JB}$	19	°C/W	4
Junction to Case		$R_{\theta JC}$	7	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	6

1 208 MAP BGA, Case Outline: 1159A-01

Comments:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board at the center lead. For fused lead packages, the adjacent lead is used.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Power Dissipation 1/8 Simulation Model Packaging Parameters

Component	Conductivity
Mold Compound	0.9 W/m K
Leadframe (Copper)	263 W/m K
Die Attach	1.7 W/m K

3.6 Power Supply

The MAC7100 Family utilizes several pins to supply power to the oscillator, PLL, digital core, I/O ports and ATD. In the context of this section, $V_{DD}5$ is used for $V_{DD}A$, $V_{DD}R$ or $V_{DD}X$; $V_{SS}5$ is used for $V_{SS}A$, $V_{SS}R$ or $V_{SS}X$ unless otherwise noted. $I_{DD}5$ denotes the sum of the currents flowing into the $V_{DD}A$, $V_{DD}X$, and $V_{DD}R$. V_{DD} is used for $V_{DD}2.5$, and $V_{DD}PLL$, V_{SS} is used for $V_{SS}2.5$ and $V_{SS}PLL$. I_{DD} is used for the sum of the currents flowing into $V_{DD}2.5$ and $V_{DD}PLL$.

3.6.1 Current Injection

The power supply must maintain regulation within the $V_{DD}5$ or $V_{DD}2.5$ operating range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}5$) is greater than $I_{DD}5$, the injection current may flow out of $V_{DD}5$ and could result in the external power supply going out of regulation. It is important to ensure that the external $V_{DD}5$ load will shunt current greater than the maximum injection current. The greatest risk will be when the MCU is consuming very little power (for example, if no system clock is present, or if the clock rate is very low).

3.6.2 Power Supply Pins

The $V_{DD}R - V_{SS}R$ pair supplies the internal voltage regulator. The $V_{DD}A - V_{SS}A$ pair supplies the A/D converter and the reference circuit of the internal voltage regulator. The $V_{DD}X - V_{SS}X$ pair supplies the I/O pins. $V_{DD}PLL - V_{SS}PLL$ pair supplies the oscillator and PLL.

All $V_{DD}X$ pins are internally connected by metal. All $V_{SS}X$ pins are internally connected by metal. All $V_{SS}2.5$ pins are internally connected by metal. $V_{DD}A$, $V_{DD}X$ and $V_{DD}R$ as well as $V_{SS}A$, $V_{SS}X$ and $V_{SS}R$ are connected by anti-parallel diodes for ESD protection.

3.6.3 Supply Currents

All current measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 40MHz bus frequency using a 4MHz oscillator in low power mode. Production testing is performed using a square wave signal at the EXTAL input.

In expanded modes, the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A good estimate is to take the single chip currents and add the currents due to the external loads.

Table 12. Supply Current Characteristics

Num	C	Rating			Symbol	Typ	Max	Unit
D1a	C	**Run Supply Current** Single Chip	**Core**	–40° C	$I_{DD}R_{core}$	— [1]	— [1]	mA
				25° C		— [1]	— [1]	mA
				85° C [2]		— [1]	— [1]	mA
				105° C [2]		— [1]	— [1]	mA
				125° C [2]		— [1]	— [1]	mA
D1b	C		**Regulator** (if enabled)	–40° C	$I_{DD}R_{reg}$	— [1]	— [1]	mA
				25° C		— [1]	— [1]	mA
				85° C [2]		— [1]	— [1]	mA
				105° C [2]		— [1]	— [1]	mA
				125° C [2]		— [1]	— [1]	mA
D1c	C		**Pins**	–40° C	$I_{DD}R_{pins}$	— [1]	— [1]	mA
				25° C		— [1]	— [1]	mA
				85° C [2]		— [1]	— [1]	mA
				105° C [2]		— [1]	— [1]	mA
				125° C [2]		— [1]	— [1]	mA
D2	C	**Doze Supply Current**	Run ≥ Doze ≥ Pseudo Stop					
D3a	C	**Psuedo Stop Current** PLL on	**Core**	–40° C	$I_{DD}PS_{core}$	— [1]	— [1]	µA
				25° C		— [1]	— [1]	µA
				85° C [2]		— [1]	— [1]	µA
				105° C [2]		— [1]	— [1]	µA
				125° C [2]		— [1]	— [1]	µA
D3b	C		**Regulator**	–40° C	$I_{DD}PS_{reg}$	— [1]	— [1]	µA
				25° C		278 / 327 [3]	— [1]	µA
				85° C [2]		— [1]	— [1]	µA
				105° C [2]		— [1]	— [1]	µA
				125° C [2]		— [1]	— [1]	µA
D3c	C		**Pins**	–40° C	$I_{DD}PS_{pins}$	— [1]	— [1]	µA
				25° C		4 / 5 [3]	— [1]	µA
				85° C [2]		— [1]	— [1]	µA
				105° C [2]		— [1]	— [1]	µA
				125° C [2]		— [1]	— [1]	µA
D4a	C	**Stop Current** $T_J = T_A$ assumed	**Core**	–40° C	$I_{DD}S_{core}$	— [1]	— [1]	µA
				25° C		— [1]	— [1]	µA
				85° C [2]		— [1]	— [1]	µA
				105° C [2]		— [1]	— [1]	µA
				125° C [2]		— [1]	— [1]	µA
D4b	C		**Regulator**	–40° C	$I_{DD}S_{reg}$	— [1]	— [1]	µA
				25° C		68	— [1]	µA
				85° C [2]		— [1]	— [1]	µA
				105° C [2]		— [1]	— [1]	µA
				125° C [2]		— [1]	— [1]	µA
D4c	C		**Pins**	–40° C	$I_{DD}S_{pins}$	— [1]	— [1]	µA
				25° C		4	— [1]	µA
				85° C [2]		— [1]	— [1]	µA
				105° C [2]		— [1]	— [1]	µA
				125° C [2]		— [1]	— [1]	µA

1 At the time of publication, this value is yet to be determined, and will be supplied when device characterization is complete.
2 85°C, 105°C, and 125°C refer to the "C", "V", and "M" Temperature Options, respectively.
3 RTI disabled / enabled.

3.6.4 Voltage Regulator Characteristics

Table 13. VREG Operating Conditions

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
E1	P	Input Voltages	V_{VDDRA}	2.97	—	5.5	V
E2	P	Regulator Current Reduced Power Mode Shutdown Mode	I_{REG}	 — —	 TBD TBD	 50 40	 μA μA
E3	P	Output Voltage Core Full Performance Mode Reduced Power Mode Shutdown Mode	V_{DD}	 2.45 1.60 —	 2.5 2.5 — [1]	 2.75 2.75 —	 V V V
E4	P	Output Voltage PLL Full Performance Mode Reduced Power Mode [2] Reduced Power Mode [3] Shutdown Mode	$V_{DD}PLL$	 2.35 2.00 1.60 —	 2.5 2.5 2.5 — [1]	 2.75 2.75 2.75 —	 V V V V
E5	P	Low Voltage Interrupt [4] Assert Level Deassert Level	 V_{LVIA} V_{LVID}	 4.10 4.25	 4.37 4.52	 4.66 4.77	 V V
E6	P	Low Voltage Reset [5] Assert Level	 V_{LVRA}	 2.25	 2.35	 —	 V
E7	P	Power On Reset [6] Assert Level Deassert Level	 V_{PORA} V_{PORD}	 0.97 —	 — —	 — 2.05	 V V

1 High Impedance Output.
2 Current $I_{DD}PLL$ = 1mA (Low Power Oscillator).
3 Current $I_{DD}PLL$ = 3mA (Standard Oscillator).
4 Monitors $V_{DD}A$, active only in full performance mode. Indicated I/O and ATD performance degradation due to low supply voltage.
5 Monitors $V_{DD}2.5$, active only in full performance mode. Only POR is active in reduced performance mode.
6 Monitors $V_{DD}2.5$, active in all modes.

3.6.5 Chip Power Up and Voltage Drops

The VREG sub-modules LVI (low voltage interrupt), POR (power on reset) and LVR (low voltage reset) handle chip power-up or drops of the supply voltage. Refer to Figure 2.

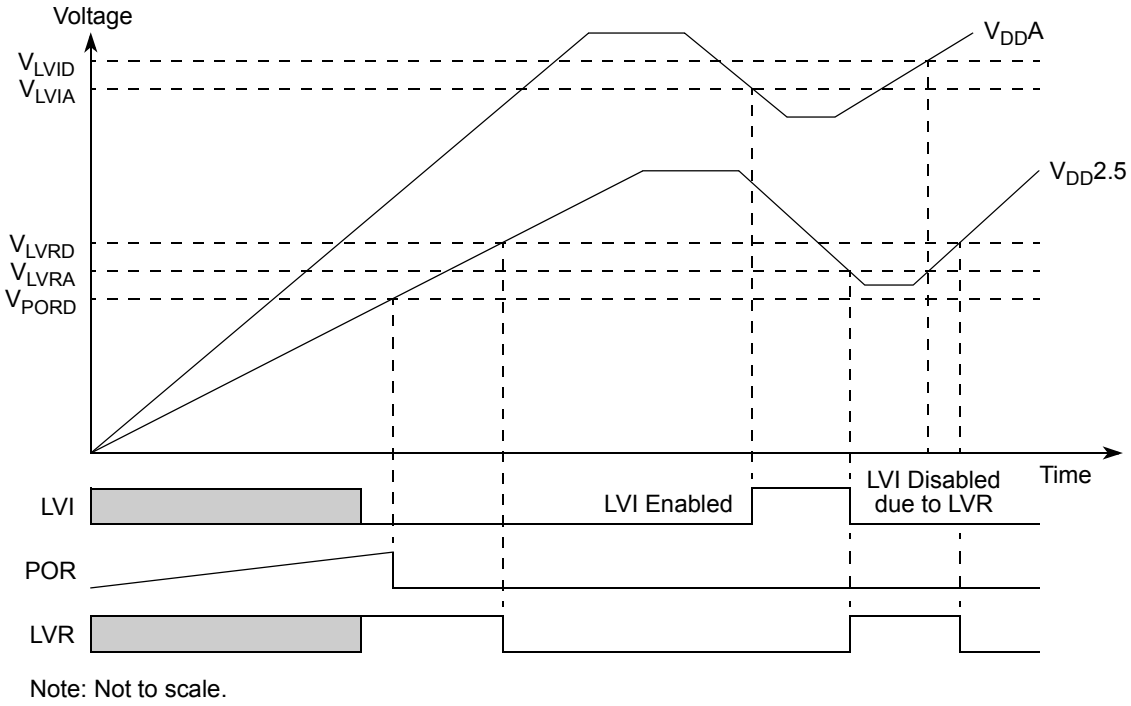


Figure 2. VREG Chip Power-up and Voltage Drops

3.6.6 Output Loads

The on-chip voltage regulator is intended to supply the internal logic and oscillator circuits. No external DC load is allowed. Capacitive loads are specified in Table 14. Capacitors with X7R dielectricum are required.

Table 14. VREG Recommended Load Capacitances

Rating	Symbol	Min	Typ	Max	Unit
Load Capacitance on each V_{DD}2.5 pin	C_{LVDD}	200	440	12000	nF
Load Capacitance on V_{DD}PLL pin	$C_{LVDDfcPLL}$	90	220	5000	nF

3.7 I/O Characteristics

This section describes the characteristics of all I/O pins in both 3.3 V and 5 V operating conditions. All parameters are not always applicable; for example, not all pins feature pull up/down resistances.

Table 15. 5 V I/O Characteristics

Conditions shown in Table 6 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
F1a	P	Input High Voltage	V_{IH}	0.65 × $V_{DD}5$	—	—	V
F1b	T	Input High Voltage	V_{IH}	—	—	$V_{DD}5$ + 0.3	V
F2a	P	Input Low Voltage	V_{IL}	—	—	0.35 × $V_{DD}5$	V
F2b	T	Input Low Voltage	V_{IL}	$V_{SS}5$ – 0.3	—	—	V
F3	C	Input Hysteresis	V_{HYS}	—	250	—	mV
F4	P	Input Leakage Current (pins in high impedance input mode) [1] V_{in} = $V_{DD}5$ or $V_{SS}5$	I_{in}	TBD	—	TBD	µA
F5	P	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –2mA Full Drive I_{OH} = –10mA	V_{OH}	$V_{DD}5$ – 0.8	—	—	V
F6	P	Output Low Voltage (pins in output mode) Partial Drive I_{OL} = +2mA Full Drive I_{OL} = +10mA	V_{OL}	—	—	0.8	V
F7	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	—	—	–130	µA
F8	P	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	–10	—	—	µA
F9	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	—	—	130	µA
F10	P	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	—	—	µA
F11	D	Input Capacitance	C_{in}	—	6	—	pF
F12	T	Injection current [2] Single Pin limit Total Device Limit. Sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	—	 2.5 25	µA
F13	P	Port Interrupt Input Pulse filtered [3]	t_{PULSE}	—	—	3	µs
F14	P	Port Interrupt Input Pulse passed [3]	t_{PULSE}	10	—	—	µs

1 Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°C to 12°C in the temperature range from 50°C to 125°C.
2 Refer to Section 3.6.1, “Current Injection,” for more details
3 Parameter only applies in STOP or Pseudo STOP mode.

Table 16. 3.3 V I/O Characteristics

Conditions shown in Table 6, with $V_{DD}X$ = 3.3 V ±10% and a temperature maximum of +140°C unless otherwise noted.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
G1a	P	Input High Voltage	V_{IH}	0.65 × $V_{DD}5$	—	—	V
G1b	T	Input High Voltage	V_{IH}	—	—	$V_{DD}5$ + 0.3	V
G2a	P	Input Low Voltage	V_{IL}	—	—	0.35 × $V_{DD}5$	V
G2b	T	Input Low Voltage	V_{IL}	$V_{SS}5$ – 0.3	—	—	V
G3	C	Input Hysteresis	V_{HYS}	—	250	—	mV
G4	P	Input Leakage Current (pins in high impedance input mode) [1] V_{in} = $V_{DD}5$ or $V_{SS}5$	I_{in}	TBD	—	TBD	µA
G5	P	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –0.75mA Full Drive I_{OH} = –4.5mA	V_{OH}	$V_{DD}5$ – 0.4	—	—	V
G6	P	Output Low Voltage (pins in output mode) Partial Drive I_{OL} = +0.9mA Full Drive I_{OL} = +5.5mA	V_{OL}	—	—	0.4	V
G7	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	—	—	–60	µA
G8	P	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	–6	—	—	µA
G9	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	—	—	60	µA
G10	P	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	6	—	—	µA
G11	D	Input Capacitance	C_{in}	—	6	—	pF
G12	T	Injection current [2] Single Pin limit Total Device Limit. Sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	—	 2.5 25	µA
G13	P	Port Interrupt Input Pulse filtered [3]	t_{PULSE}	—	—	3	µs
G14	P	Port Interrupt Input Pulse passed [3]	t_{PULSE}	10	—	—	µs

1 Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°C to 12°C in the temperature range from 50°C to 125°C.

2 Refer to Section 3.6.1, “Current Injection,” for more details

3 Parameter only applies in STOP or Pseudo STOP mode.

3.8 Clock and Reset Generator Electrical Characteristics

This section describes the electrical characteristics for the oscillator, phase-locked loop, clock monitor and reset generator.

3.8.1 Oscillator Characteristics

The MAC7100 Family features an internal low power loop controlled Pierce oscillator and a full swing Pierce oscillator/external clock mode. The selection of loop controlled Pierce oscillator or full swing Pierce oscillator/external clock depends on the level of the $\overline{\text{XCLKS}}$ signal at the rising edge of the $\overline{\text{RESET}}$ signal. Before asserting the oscillator to the internal system clock distribution subsystem, the quality of the oscillation is checked for each start from either power on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC}. The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Clock Monitor Assert Frequency f_{CMFA}.

Table 17. Oscillator Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
H1a	C	Crystal oscillator range (loop controlled Pierce)	f_{OSC}	4.0	—	16	MHz
H1b	C	Crystal oscillator range (full swing Pierce) [1, 2]	f_{OSC}	0.5	—	40	MHz
H2	P	Startup Current	I_{OSC}	100	—	—	μA
H3	C	Oscillator start-up time (loop controlled Pierce)	t_{UPOSC}	—	TBD [3]	50 [4]	ms
H4	D	Clock Quality check time-out	t_{CQOUT}	0.45	—	2.5	s
H5	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
H6	P	External square wave input frequency [2]	f_{EXT}	0.5	—	40	MHz
H7	D	External square wave pulse width low	t_{EXTL}	9.5	—	—	ns
H8	D	External square wave pulse width high	t_{EXTH}	9.5	—	—	ns
H9	D	External square wave rise time	t_{EXTR}	—	—	1	ns
H10	D	External square wave fall time	t_{EXTF}	—	—	1	ns
H11	D	Input Capacitance (EXTAL, XTAL pins)	C_{IN}	—	7	—	pF
H12	C	EXTAL pin DC Operating Bias in loop controlled mode	V_{DCBIAS}	—	TBD	—	V

1 Depending on the crystal; a damping series resistor might be necessary
2 $\overline{\text{XCLKS}}$ negated during reset
3 f_{osc} = 4 MHz, C = 22 pF.
4 Maximum value is for extreme cases using high Q, low frequency crystals

3.8.2 PLL Filter Characteristics

The oscillator provides the reference clock for the PLL. The voltage controlled oscillator (VCO) of the PLL is also the system clock source in self clock mode. In order to operate reliably, care must be taken to select proper values for external loop filter components.

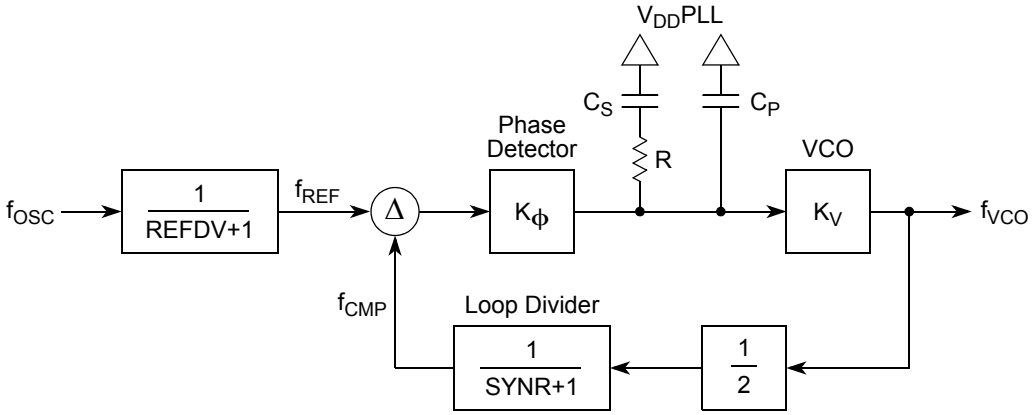


Figure 3. Basic PLL Functional Diagram

The procedure described below can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from Table 18. First, the VCO Gain at the desired VCO output frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{VCO})}{K_1 \cdot 1V}}$$

The phase detector relationship is given by:

$$K_\Phi = -|i_{ch}| \cdot K_V$$

i_{ch} is the current in tracking mode. The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot (\zeta + \sqrt{1 + \zeta^2})} \left(\frac{1}{50} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 50}; (\zeta = 0.9) \right)$$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (synr + 1)$$

With the above inputs the resistance can be calculated as:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi}$$

The capacitance C_S can now be calculated as:

$$C_S = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9)$$

The capacitance C_P should be chosen in the range of:

$$C_S \div 20 \leq C_P \leq C_S \div 10$$

The stabilization delays shown in Table 18 are dependant on PLL operational settings and external component selection (for example, crystal, XFC filter).

3.8.2.1 Jitter Information

The basic functionality of the PLL is shown in Figure 3. With each transition of the clock f_{cmp}, the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly. The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in Figure 4. It is important to note that the pre-scaler used by timers and serial modules will eliminate the effect of PLL jitter to a large extent.

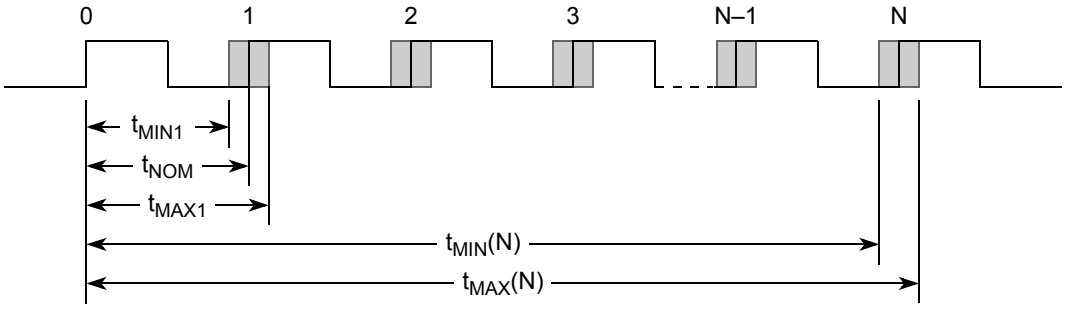


Figure 4. Jitter Definitions

The relative deviation of t_{NOM} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N). Thus, jitter is defined as:

$$J(N) = \max\left(\left|1 - \frac{t_{MAX}(N)}{N \cdot t_{NOM}}\right|, \left|1 - \frac{t_{MIN}(N)}{N \cdot t_{NOM}}\right|\right)$$

For N < 100, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$

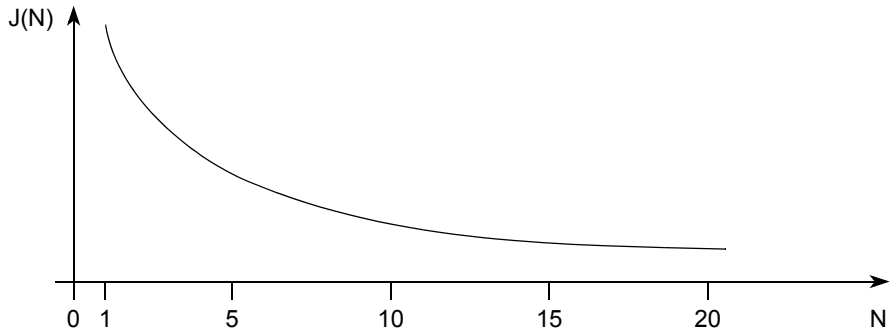


Figure 5. Maximum Bus Clock Jitter Approximation

3.8.3 PLL Characteristics

Table 18. PLL Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
J1		PLL reference frequency, crystal oscillator range [1]	f_{REF}	0.5	—	16	MHz
J2	P	Self Clock Mode frequency	f_{SCM}	1	—	5.5	MHz
J3	D	VCO locking range	f_{VCO}	8	—	40	MHz
J4	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3	—	4	% [2]
J5	D	Lock Detection	$\|\Delta_{Lock}\|$	0	—	1.5	% [2]
J6	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5	—	2.5	% [2]
J7	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6	—	8	% [2]
J8	C	PLLON Total Stabilization delay (Auto Mode) [3]	t_{stab}	—	0.5 [4]	3 [5]	ms
J9	D	PLLON Acquisition mode stabilization delay [3]	t_{acq}	—	0.3 [5]	1 [4]	ms
J10	D	PLLON Tracking mode stabilization delay [3]	t_{al}	—	0.2 [5]	2 [4]	ms
J11	D	Charge pump current acquisition mode	$\| i_{ch} \|$	—	38.5	—	μA
J12	D	Charge pump current tracking mode	$\| i_{ch} \|$	—	3.5	—	μA
J13	D	Jitter fit VCO loop gain parameter	K_1	—	–100	—	MHz/V
J14	D	Jitter fit VCO loop frequency parameter	f_1	—	60	—	MHz
J15	C	Jitter fit parameter 1	j_1	—	—	TBD	% [4]
J16	C	Jitter fit parameter 2	j_2	—	—	TBD	% [4]

1 V_{DD}PLL at 2.5 V.
2 Percentage deviation from target frequency
3 PLL stabilization delay is highly dependent on operational requirement and external component values (for example, crystal and XFC filter component values). Notes 4 and 5 show component values for a typical configurations. Appropriate XFC filter values should be chosen based on operational requirement of system.
4 f_{REF} = 4 MHz, f_{SYS} = 25 MHz (REFDV = 0x03, SYNR = 0x01), C_S = 4.7 nF, C_P = 470 pF, R_S = 10 KΩ.
5 f_{REF} = 4 MHz, f_{SYS} = 8 MHz (REFDV = 0x00, SYNR = 0x01), C_S = 33 nF, C_P = 3.3 nF, R_S = 2.7 KΩ.

3.8.4 Crystal Monitor Time-out

The time-out Table 19 shows the delay for the crystal monitor to trigger when the clock stops, either at the high or at the low level. The corresponding clock period with an ideal 50% duty cycle is twice this time-out value.

Table 19. Crystal Monitor Time-Outs

Min	Typ	Max	Unit
6	10	18.5	μs

3.8.5 Clock Quality Checker

The timing for the clock quality check is derived from the oscillator and the VCO frequency range in Table 18. These numbers define the upper time limit for the individual check windows to complete.

Table 20. CRG Maximum Clock Quality Check Timings

Clock Check Windows	Value	Unit
Check Window	9.1 to 20.0	ms
Timeout Window	0.46 to 1.0	s

3.8.6 Startup

Table 21 summarizes several startup characteristics explained in this section. Refer to the *MAC7100 Microcontroller Family Reference Manual* (MAC7100RM/D) for a detailed description of the startup behavior.

Table 21. CRG Startup Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
K1	T	POR release level	V_{PORR}	—	—	2.07	V
K2	T	POR assert level	V_{PORA}	0.97	—	—	V
K3	D	Reset input pulse width, minimum input time	PW_{RSTL}	2	—	—	t_{osc}
K4	D	Startup from Reset	n_{RST}	192	—	196	n_{osc}
K5	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20	—	—	ns
K6	D	Wait recovery startup time	t_{WRS}	—	—	14	t_{cyc}

3.8.6.1 Power On and Low Voltage Reset (POR and LVR)

The release level V_{PORR} and the assert level V_{PORA} are derived from the $V_{DD}2.5$ supply. The assert level V_{LVRA} is derived from the $V_{DD}2.5$ supply. They are also valid if the device is powered externally. After releasing the POR or LVR reset, the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self-generated clock. The fastest startup time possible is given by t_{uposc} (refer to Table 17).

3.8.6.2 SRAM Data Retention

The SRAM contents integrity is guaranteed if the PORF bit in the CRGFLG register is not set following a reset operation.

3.8.6.3 External Reset

When external reset is asserted for a time greater than PW_{RSTL}, the CRG module generates an internal reset and the CPU starts fetching the reset vector without doing a clock quality check, if there was stable oscillation before reset.

3.8.6.4 Stop Recovery

The MCU can be returned to run mode from the stop mode by an external interrupt. A clock quality check is performed in the same manner as for POR before releasing the clocks to the system.

3.8.6.5 Pseudo Stop and Doze Recovery

Recovery from pseudo stop and doze modes are essentially the same, since the oscillator is not stopped in either mode. The controller is returned to run mode by internal or external interrupts or other wakeup events in the system. After t_{wrs}, the CPU fetches an interrupt vector if the wakeup event was an interrupt, or continues to execute code if the wakeup event was not an interrupt.

3.9 External Bus Timing Specifications

Table 22 lists processor bus input timings, which are shown in Figure 6, Figure 7 and Figure 8.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

Table 22. External Bus Input Timing Specifications

Num	C	Rating [1]	Symbol	Min	Max	Unit
L1		CLKOUT	t_{CYC}	23	—	ns
Control Inputs						
L2a		Control input valid to CLKOUT high [2]	t_{CVCH}	13	—	ns
L3a		CLKOUT high to control inputs invalid [2]	t_{CHCII}	0	—	ns
Data Inputs						
L4		Data input (DATA[15:0]) valid to CLKOUT high	t_{DIVCH}	9	—	ns
L5		CLKOUT high to data input (DATA[15:0]) invalid	t_{CHDII}	0	—	ns

1 Timing specifications have been indicated taking into account the full drive strength for the pads.
2 $\overline{TA}$ pins are being referred to as control inputs.

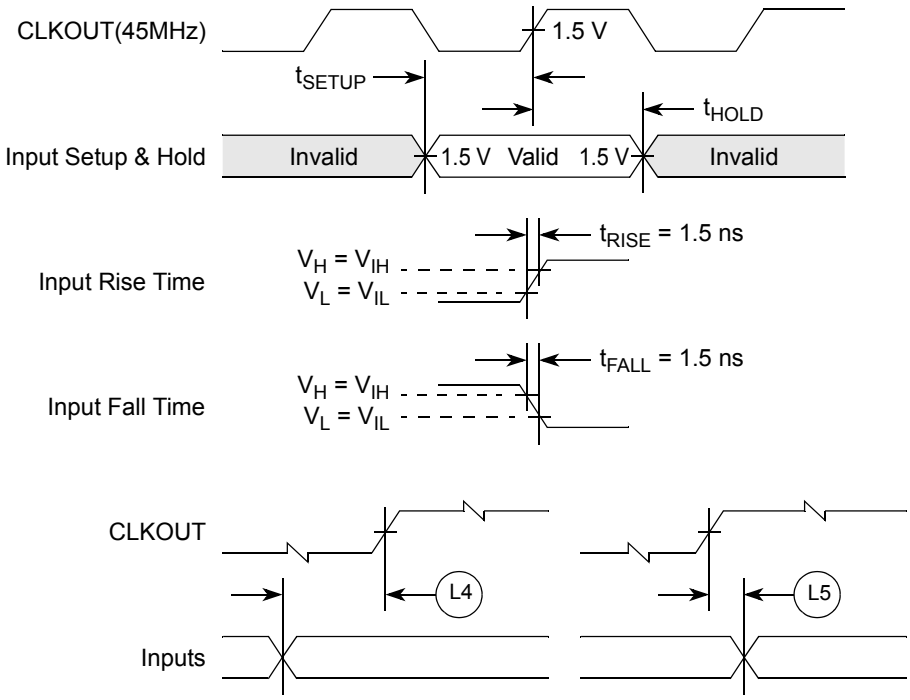


Figure 6. General Input Timing Requirements

3.9.1 Read and Write Bus Cycles

Table 23 lists processor bus output timings. Read/write bus timings listed in Table 23 are shown in Figure 7 and Figure 8.

Table 23. External Bus Output Timing Specifications

Num	C	Rating	Symbol	Min	Max	Unit
Control Outputs						
L6a		CLKOUT high to chip selects valid [1]	t_{CHCV}	—	$0.5t_{CYC}$ + 10	ns
L6b		CLKOUT high to byte select ($\overline{BS}$[1:0]) valid [2]	t_{CHBV}	—	$0.5t_{CYC}$ + 10	ns
L6c		CLKOUT high to output select ($\overline{OE}$) valid [3]	t_{CHOV}	—	$0.5t_{CYC}$ + 10	ns
L7a		CLKOUT high to control output ($\overline{BS}$[1:0], $\overline{OE}$) invalid	t_{CHCOI}	$0.5t_{CYC}$ + 2	—	ns
L7b		CLKOUT high to chip selects invalid	t_{CHCI}	$0.5t_{CYC}$ + 2	—	ns
Address and Attribute Outputs						
L8		CLKOUT high to address (ADDR[21:0]) and control (R/$\overline{W}$) valid	t_{CHAV}	—	10	ns
L9		CLKOUT high to address (ADDR[21:0]) and control (R/$\overline{W}$) invalid	t_{CHAI}	2	—	ns
Data Outputs						
L10		CLKOUT high to data output (DATA[15:0]) valid	t_{CHDOV}	—	13	ns
L11		CLKOUT high to data output (DATA[15:0]) invalid	t_{CHDOI}	2	—	ns
L12		CLKOUT high to data output (DATA[15:0]) high impedance	t_{CHDOZ}	—	9	ns

1 $\overline{CS}n$ transitions after the falling edge of CLKOUT.
2 $\overline{BS}n$ transitions after the falling edge of CLKOUT.
3 $\overline{OE}$ transitions after the falling edge of CLKOUT.

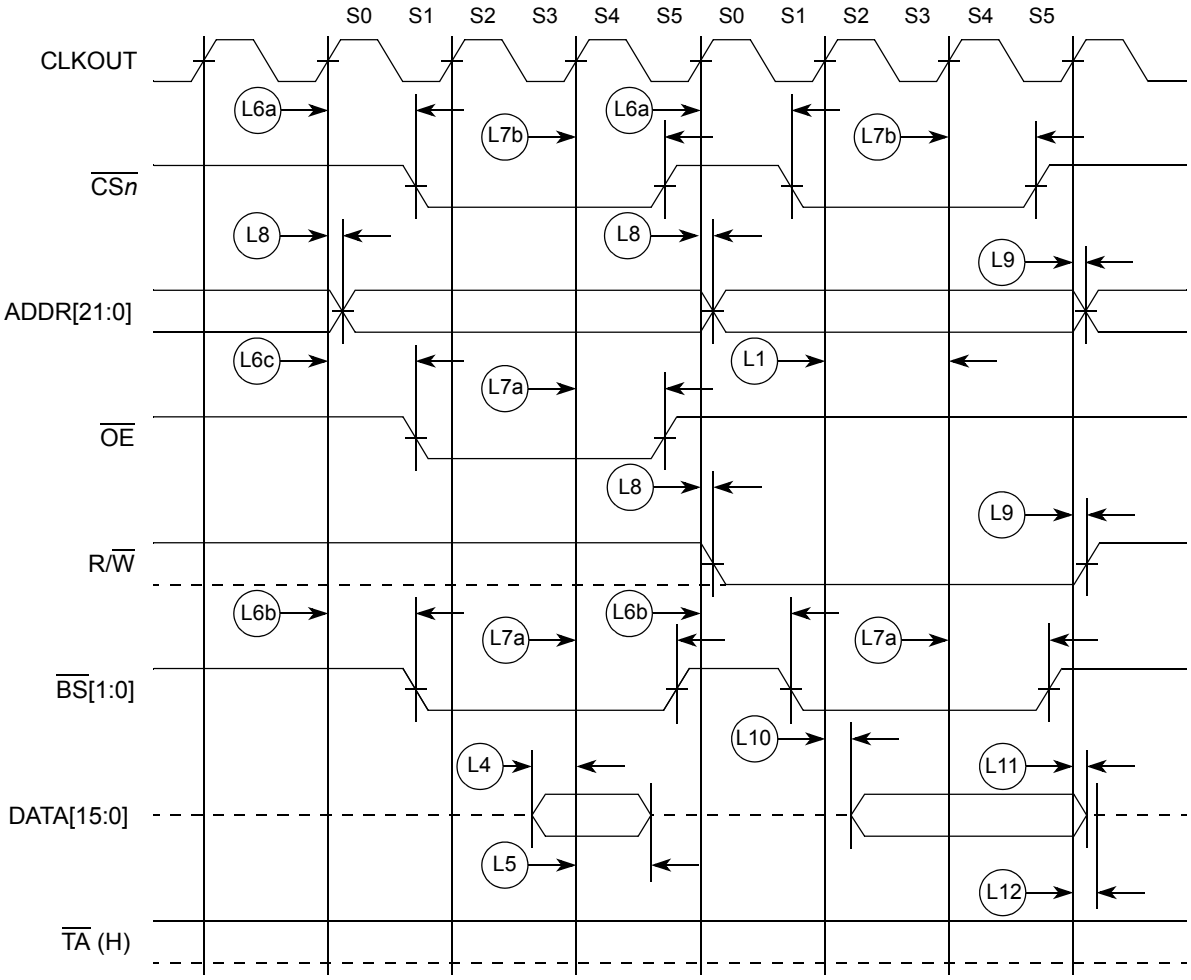


Figure 7. Read/Write (Internally Terminated) Bus Timing

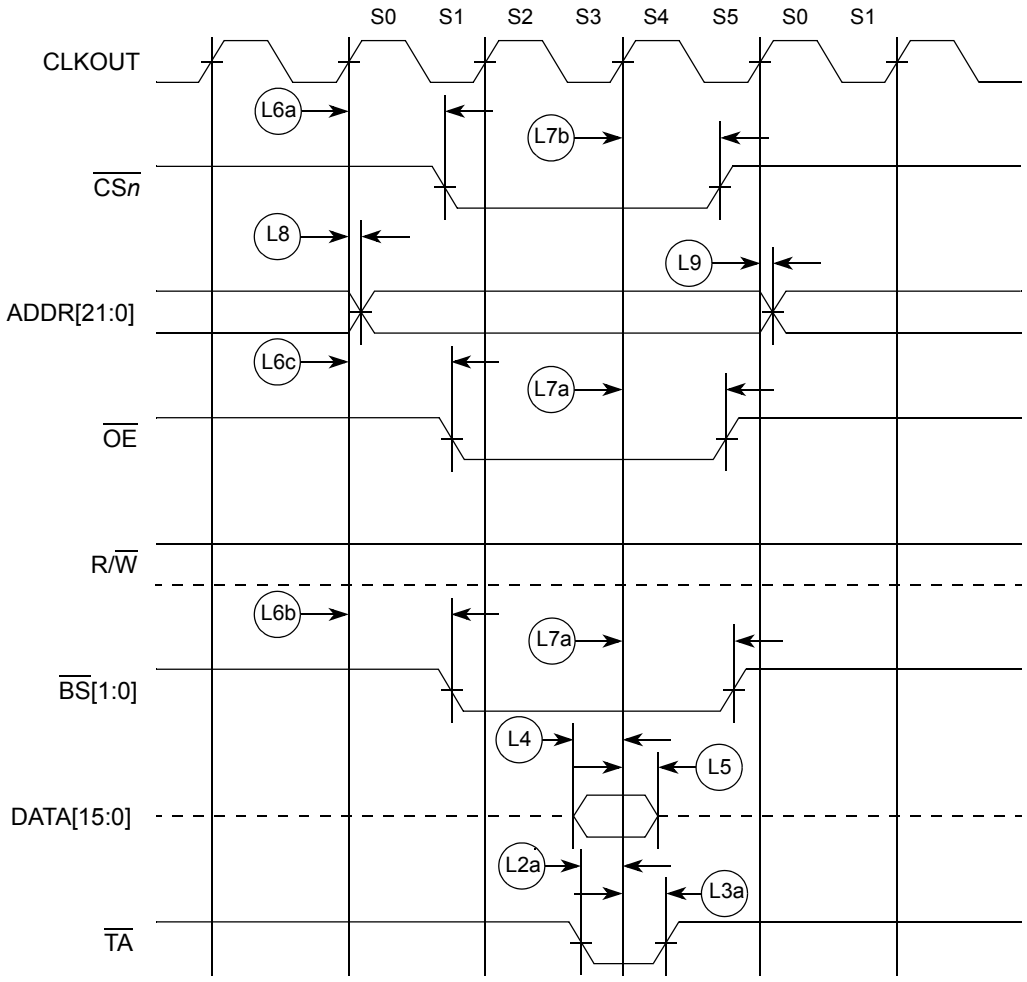


Figure 8. Read Bus Cycle Terminated by $\overline{TA}$

3.10 Analog-to-Digital Converter Characteristics

Table 24 and Table 25 show conditions under which the ATD operates. The following constraints exist to obtain full-scale, full range results: $V_{SS}A \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DD}A$. This constraint exists because the sample buffer amplifier cannot drive beyond the ATD power supply levels. If the input level goes outside of this range it will effectively be clipped.

Table 24. ATD Operating Characteristics in 5 V Range

Conditions shown in Table 6 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
M1	D	Reference Potential Low High	V_{RL} V_{RH}	$V_{SS}A$ $V_{DD}A \div 2$	— —	$V_{DD}A \div 2$ $V_{DD}A$	V V
M2	C	Differential Reference Voltage [1]	$V_{RH} - V_{RL}$	4.50	5.00	5.25	V
M3	D	ATD Clock Frequency	f_{ATDCLK}	0.5	—	2.0	MHz
M4	D	ATD 10-bit Conversion PeriodClock Cycles [2] @ 2.0MHz f_{ATDCLK}	N_{CONV10} T_{CONV10}	14 7	— —	28 14	Cycles µs
M5	D	ATD 8-bit Conversion PeriodClock Cycles [2] @ 2.0MHz f_{ATDCLK}	N_{CONV8} T_{CONV8}	12 6	— —	26 13	Cycles µs
M6	D	Recovery Time ($V_{DD}A$ = 5.0 V)	t_{REC}	—	—	20	µs
M7	P	Reference Supply current 1 ATD module enabled	I_{REF}	—	—	0.375	mA
M8	P	Reference Supply current 2 ATD modules enabled	I_{REF}	—	—	0.750	mA

1 Full accuracy is not guaranteed when differential voltage is less than 4.50 V
2 Minimum time assumes final sample period of 2 ATD clocks; maximum time assumes final sample period of 16 ATD clocks.

Table 25. ATD Operating Characteristics in 3.3 V Range

Conditions shown in Table 6, with $V_{DD}X$ = 3.3 V ±10% and a temperature maximum of +140°C unless otherwise noted.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
N1	D	Reference Potential Low High	V_{RL} V_{RH}	$V_{SS}A$ $V_{DD}A \div 2$	— —	$V_{DD}A \div 2$ $V_{DD}A$	V V
N2	C	Differential Reference Voltage [1]	$V_{RH}–V_{RL}$	3.0	3.3	3.6	V
N3	D	ATD Clock Frequency	f_{ATDCLK}	0.5	—	2.0	MHz
N4	D	ATD 10-bit Conversion PeriodClock Cycles [2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	N_{CONV10} T_{CONV10}	14 7	— —	28 14	Cycles µs
N5	D	ATD 8-bit Conversion PeriodClock Cycles [2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	N_{CONV8} T_{CONV8}	12 6	— —	26 13	Cycles µs
N6	D	Recovery Time ($V_{DD}A$=5.0 V)	t_{REC}	—	—	20	µs
N7	P	Reference Supply current 1 ATD module enabled	I_{REF}	—	—	0.375	mA
N8	P	Reference Supply current 2 ATD modules enabled	I_{REF}	—	—	0.250	mA

1 Full accuracy is not guaranteed when differential voltage is less than 3.0 V
2 Minimum time assumes final sample period of 2 ATD clocks; maximum time assumes final sample period of 16 ATD clocks.

3.10.1 Factors Influencing Accuracy

Three factors — source resistance, source capacitance and current injection — have an influence on the accuracy of the ATD.

3.10.1.1 Source Resistance

Due to the input pin leakage current as specified in Table 15 in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum specified source resistance R_S, results in an error of less than 1/2 LSB (2.5 mV) at the maximum leakage current. If the device or operating conditions are less than the worst case, or leakage-induced errors are acceptable, larger values of source resistance are allowed.

3.10.1.2 Source Capacitance

When sampling, an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external capacitance and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1 LSB, then the external filter capacitor must be calculated as, $C_f \geq 1024 \times (C_{INS} - C_{INN})$.

3.10.1.3 Current Injection

There are two cases to consider:

1. A current is injected into the channel being converted. The channel being stressed has conversion values of 0x3FF (0xFF in 8-bit mode) for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance. The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K \times R_S \times I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table 26. ATD Electrical Characteristics

Conditions are shown in Table 6 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
P1	C	Max input Source Resistance	R_S	—	—	1	KΩ
P2	T	Total Input Capacitance Non Sampling Sampling	 C_{INN} C_{INS}	 — —	 — —	 10 22	 pF pF
P3	C	Disruptive Analog Input Current	I_{NA}	–2.5	—	2.5	mA
P4	C	Coupling Ratio positive current injection	K_p	—	—	TBD	A/A
P5	C	Coupling Ratio negative current injection	K_n	—	—	TBD	A/A

3.10.2 ATD Accuracy

Table 27 and Table 28 specify the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table 27. ATD Conversion Performance in 5 V Range

Conditions shown in Table 6 unless otherwise noted. $V_{REF} = V_{RH} - V_{RL} = 5.12$ V, resulting in one 8 bit count = 20 mV and one 10 bit count = 5 mV $f_{ATDCLK} = 2.0$ MHz, $4.5\ V \le V_{DD}A \le 5.5$ V							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Q1	P	10-bit Resolution	LSB	—	5	—	mV
Q2	P	10-bit Differential Nonlinearity	DNL	–1	—	1	Counts
Q3	P	10-bit Integral Nonlinearity	INL	–2.5	±1.5	2.5	Counts
Q4	P	10-bit Absolute Error [1]	AE	–3	±2.0	3	Counts
Q5	P	8-bit Resolution	LSB	—	20	—	mV
Q6	P	8-bit Differential Nonlinearity	DNL	–0.5	—	0.5	Counts
Q7	P	8-bit Integral Nonlinearity	INL	–1.0	±0.5	1.0	Counts
Q8	P	8-bit Absolute Error [1]	AE	–1.5	±1.0	1.5	Counts

[1] These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table 28. ATD Conversion Performance in 3.3 V Range

Conditions shown in Table 6 unless otherwise noted. $V_{REF} = V_{RH} - V_{RL} = 5.12$ V, resulting in one 8 bit count = 20 mV and one 10 bit count = 5 mV $f_{ATDCLK} = 2.0$ MHz, $4.5\ V \le V_{DD}A \le 5.5$ V							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
R1	P	10-bit Resolution	LSB	—	3.25	—	mV
R2	P	10-bit Differential Nonlinearity	DNL	–1.5	—	1.5	Counts
R3	P	10-bit Integral Nonlinearity	INL	–3.5	±1.5	3.5	Counts
R4	P	10-bit Absolute Error [1]	AE	–5	±2.0	5	Counts
R5	P	8-bit Resolution	LSB	—	13	—	mV
R6	P	8-bit Differential Nonlinearity	DNL	–0.5	—	0.5	Counts
R7	P	8-bit Integral Nonlinearity	INL	–1.5	±1.0	1.5	Counts
R8	P	8-bit Absolute Error [1]	AE	–1.5	±1.0	1.5	Counts

[1] These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also Figure 8.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1\ LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1\ LSB} - n$$

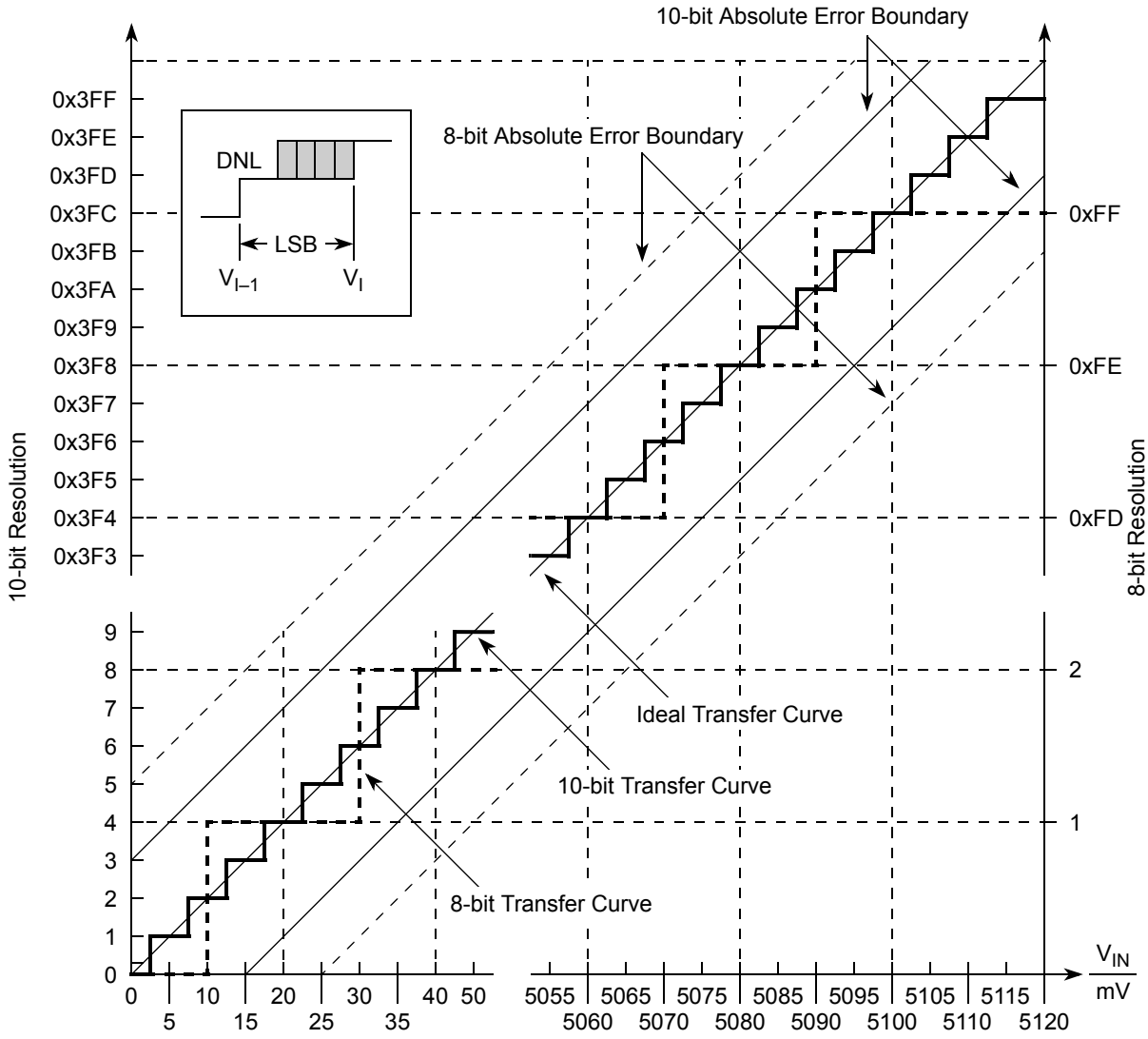


Figure 9. ATD Accuracy Definitions

NOTE

Figure 8 shows only definitions, for specification values refer to Table 27.

3.10.3 ATD Electrical Specifications

Table 29 lists the DC electrical characteristics for the ATD module. Table 27 lists the analog-to-digital conversion performance specifications.

Table 29. ATD Electrical Characteristics (Operating) [1]

Num	C	Rating			Symbol	Min	Typ	Max	Unit
S1		Reference Potential [2] Low			V_{RL}	$V_{SS}A$	—	$V_{DD}A \div 2$	V
S2			High		V_{RH}	$V_{DD}A \div 2$	—	$V_{DD}A$	V
S3		Voltage Difference $V_{RH} - V_{RL}$ [3]			$V_{RH} - V_{RL}$	4.5	—	5.5	V
S4		Analog Input Voltage			V_{INDC}	–0.3	—	$V_{DD}A + 0.3$	V
S5		Digital Input	High		V_{IH}	$0.7 \times V_{DD}A$	—	$V_{DD}A + 0.3$	V
S6		Voltage	Low		V_{IL}	$V_{SS}A - 0.3$	—	$0.2 \times V_{DD}A$	V
S7		Analog Supply Current	Run	–40°C	$I_{DD}A_{run}$	—	TBD	TBD	mA
				25°C		—	TBD	TBD	mA
				85°C [4]		—	TBD	TBD	mA
				105°C [4]		—	TBD	TBD	mA
				125°C [4]		—	TBD	TBD	mA
S8			Pseudo Stop	–40°C	$I_{DD}A_{pseudo\_stop}$	—	TBD	TBD	µA
				25°C		—	17	TBD	µA
				85°C [4]		—	TBD	TBD	µA
				105°C [4]		—	TBD	TBD	µA
				125°C [4]		—	TBD	TBD	µA
S9			Stop (low power)	–40°C	$I_{DD}A_{stop}$	—	TBD	TBD	µA
				25°C		—	17	TBD	µA
				85°C [4]		—	TBD	TBD	µA
				105°C [4]		—	TBD	TBD	µA
				125°C [4]		—	TBD	TBD	µA
S10		Reference Supply Current			I_{REF}	—	200	250	µA
S11		Input Injection Current [5]			I_{INJ}	—	—	2	mA
S12		Input Current, Off Channel [6]			I_{OFF}	–200	—	200	nA
S13		Total Input Capacitance	Not Sampling		C_{INN}	—	—	10	pF
S14			Sampling		C_{INS}	—	—	15	pF
S15		Disruptive Analog Input Current [7]			I_{NA}	–3	—	3	mA
S16		Coupling Ratio [8]			K	—	—	10^{-4}	A/A
S17		Incremental Error due to injection current (All channels with 10k < Rs < 100k) [9]				—	—	±1	Counts
S18		Incremental Error due to injection current (Channel under test Rs=10k, I_{INJ}=±3mA) [9]				—	—	±1	Counts
S19		Incremental Capacitance during Sampling [10]			C_{SAMP}	—	—	5	pF

1 All voltages referred to $V_{SS}A$, –40 to 125°C, $V_{DD}A$ = 5.0 V ±10% and 2.0 MHz conversion rate unless otherwise noted. Refer to Table 6 for additional operating conditions.

2 To obtain full-scale, full-range results, $V_{SS}A < V_{RL} < V_{INDC} < V_{RH} < V_{DD}A$. Sample buffer amp cannot drive beyond the power supply levels. If the input level goes outside of this range, it will effectively be clipped.

3 Full accuracy is not guaranteed when the differential reference voltage is less than 4.5 V.

4 85°C, 105°C, and 125°C refer to the "C", "V", and "M" Temperature Options, respectively.

5 The input injection current is specified to 1 count of error.

6 Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C.

7 Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL}. This assumes that $V_{DD}A \geq AV_{RH}$ and $V_{RL} \geq V_{SS}A$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

8 Coupling Ratio, K, is defined as the ratio of the output current, I_{OUT}, measured on the pin under test to the injection current, I_{INJ}, when both adjacent pins are overstressed with the specified injection current. $K = I_{OUT} \div I_{INJ}$. The input voltage error on the channel under test is calculated as $Verr = I_{INJ} \times K \times R_S$.

9 Total injection current is determined by the number of channels injecting (for example, 15), external injection voltage ($V_{INJ} - V_{POSCLAMP}$, or $V_{INJ} - V_{NEGCLAMP}$), and the external source impedance, Rs, wherein all input channels have the same values. To determine the error voltage on the converted channel, only the two adjacent channels are expected to contribute to the error voltage: $V_{errj} = (V_{INJ} - V_{CLAMP}) \times K \times 2$.

10 For a maximum sampling error of the input voltage ≤ 1LSB, then the external filter capacitor, $C_f \geq 1024 \times C_{SAMP}$. The value of C_{SAMP} in the new design may be reduced, or increased slightly.

Table 30. ATD Performance Specifications [1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
T1	D	10-bit Resolution	LSB	—	5	—	mV
T2	D	10-bit Differential Nonlinearity [2]	DNL	–1	—	1	Counts
T3	D	10-bit Integral Nonlinearity [2]	INL	–2	—	2	Counts
T4	D	10-bit Absolute Error [2, 3]	AE	–2.5	—	2.5	Counts
T5	D	Max input Source Impedance [4]	R_S	—	—	100	kΩ

1 All voltages referred to $V_{SS}A$, $V_{DD}A$ = 5.0 V±10%, ATD clock = 2.1 Mhz., –40 to 125 °C.

2 Note: 1 LSB = 1 Count (At V_{REF} = 5.12 V, one 8 bit count = 20 mV, one 10-bit count = 5 mV)

3 These values include quantization error which is inherently 1/2 count for any A/D converter.

4 This value is based on error attributed to the specified leakage value of TBD nA resulting in an error of less than 1/2 LSB (2.5 mV). If operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowable.

3.10.4 ATD Timing Specifications

Table 31. ATD Timing Specifications

Num	C	Rating	Symbol	Min	Typ	Max	Unit
U1	D	ATD Module Clock Frequency	F_{clk}	—	—	25.0	MHz
U2	D	ATD Conversion Clock Frequency	F_{atdclk}	0.5	—	2.0	MHz
U3	D	ATD 10-bit Conversion Period Clock Cycles Conv. Time	N_{CONV10} T_{CONV10}	14 7	— —	28 14	Cycles µsec
U4	D	Stop Recovery Time ($V_{DD}A$ = 5.0 V)	T_{SR}	—	—	100	µsec

Table 32. ATD External Trigger Timing Specifications

Num	C	Parameter	Symbol	Min	Max	Unit
V1	D	ETRIG Minimum Period	T_{PERIOD}	—	1 sample + 1 conv. + 1 ATD clock	CYCLE
V2	D	ETRIG Minimum Pulse Width	t_{PW}	2	—	SYS CLK
V3	D	ETRIG Level Recovery [1]	t_{LR}	1	—	SYS CLK
V4	D	Conversion Start Delay	t_{DLY}	—	2	SYS CLK

1 Time prior to end of conversion that the ETRIG pin must be deactivated so that another conversion sequence does not start.

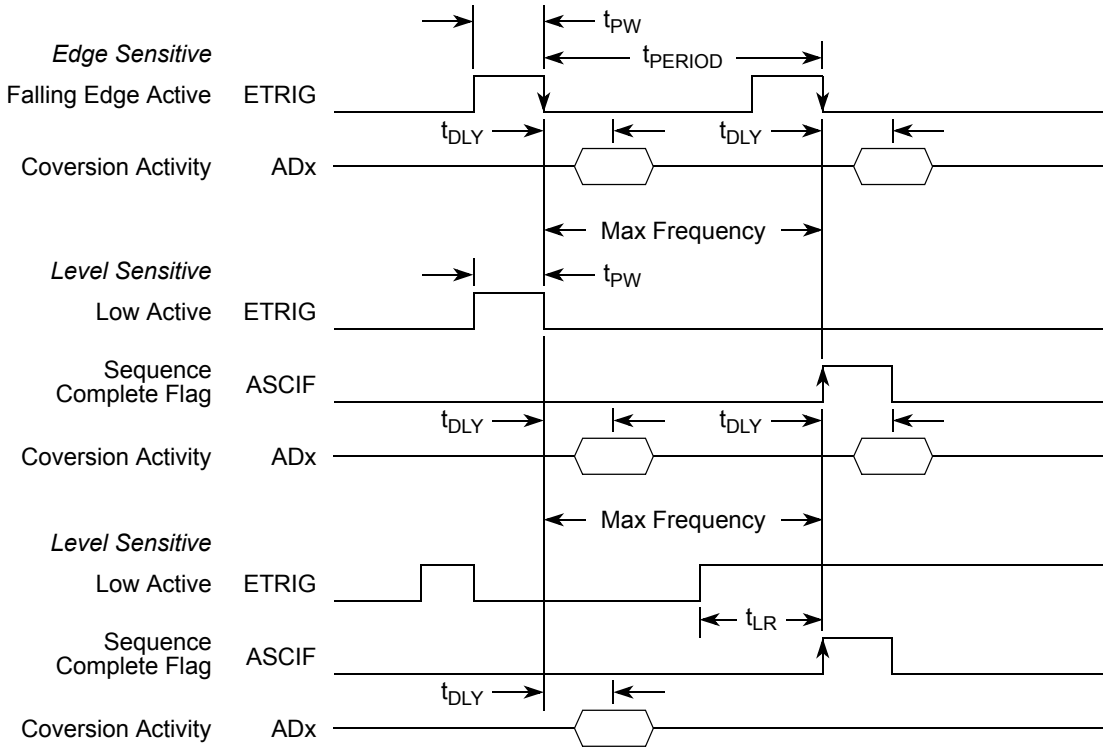


Figure 10. ATD External Trigger Timing Diagram

3.11 Serial Peripheral Interface Electrical Specifications

3.11.1 Master Mode

Figure 11 and Figure 12 illustrate master mode timing. Timing values are shown in Table 33.

Table 33. SPI Master Mode Timing Characteristics [1]

Conditions are shown in Table 6 unless otherwise noted, C_{LOAD} = 200pF on all outputs							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
W1a	P	Operating Frequency	f_{op}	DC	—	1/4	f_{bus}
W1b	P	SCK Period $t_{sck} = 1/f_{op}$	t_{sck}	4	—	2048	t_{bus}
W2	D	Enable Lead Time	t_{lead}	1/2	—	—	t_{sck}
W3	D	Enable Lag Time	t_{lag}	1/2	—	—	t_{sck}
W4	D	Clock (SCK) High or Low Time	t_{wsck}	t_{bus} – 30	—	1024 t_{bus}	ns
W5	D	Data Setup Time (Inputs)	t_{su}	25	—	—	ns
W6	D	Data Hold Time (Inputs)	t_{hi}	0	—	—	ns
W9	D	Data Valid (after Enable Edge)	t_v	—	—	25	ns
W10	D	Data Hold Time (Outputs)	t_{ho}	0	—	—	ns
W11	D	Rise Time Inputs and Outputs	t_r	—	—	25	ns
W12	D	Fall Time Inputs and Outputs	t_f	—	—	25	ns

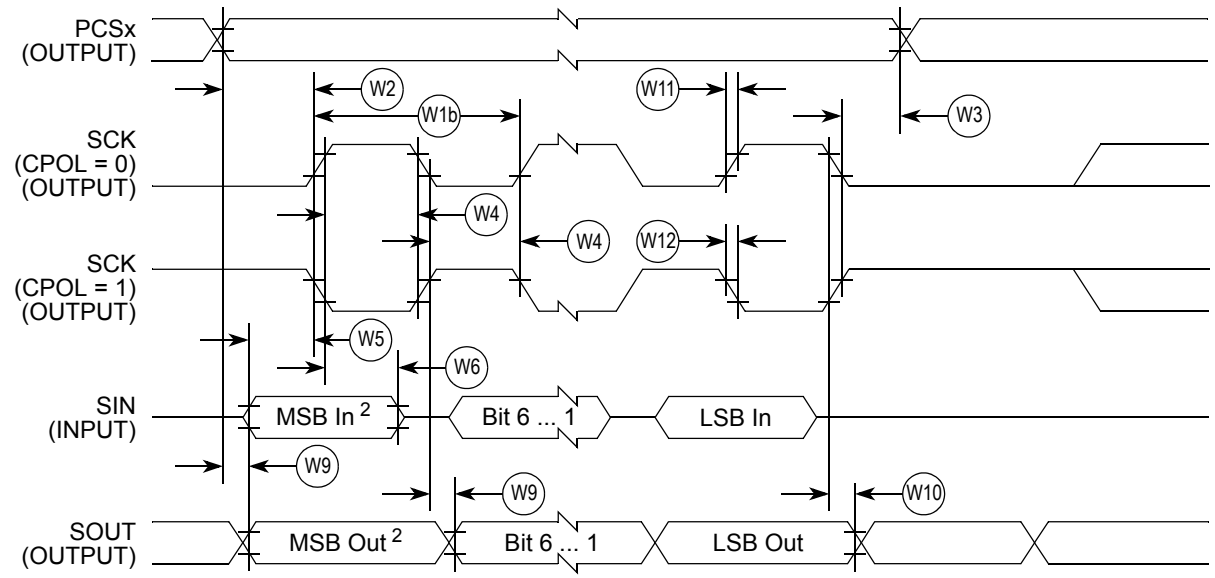
[1] The numbers 7, 8 in the column labeled “Num” are missing. This has been done on purpose to be consistent between the Master and the Slave timing shown in Table 34.

3.11.2 Slave Mode

Figure 13 and Figure 14 illustrate the slave mode timing. Timing values are shown in Table 34.

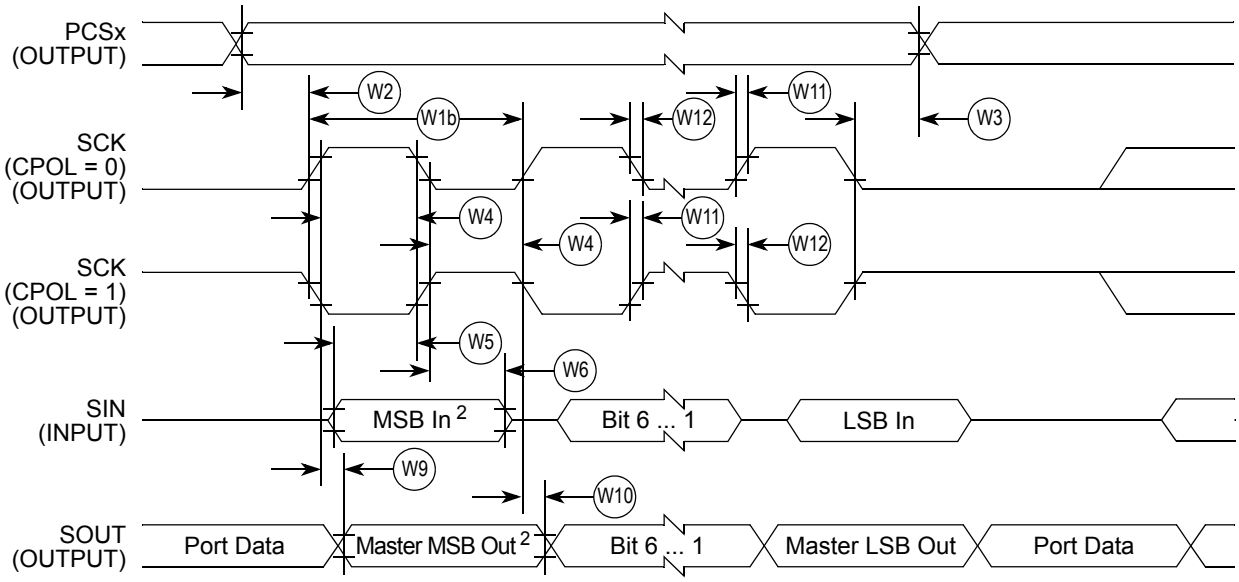
Table 34. SPI Slave Mode Timing Characteristics

Conditions are shown in Table 6 unless otherwise noted, CLOAD = 200pF on all outputs							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
X1a	P	Operating Frequency	f_{op}	DC	—	1/4	f_{bus}
X1b	P	SCK Period $t_{sck} = 1/f_{op}$	t_{sck}	4	—	2048	t_{bus}
X2	D	Enable Lead Time	t_{lead}	1	—	—	t_{cyc}
X3	D	Enable Lag Time	t_{lag}	1	—	—	t_{cyc}
X4	D	Clock (SCK) High or Low Time	t_{wsck}	t_{cyc} – 30	—	—	ns
X5	D	Data Setup Time (Inputs)	t_{su}	25	—	—	ns
X6	D	Data Hold Time (Inputs)	t_{hi}	25	—	—	ns
X7	D	Slave Access Time	t_a	—	—	1	t_{cyc}
X8	D	Slave SIN Disable Time	t_{dis}	—	—	1	t_{cyc}
X9	D	Data Valid (after SCK Edge)	t_v	—	—	25	ns
X10	D	Data Hold Time (Outputs)	t_{ho}	0	—	—	ns
X11	D	Rise Time Inputs and Outputs	t_r	—	—	25	ns
X12	D	Fall Time Inputs and Outputs	t_f	—	—	25	ns



1 If configured as output.
2 LSBFE = 0. For LSBFE = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 11. SPI Master Timing (CPHA = 0)



1 If configured as output.
2 LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. SPI Master Timing (CPHA =1)

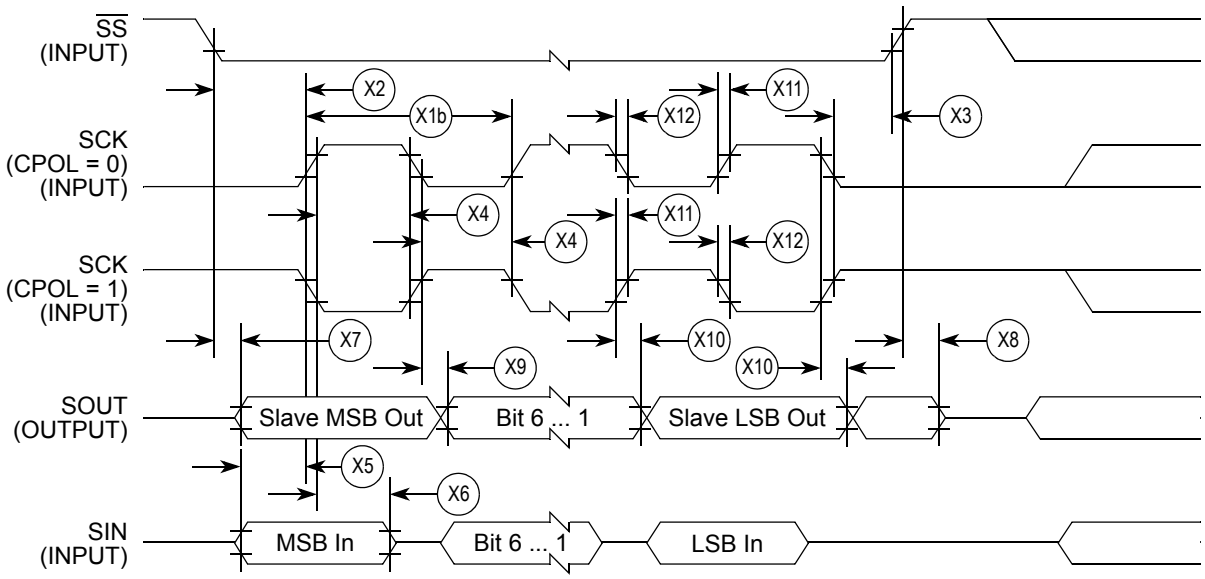


Figure 13. SPI Slave Timing (CPHA = 0)

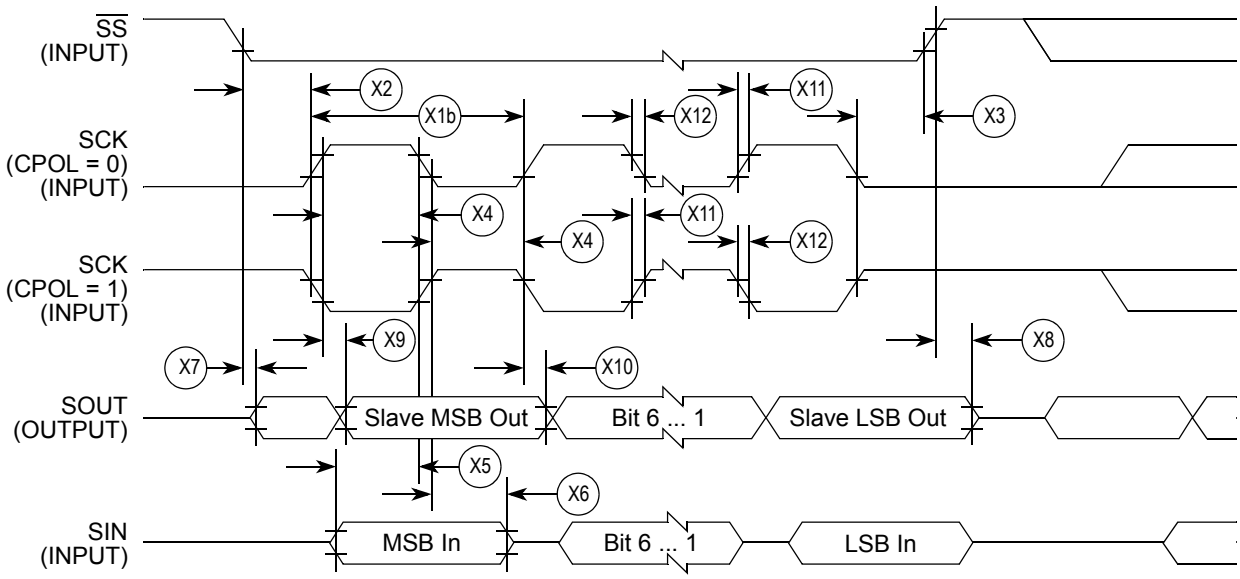


Figure 14. SPI Slave Timing (CPHA =1)

3.12 FlexCAN Electrical Specifications

Table 35. FlexCAN Wake-up Pulse Characteristics

Conditions are shown in Table 6 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Y1	P	FlexCAN Wake-up dominant pulse filtered	t_{WUP}	—	—	2	µs
Y2	P	FlexCAN Wake-up dominant pulse passed	t_{WUP}	5	—	—	µs

3.13 Program Flash and Data Flash Timing Characteristics

NOTE

Unless otherwise noted the abbreviation NVM (Non-Volatile Memory) is used for both program Flash and data Flash.

3.13.1 NVM timing

The time base for all NVM program or erase operations is derived from the system clock divided by two (Fsys/2). A minimum system frequency $f_{NVMfsys}$ is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and Data Flash program and erase operations are timed using a clock derived from the system frequency using the CFMCLKD register. The frequency of this clock must be set within the limits specified as f_{NVMOP}. The minimum program and erase times shown in Table 36 are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2 MHz.

3.13.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

3.13.1.2 Burst Programming

This applies only to the Flash where up to 32 words in a row can be programmed consecutively using burst programming by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 31 \cdot t_{bwpgm}$$

Burst programming is more than 2 times faster than single word programming.

3.13.1.3 Sector Erase

Erasing a 4k byte Flash sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

3.13.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

3.13.1.5 Blank Check

The time it takes to perform a blank check on the Flash or Data Flash is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table 36. NVM Timing Characteristics [1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
Z1	D	System Clock/2	$f_{NVMfsys}$	0.5	—	50 [2]	MHz
Z2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1	—	—	MHz
Z3	D	Operating Frequency	f_{NVMOP}	150	—	200	kHz
Z4	P	Single Word Programming Time	t_{swpgm}	46 [3]	—	74.5 [4]	µs
Z5	D	Flash Burst Programming consecutive word	t_{bwpgm}	20.4 [3]	—	31 [4]	µs
Z6	D	Flash Burst Programming Time for 32 Words	t_{brpgm}	678.4 [3]	—	1035.5 [4]	µs
Z7	P	Sector Erase Time	t_{era}	20 [5]	—	26.7 [4]	ms
Z8	P	Mass Erase Time	t_{mass}	100 [5]	—	133 [4]	ms
Z9	D	Blank Check Time Flash per block	t_{check}	11 [6]	—	32778 [7]	t_{cyc}
Z10	D	Blank Check Time Data Flash per block	t_{check}	11 [6]	—	2058 [7]	t_{cyc}

1 Conditions are shown in Table 6 unless otherwise noted
2 Restrictions for oscillator in crystal mode apply!
3 Minimum programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.
4 Maximum erase and programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formulae in Section 3.13.1.1, “Single Word Programming,” through Section 3.13.1.4, “Mass Erase,” for more information.
5 Minimum erase times are achieved under maximum NVM operating frequency f_{NVMOP}.
6 Minimum time, if first word in the array is not blank
7 Maximum time to complete check on an erased block

3.13.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures. The failure rates for data retention and program/erase cycling are specified at the operating conditions noted. The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

Table 37. NVM Reliability Characteristics

Conditions shown in Table 6 unless otherwise noted.				
Num	**C**	**Rating**	**Min**	**Unit**
Z10	C	Program/Data Flash Program/Erase endurance (–40C to +125C)	10,000	Cycles
Z11	C	Program/Data Flash Data Retention Lifetime	15	Years

NOTE

All values shown in Table 37 are target values and subject to characterization.

For Flash cycling performance, each Program operation must be preceded by an erase.

4 Device Pin Assignments

The MAC7100 Family is available in 208-pin ball grid array (MAP BGA), 144-pin low profile quad flat (LQFP), 112-pin LQFP, and 100-pin LQFP package options. The family of devices offer pin-compatible packaged devices to assist with system development and accommodate a direct application enhancement path. Refer to Table 1 for a comparison of the peripheral sets and package options for each device.

Most pins perform two or more functions, which is described in more detail in the *MAC7100 Microcontroller Family Reference Manual* (MAC7100RM/D). Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19 show the pin assignments for the various packages.

4.1 MAC7141PV Pin Assignments

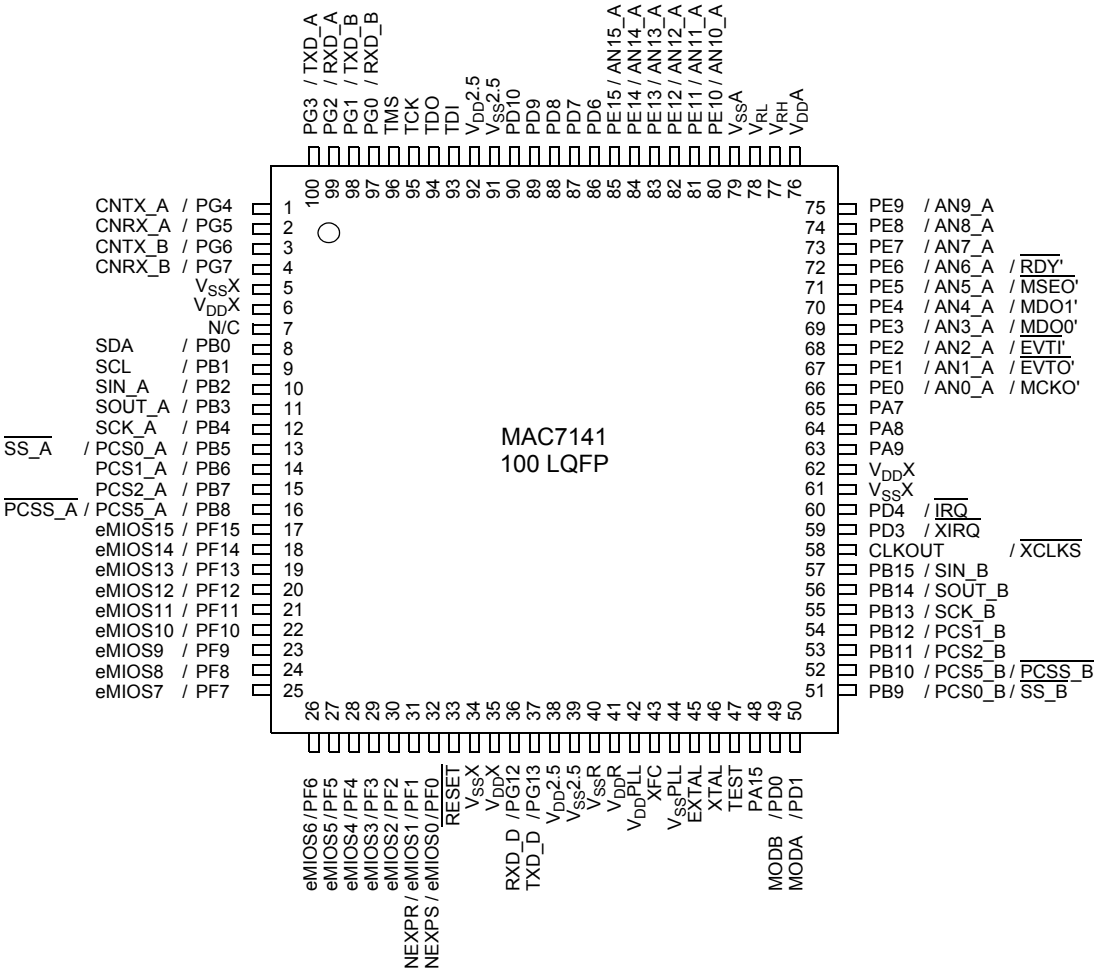


Figure 15. Pin Assignments for MAC7141 in 100-pin LQFP

4.2 MAC7121PV Pin Assignments

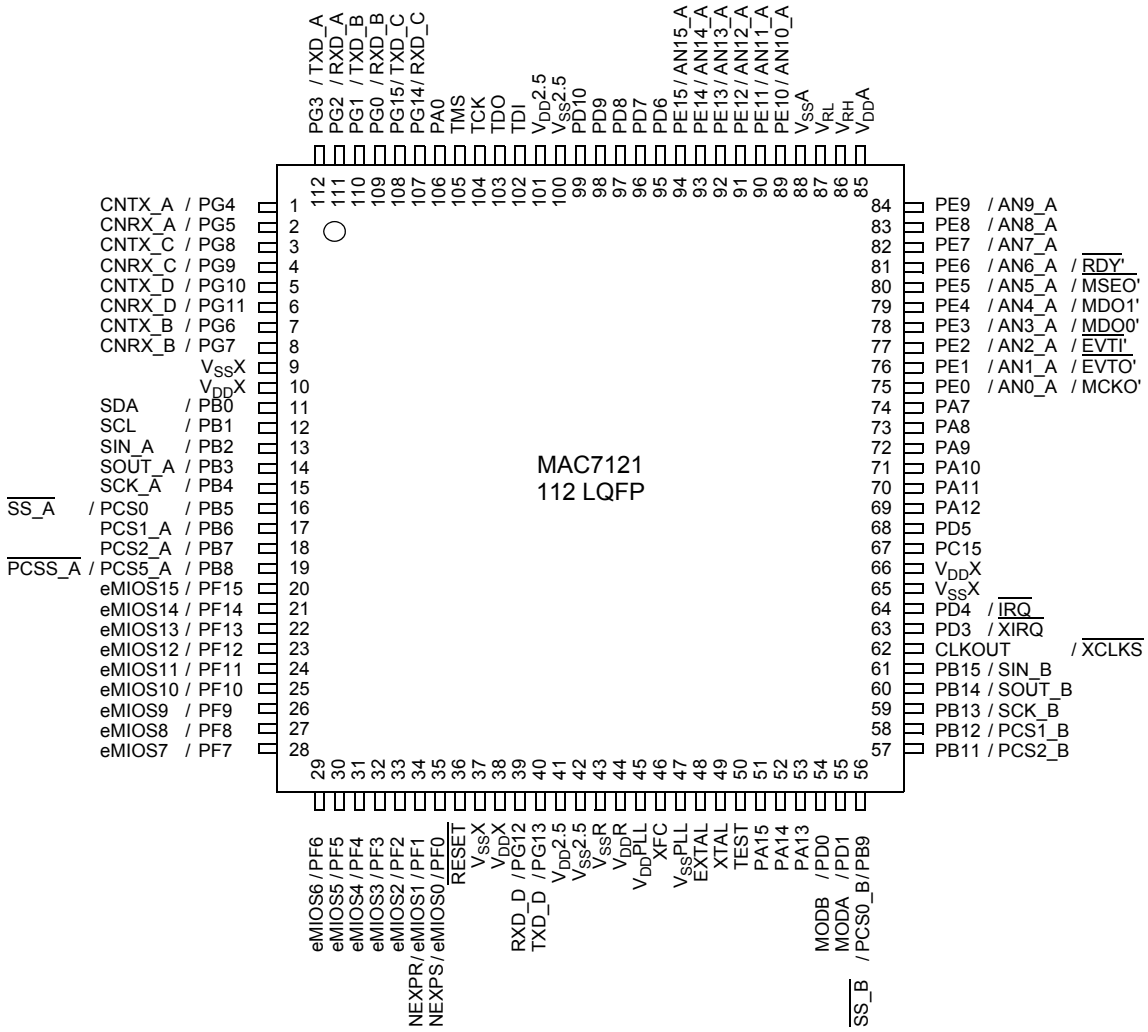


Figure 16. Pin Assignments for MAC7121 in 112-pin LQFP

4.3 MAC7101PV Pin Assignments

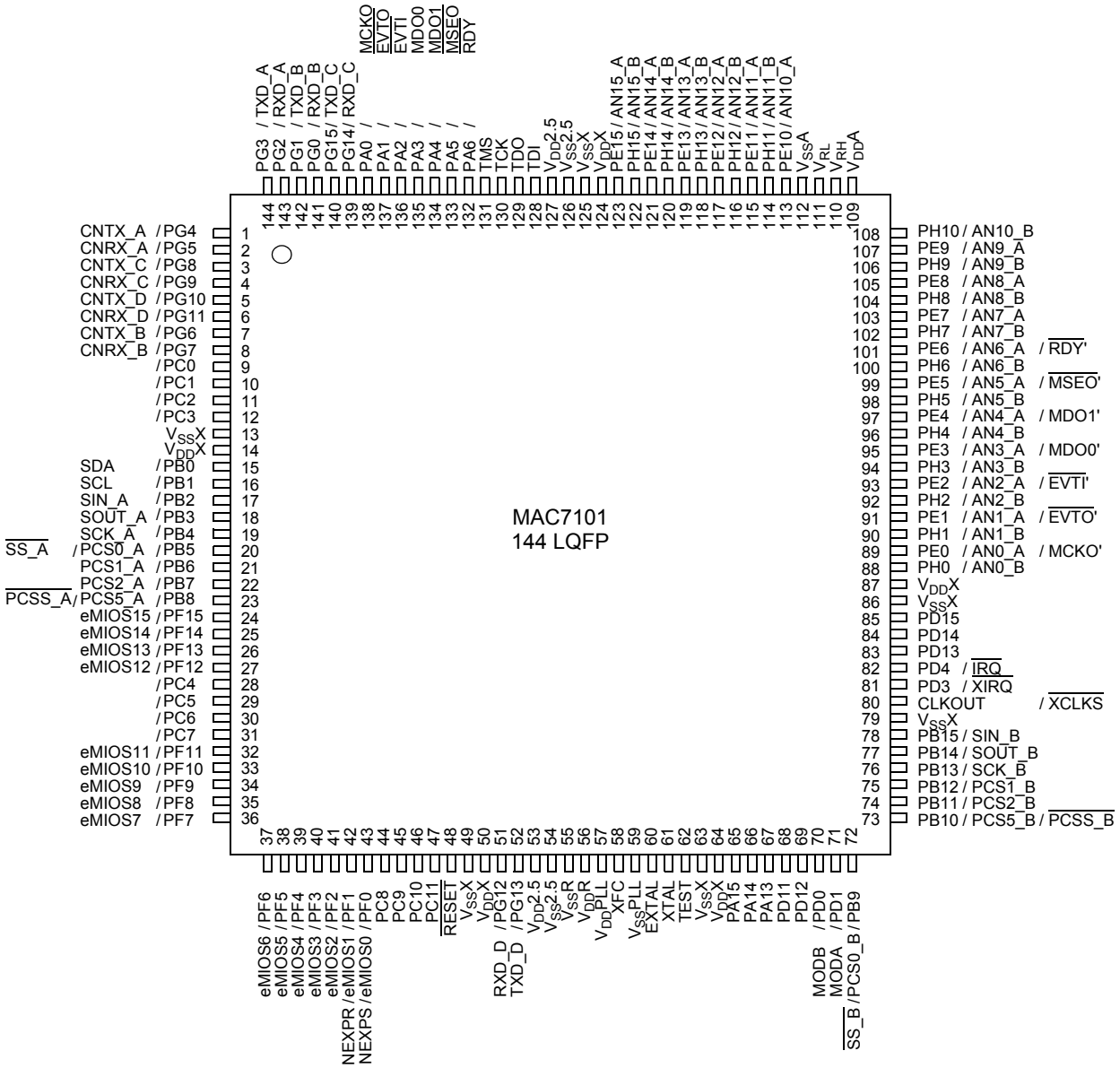


Figure 17. Pin Assignments for MAC7101 in 144-pin LQFP

4.4 MAC7111PV Pin Assignments

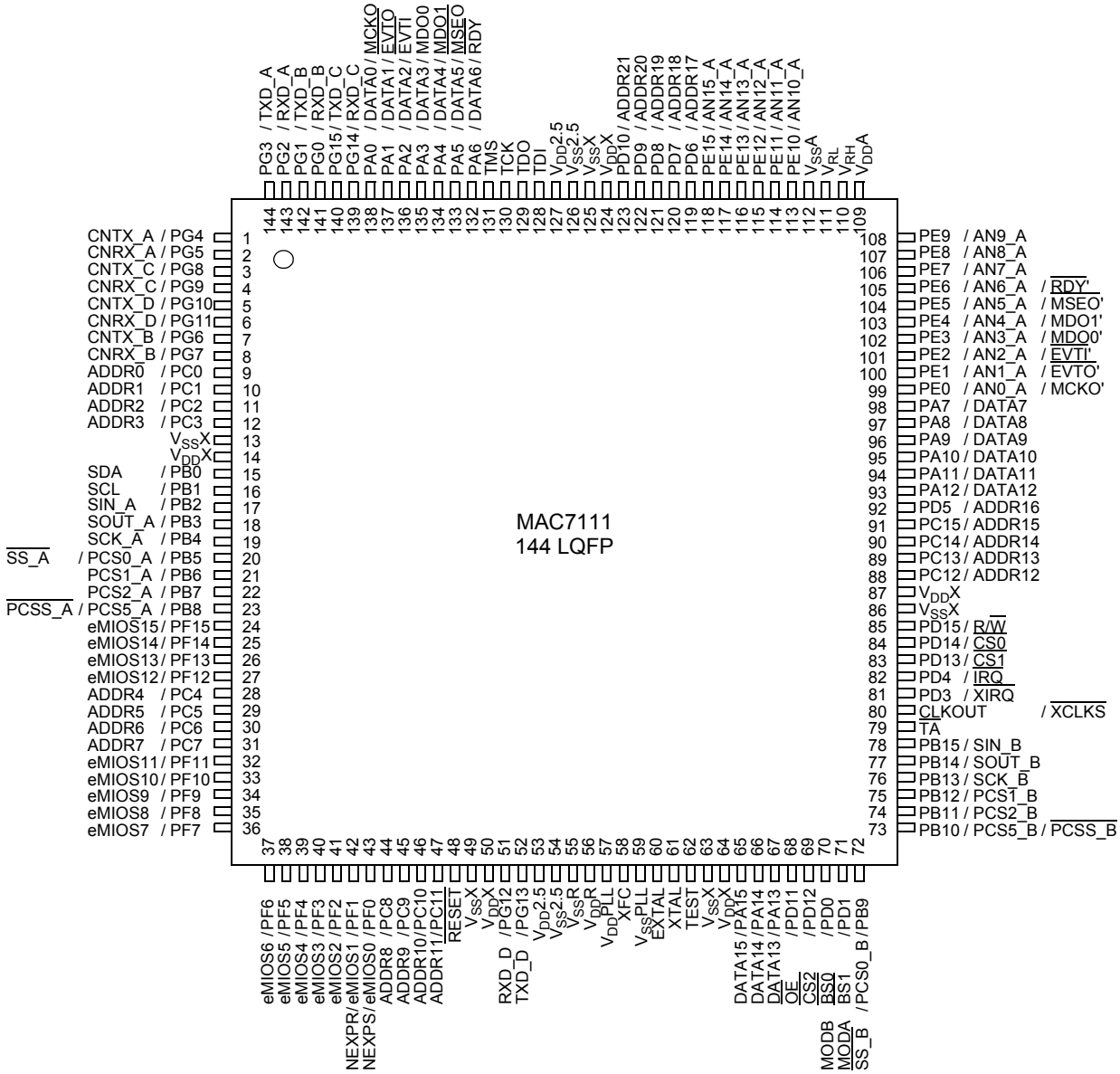


Figure 18. Pin Assignments for MAC7111 in 144-pin LQFP

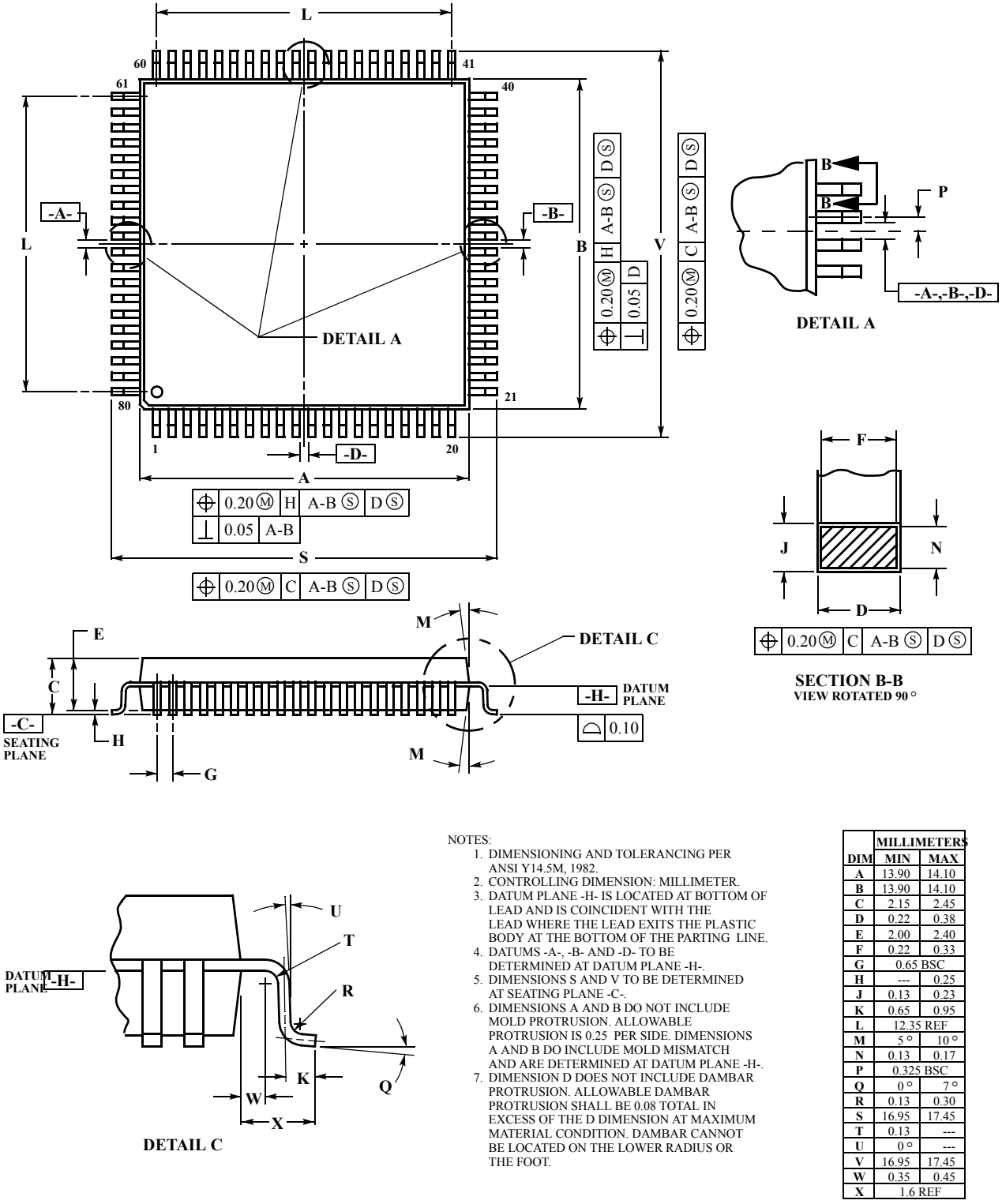
4.5 MAC7131VF Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	V_{SS}X	V_{SS}X	PG0	PG14	PA2	PA5	TCLK	TDI	PE15	PE14	PH14	PE12	PH11	V_{RL}	V_{RH}	V_{DD}A
B	V_{SS}X	V_{SS}X	PG2	PG15	PA0	PA4	TMS	TDO	PD9	PH15	PE13	PH12	PE10	PH9	V_{DD}A	PH8
C	PG5	PG3	V_{SS}X	PG1	PA1	PA3	PA6	V_{SS}2.5	V_{DD}X	PD6	PH13	PE11	V_{DD}A	PE8	PE7	PH7
D	PG9	PG8	PG4	V_{SS}X	V_{SS}X	V_{SS}2.5	V_{SS}2.5	PD10	PD8	PD7	V_{SS}A	V_{SS}A	PH10	PE9	PE6	PH6
E	PG6	PG11	PG10	V_{SS}X									PE4	PE5	PH5	PH4
F	PC0	PG7	PC1	V_{SS}X									PE2	PE3	PH3	PH2
G	PB0	PC2	PC3	V_{SS}X			V_{SS}X	V_{SS}X	V_{SS}X	V_{SS}X			PH0	PH1	PE1	PE0
H	PB3	PB2	PB1	V_{DD}X			V_{SS}X	V_{SS}X	V_{SS}X	V_{SS}X			PA8	PA9	PA7	PA10
J	PB5	PB6	PB4	V_{SS}X			V_{SS}X	V_{SS}X	V_{SS}X	V_{SS}X			PD5	PA12	PA11	PC15
K	PB7	PB8	PF15	V_{SS}X			V_{SS}X	V_{SS}X	V_{SS}X	V_{SS}X			PC13	PC12	PC14	V_{DD}X
L	PF14	PF13	PC4	V_{SS}X									PD13	PD14	PD15	PD4
M	PF12	PC5	PC6	V_{SS}X									V_{SS}X	$\overline{TA}$	PD3	CLKOUT
N	PF11	PF10	PC7	V_{SS}X	V_{SS}R	V_{SS}R	V_{SS}2.5	V_{SS}2.5	V_{SS}PLL	V_{SS}PLL	V_{SS}X	V_{SS}X	V_{SS}X	PB11	PB14	PB15
P	PF9	PF8	V_{SS}X	PF5	PC8	PC10	V_{DD}X	V_{SS}2.5	V_{DD}R	V_{DD}X	PA15	PD11	PD12	V_{SS}X	PB12	PB13
R	PF7	V_{SS}X	PF6	PF3	PF1	PC9	PG12	PG13	V_{SS}X	V_{SS}X	TEST	PA13	PD1	PB10	V_{SS}X	V_{SS}X
T	V_{SS}X	V_{SS}X	PF4	PF2	PF0	PC11	$\overline{RESET}$	V_{SS}PLL	XFC	EXTAL	XTAL	PA14	PD0	PB9	V_{SS}X	V_{SS}X

Figure 19. Pin Assignments for MAC7131 in 208-pin MAP BGA

5 Mechanical Information

5.1 100-Pin LQFP Package

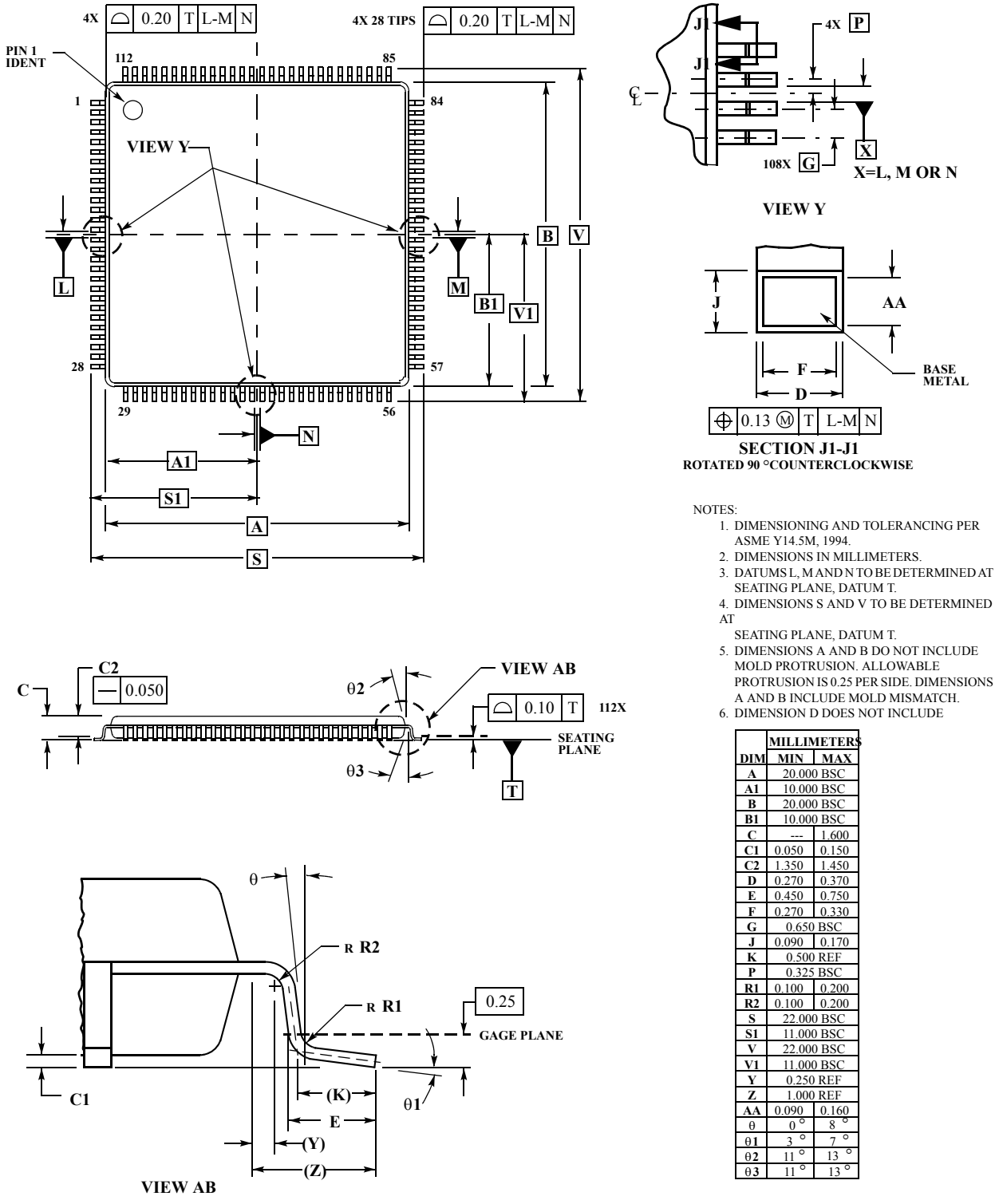


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure 20. 100-Pin LQFP Mechanical Dimensions (Case No. 983)

5.2 112-Pin LQFP Package

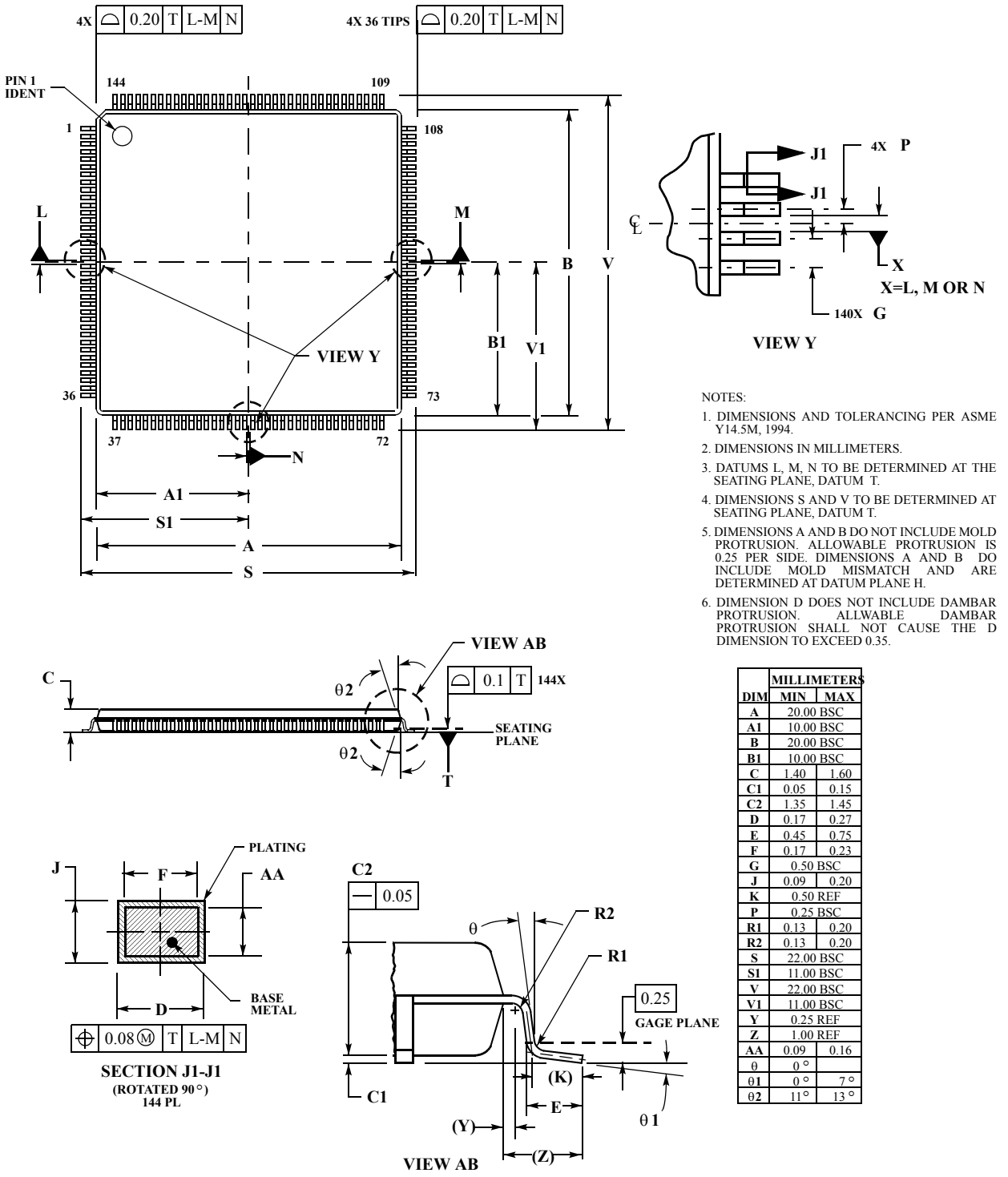


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0 °	8 °
θ1	3 °	7 °
θ2	11 °	13 °
θ3	11 °	13 °

Figure 21. 112-Pin LQFP Mechanical Dimensions (Case No. 987)

5.3 144-Pin LQFP Package



DIM	MILLIMETERS MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0 °	
θ1	0 °	7 °
θ2	11°	13 °

Figure 22. 144-Pin LQFP Mechanical Dimensions (Case No. 918)

5.4 208-Pin MAP BGA Package

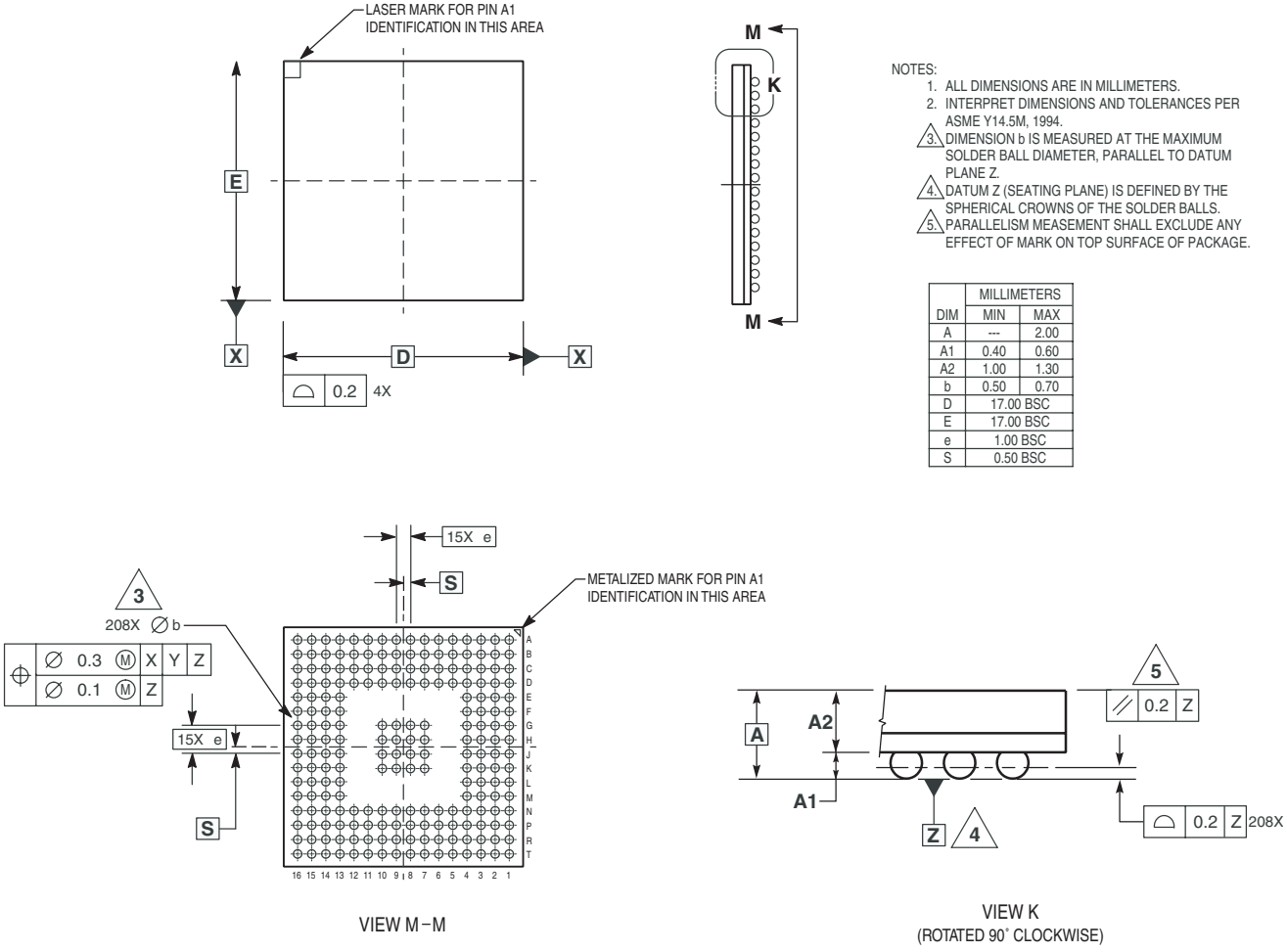


Figure 23. 208-Pin MAP BGA Mechanical Dimensions (Case No. 1159A-01)

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