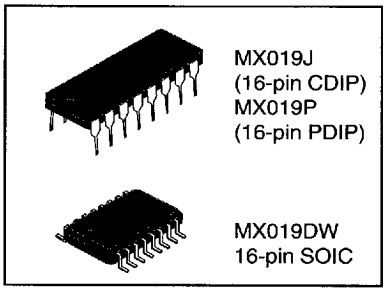
Preliminary Information

QUAD DIGITAL CONTROL AMPLIFIER

Features

- **4 Digitally Controlled Amplifiers**
- **15 Gain/Attenuation Steps**
- **3 Amplifiers with a ± 3dB Range in 0.43dB Steps**
- **1 'Volume' Amplifier with a ± 14dB Range in 2dB Steps**
- **8-Bit Serial Data Control**
- **Output Mute Function**
- **Audio and Data Gain Control Applications**
- **Telecommunications, Radio and Industrial Applications**



MX019J
(16-pin CDIP)
MX019P
(16-pin PDIP)

MX019DW
16-pin SOIC

DESCRIPTION

The MX019 Digitally Adjustable Amplifier Array replaces trimmer potentiometers and volume controls in Cellular, LMR, Telephony and Communications applications where voice or data signals need adjustment.

The MX019 is a single-chip LSI consisting of four digitally controlled amplifier stages, each with 15 distinct gain/attenuation steps. Control of each individual amplifier is by an 8-bit serial data stream. Three of the amplifier stages offer a +/-3dB range in steps of 0.43dB, while the remaining amplifier offers a +/-14dB range in steps of 2dB, and is suggested for volume control applications. Each amplifier includes a 16th 'Off' state which, when applied, mutes the output audio from that channel. This array uses a Chip Select input to select one of two MX019s in a system.

This product uses the host microprocessor to digitally control the set-up of all audio levels during development, production/calibration and operation.

Applications include:

(i) Control, adjustment and set-up of communications equipment by an Intelligent ATE without manual intervention – eg. Deviation, Microphone and L/S Levels, RX Audio Level etc.

(ii) Automatic Dynamic Compensation of drift caused by variations in temperature, linearity, etc.

(iii) Fully automated servicing and re-alignment.

The MX019 is a low-power, single 5-volt CMOS device available in 16-pin CDIP, PDIP and SOIC package versions.

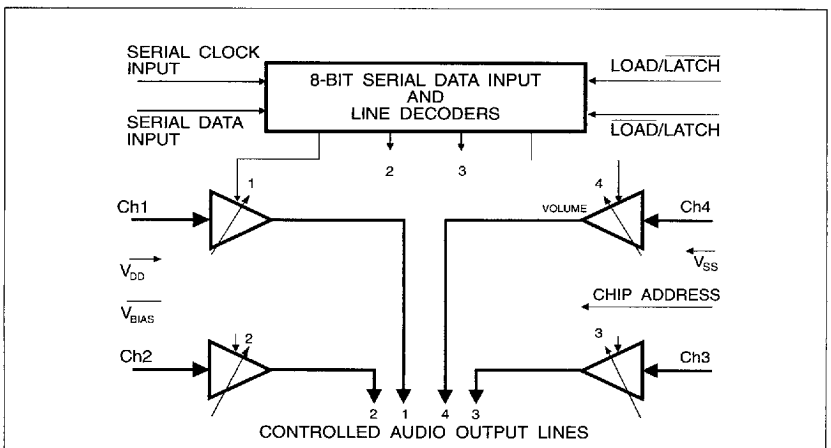
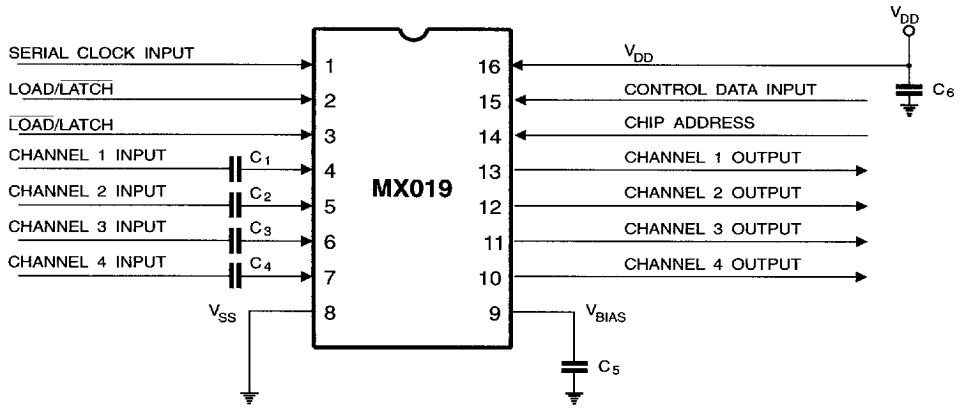


Figure 1 - Functional Block Diagram

PIN FUNCTION TABLE

Pin	Function
1	**Serial Clock :** This external clock pulse input is used to "clock in" the Control Data. See Figure 4, Serial Control Data Load Timing. This input has an internal 1MΩ pullup resistor.
2	**Load/Latch :** This input governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '0' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '0 - 1 - 0' to latch the new data in. Data is executed on the falling edge of the strobe. If the Load/Latch input is used this pin should be left open circuit. This input has an internal 1MΩ pullup resistor.
3	**Load/Latch :** This inverted Load/Latch input governs the loading and execution of control data. During serial data loading this input should be kept at a logical '1' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '1' - '0' - '1' to latch the new data in. Data is executed on the rising edge of the strobe. If the Load/Latch input is used this pin should be left open circuit. This input has an internal 1MΩ pulldown resistor.
4	**Ch1 Input :** **Analog Inputs :**
5	**Ch2 Input :** These individual amplifier inputs are self-biasing, a.c. input analog signals must be capacitively coupled to these pins, as shown in Figure 2. Note that amplifiers Ch1 to Ch4 are 'inverting amplifiers.'
6	**Ch3 Input :**
7	**Ch4 Input :**
8	V_{SS} : Negative supply rail (GND).
9	V_{BIAS} : The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} as shown in Figure 2.
10	**Ch4 Output :** **Controlled Analog Outputs :**
11	**Ch3 Output :** These are individual "Gain Controlled" amplifier outputs. Ch1 to Ch3 range from -3dB to +3dB in 0.43dB steps, Ch4 can be utilized as a volume control, ranging from -14dB to +14dB in 2.0dB steps. In the "OFF" mode there is no output from the selected amplifier.
12	**Ch2 Output :**
13	**Ch1 Output :**
14	**Chip Address :** A logic input to select one of two MX019 ICs in a system (see Table 1). This input has an internal 1MΩ pulldown resistor.
15	**Control Data Input :** Operation of the 4 amplifier channels (Ch1 – Ch4) is controlled by the 8 bits of data entered serially at this pin. The data is entered (bit 7 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1, 2 and Figure 4. This input has an internal 1MΩ pullup resistor.
16	V_{DD} : Positive supply rail. A single +5-volt power supply is required.



Notes

(1) Channel Amplifiers 1 to 4 are inverting amplifiers.

(2) Analog input capacitors C_1 to C_4 are only required for a.c. input signals, d.c. input signals do not require these components.

Component	Value
C_1 to C_4	0.1µF
C_5	1.0µF
C_6	1.0µF

Tolerances: C = ± 20%

Figure 2 - External Component Connections

Application Recommendations

To avoid excess noise and instability you should take note of the following:

(a) A noisy or badly regulated power supply can cause instability and/or variance of selected gains.

(b) Care should be taken on the design and layout of the printed circuit board.

(c) All external components (Figure 2) should be kept close to the MX019 package.

(d) Inputs and outputs should be shielded wherever possible.

(e) Tracks should be kept short.

(f) Analog tracks should not run parallel to digital tracks.

(g) A "Ground Plane" connected to V_{SS} will assist in eliminating external pick-up on the channel input and output pins.

(h) Do not run high-level output tracks close to low-level input tracks.

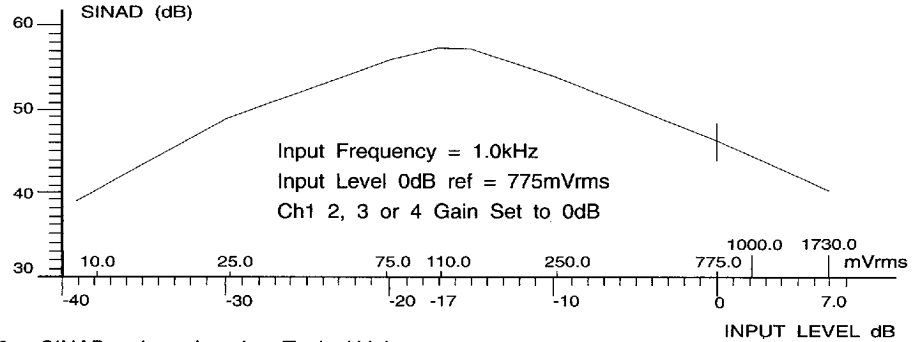


Figure 3 - SINAD vs Input Level – Typical Values

Control Data and Timing

The gain of each amplifier block (Channel 1 to Channel 4) in the MX019 is set by a separate 8-bit data word (bit 7 to bit 0). This 8-bit word, consisting of 4 Address bits (bit 7 to bit 4) and 4 Gain Control bits (bit 3 to bit 0), is loaded to the Control Data Input in serial format using the external data clock.

Table 1 Address Bits Format

Bit 7 MSB	Bit 6	Bit 5	Bit 4 LSB	Channel Address	Chip Address	Chip Number
1	0	0	0	1	0	
1	0	0	1	2	0	Chip
1	0	1	0	3	0	1
1	0	1	1	4	0	
1	1	0	0	1	1	
1	1	0	1	2	1	Chip
1	1	1	0	3	1	2
1	1	1	1	4	1	

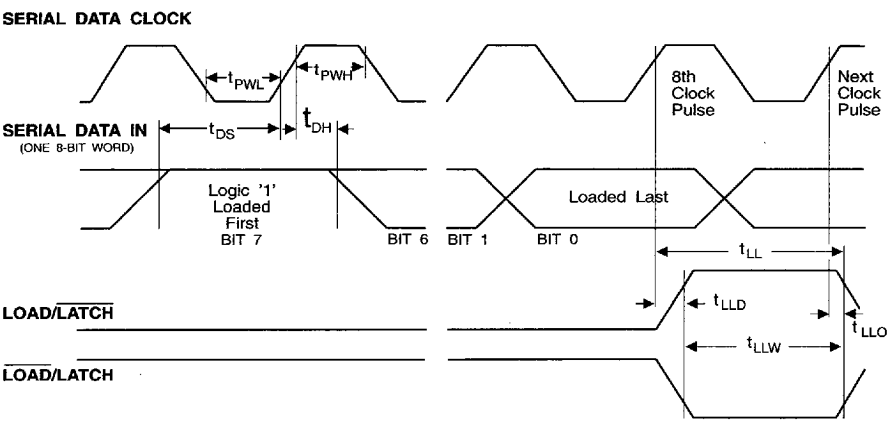
Data Loading

The 8-bit data word is loaded *bit 7 first and bit 0* last. Bit 7 must be a logic "1" to address the chip.
If bit 7 in the word is a logic "0" that 8-bit word will not be executed. The Chip Address input permits the use of two devices in a system by indicating to the chip what its address is, a "1" or a "0." Bit 6 in the address section of the control word is then used to select which device is being controlled. Figure 4 (below) shows the timing information required to load and operate this device.

Data is loaded to the MX019 on the rising edge of the Serial Clock. Loaded data is executed on the falling (rising) edge of the Load/Latch (Load/Latch) pulse. Table 1 shows the format of each 4-bit Address word, Table 2 shows the format of each Gain Control word with Figure 4 describing the data loading operation and timing.

Table 2 Gain Control Bits Format

Bit 3 MSB	Bit2	Bit 1	Bit 0 LSB	Stage 1, 2, 3 (0.43dB)	Stage 4 (2.0dB)
0	0	0	0	OFF	OFF
0	0	0	1	-3.0	-14.0dB
0	0	1	0	-2.571	-12.0
0	0	1	1	-2.143	-10.0
0	1	0	0	-1.714	-8.0
0	1	0	1	-1.286	-6.0
0	1	1	0	-0.857	-4.0
0	1	1	1	-0.428	-2.0
1	0	0	0	0	0
1	0	0	1	0.428	2.0
1	0	1	0	0.857	4.0
1	0	1	1	1.286	6.0
1	1	0	0	1.714	8.0
1	1	0	1	2.143	10.0
1	1	1	0	2.571	12.0
1	1	1	1	3.0	14.0



Timing

t_{PWH} Serial Clock "High" Pulse Width
t_{PWL} Serial Clock "Low" Pulse Width
t_{DS} Data Set-up Time
t_{DH} Data Hold Time
t_{LLD} Load/Latch Delay
t_{LL} Load/Latch Set-up Time
t_{LLW} Load/Latch Pulse Width
t_{LLO} Load/Latch Over Time

Fig.4 Serial Control Data Loading Diagram

SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Sink/Source Current	
(supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation @ T_{AMB} 25°C	800mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD}=5.0V

T_{AMB}=25°C

Audio Level 0dB ref. = 775mVrms

Amplifier Gain Set = 0dB

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage (V_{DD})			4.5	5.0	5.5	V
Supply Current			-	1.5	-	mA
Dynamic Values						
Control Functions						
Input Logic '1'			3.5	–	–	V
Input Logic '0'			–	–	1.5	V
Digital Input Impedances			0.5	1.0	–	MΩ
Amplifier Stages (General)						
Bandwidth (-3dB)			20.0	–	–	kHz
Output Impedance			–	1.0	-	kΩ
Total Harmonic Distortion		1	–	0.35	0.5	%
Output Noise Level (per stage)		2	–	180.0	400.0	µVrms
Onset of Clipping		3	–	1.73	–	Vrms
Gain Variation		4	–	–	0.1	dB
Interstage Isolation			–	60.0	–	dB
"Trimmer" Stages (Ch1 – Ch3)						
Gain			-3.0		+3.0	dB
Gain per Step (15 in No.)			–	0.43	–	dB
Step Error			–	–	0.2	dB
Input Impedance			100.0	–	–	kΩ
"Volume" Stage (Ch4)						
Gain			-14.0		+14.0	dB
Gain per Step (15 in No.)			–	2.0	–	dB
Step Error			–	–	0.4	dB
Input Impedance			50.0	–	–	kΩ
Timing (Figure 4)						
Serial Clock "High" Pulse Width	(t_{PWH})		250	–	–	ns
Serial Clock "Low" Pulse Width	(t_{PWL})		250	–	–	ns
Data Set-up Time	(t_{DS})		150	–	–	ns
Data Hold Time	(t_{DH})		50.0	–	–	ns
Load/Latch Set-up Time	(t_{LL})		250	–	–	ns
Load/Latch Pulse Width	(t_{LLW})		150	–	–	ns
Load/Latch Delay	(t_{LLD})		200	–	–	ns
Load/Latch Over	(t_{LLO})		–	–	50.0	ns
Serial Data Clock Frequency			–	–	2.0	MHz

Notes
1. Gain Set 0dB, Input Level 1kHz -3.0dB (549mVrms).
2. With an a.c short-circuit input, measured in a 30kHz bandwidth.
3. See Figure 3.
4. Over the temperature and supply voltage range.