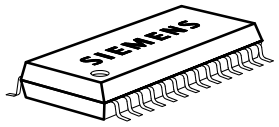
SIEMENS

TV Mixer-Oscillator-PLL for 1.1 GHz TUA 6010X

1 Overview



P-DSO-28-1

1.1 Features

- Smallest possible lock-in time; no asynchronous divider stage
- 1-chip system for MPU control (I^2C Bus)
- Fast I^2C Bus mode possible
- 4 programmable chip addresses
- Short pull-in time for quick channel switch-over and optimized loop stability
- 3 high-current switch outputs
- 2 TTL inputs
- 5-level A/D converter
- Lock-in flag
- Power-down flag
- Few external components
- Frequency and amplitude-stable balanced oscillator for the VHF, HYPER and UHF frequency range
- Optimum decoupling of input frequency from oscillator
- Double balanced mixer with wide dynamic range and low-impedance inputs for the VHF, HYPER and UHF frequency range
- Internal band switch
- Low-noise reference voltage
- Package P-DSO-28-1

1.2 Application

The IC is suitable for all tuners in TV and VCR sets.

Type	Ordering Code	Package
TUA 6010X	Q67001-A5210	P-DSO-28-1

1.3 Pin Configuration

(top view)

P-DSO-28-1

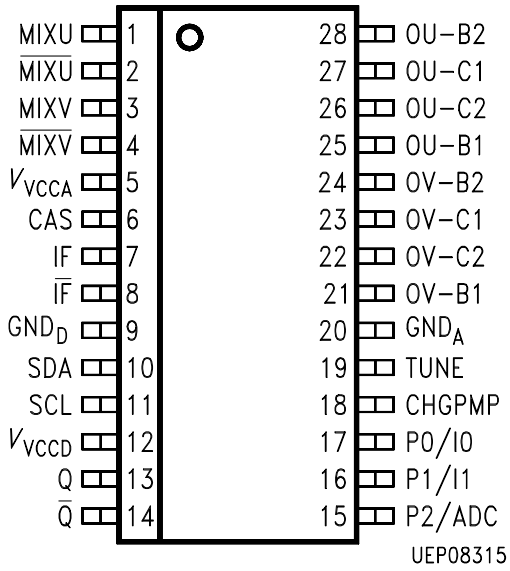


Figure 1

1.4 Pin Definitions and Functions

Pin No.	Symbol	Function
PLL Section		
6	CAS	Chip address select
9	GND_D	Ground for digital block (PLL)
10	SDA	Data input/output for the I^2C Bus
11	SCL	Clock input for the I^2C Bus
12	V_{VCCD}	Positive supply voltage for digital block (PLL)
13	Q	4 MHz low-impedance crystal oscillator input
14	$\overline{Q}$	4 MHz low-impedance crystal oscillator input
15	P2/ADC	Port output/ADC input
16	P1/I1	Port output/TTL input
17	P0/I0	Port output/TTL input
18	CHPMP	Charge pump output/loop filter
19	TUNE	Open collector output for pull-up resistor/loop filter
Mixer Oscillator Section		
1	MIXU	UHF mixer input, low-impedance, symmetrical to $\overline{MIXU}$
2	$\overline{MIXU}$	UHF mixer input, low-impedance, symmetrical to MIXU
3	MIXV	VHF or HYPER mixer input, low-impedance, symmetrical to $\overline{MIXV}$
4	$\overline{MIXV}$	VHF or HYPER mixer input, low-impedance, symmetrical to MIXV
5	V_{VCCA}	Positive supply voltage for analog block
7	IF	Open collector mixer output, high-impedance, symmetrical to $\overline{IF}$
8	$\overline{IF}$	Open collector mixer output, high-impedance, symmetrical to IF
20	GND_A	Ground for analog block
21	OV-B1	VHF oscillator amplifier, high-impedance base input, symmetrical to OV-B2
22	OV-C2	VHF oscillator amplifier, high-impedance collector output, symmetrical to OV-C1
23	OV-C1	VHF oscillator amplifier, high-impedance collector output, symmetrical to OV-C2

1.4 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
24	OV-B2	VHF oscillator amplifier, high-impedance base input, symmetrical to OV-B1
25	OU-B1	UHF oscillator amplifier, high-impedance base input, symmetrical to OV-B2
26	OU-C2	UHF oscillator amplifier, high-impedance collector output, symmetrical to OU-C1
27	OU-C1	UHF oscillator amplifier, high-impedance collector output, symmetrical to OU-C2
28	OU-B2	UHF oscillator amplifier, high-impedance base input, symmetrical to OU-B1

1.5 Functional Block Diagram

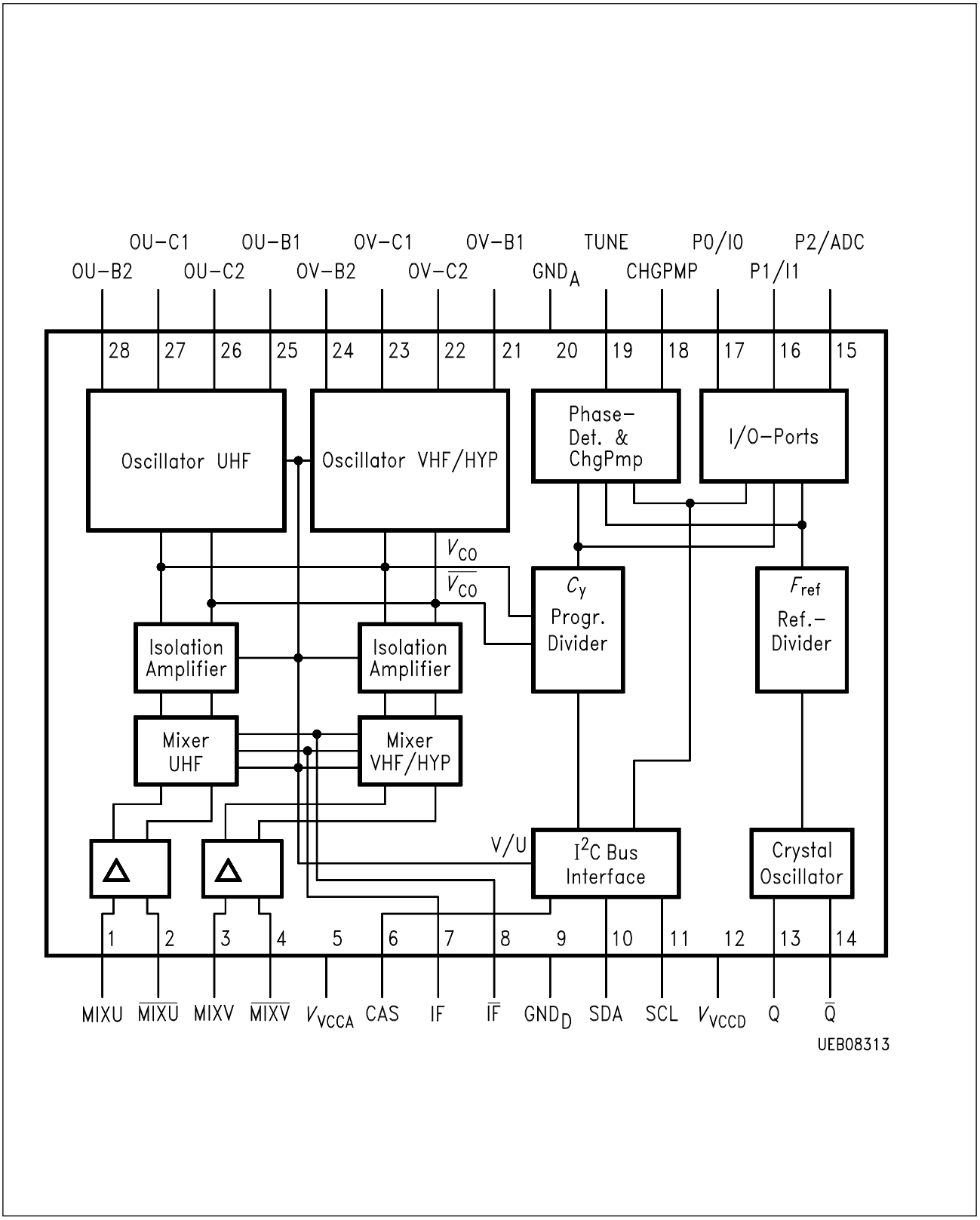


Figure 2
Block Diagram

2 Functional Description

The TUA 6010X device combines a digitally programmable phase locked loop (PLL), with a mixer oscillator block including two balanced mixers and oscillators for use in TV tuners.

The PLL block with four hard-switched chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 1.1 GHz in increments of 62.5 kHz. The tuning process is controlled by a microprocessor via an I^2C Bus. The device has three output ports, which all can also be used as input ports (two TTL inputs and one A/D converter input). A flag is set when the loop is locked. The input ports and lock flag can be read by the processor via the I^2C Bus.

The mixer oscillator block includes two balanced mixers (double balanced mixer with low-impedance input), two frequency and amplitude-stable balanced oscillators for VHF, HYPER and UHF, a low-noise reference voltage source and a band switch.

3 Circuit Description

Mixer-Oscillator Block

The mixer oscillator section includes two balanced mixers (double balanced mixer), two balanced oscillators for VHF and/or HYPER and UHF, a reference voltage source and a band switch.
Filters between tuner input and IC separate the TV frequency signals into two bands. The band switch ensures that only one mixer oscillator block at a time is activated. In the activated band the signal passes a front-end stage with MOSFET amplifier, a double tuned bandpass filter and is then fed to the balanced mixer input of the IC which has a low-impedance input. The input signal is mixed there with the on-chip oscillator signal from the activated oscillator section.

PLL Block

The mixer oscillator signal $V_{CO}/\overline{V}_{CO}$ is internally DC coupled as a differential signal at the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio N = 256 through 32767 and is then compared in a digital frequency/ phase detector to a reference frequency f_{REF} = 62.5 kHz. This frequency is derived from a balanced, low-impedance 4 MHz crystal oscillator (pin Q, $\overline{Q}$) divided by Q = 64.

The phase detector has two outputs UP and DOWN that drive two current sources I+ and I– of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the I+ current source pulses for the duration of the phase difference. In the reverse case the I– current source pulses. lf the two signals are in phase, the charge pump output (CHGPMP) goes into the high-impedance state (PLL is locked). An active lowpass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pull-up resistor at TUNE and external RC circuitry). The charge pump output is also switched into the high-impedance state when the control bit T0 = ‘1’. Here it should be noted, however, that the tuning voltage can alter over a long period in the high-impedance state as a result of self-discharge in the peripheral circuitry. TUNE may be switched off by the control bit OS to allow external adjustments.

By means of a control bit 5I the pump current can be switched between two values by software. This programmability permits alteration of the control response of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.

The software-switched ports P0, P1, P2 are general-purpose open-collector outputs.The test bit T1 = ‘1’, switches the test signals f_{REF} (4 MHz/32) and Cy (divided input signal) to P0 and P1 respectively. P0, P1, P2 are bidirectional: P0 and P1 are TTL inputs; P2 is an A/D converter input.

Data are exchanged between the processor and the PLL via the I²C Bus. The clock is generated by the processor (input SCL), while pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have hysteresis and a lowpass characteristic, which enhance the noise immunity of the I²C Bus.

The data from the processor pass through an I²C Bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are 'HIGH'). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes 'LOW', while SCL remains 'HIGH'. Stop condition: SDA goes 'HIGH' while SCL remains 'HIGH'. All further information transfer takes place during SCL = 'LOW', and the data is forwarded to the control logic on the positive clock edge.

The **table 1 'bit allocation'** should be referred to the following description. All telegrams are transmitted byte by byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to 'LOW' (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (chip select). The eighth bit (R/W) determines whether data are written into (R/W = '0') or read from (R/W = '1') the PLL.

In the data portion of the telegram during a WRITE operation, the first bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type or a stop condition has to follow the first byte.

If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists of two bits from the TTL input ports, three bits from the A/D converter, the lock flag and the power ON flag.

Four different chip addresses can be set by appropriate connection of pin CAU (see **table 2 'address selection'**).
When the supply voltage is applied, a power-on reset circuit prevents the PLL from setting the SDA line to 'LOW', which would block the bus. The power-on reset flag POR is set at power-on and when V_{VCCD} goes below 3.2 V. It will be reset at the end of a READ operation.

The lock detector resets the lock flag FL when the width of the charge pump current pulses is greater than the period of the crystal oscillator (i.e. 250 ns). Hence, when FL = '1', the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_p \, (K_{VCO} / f_Q) \, (C_1 + C_2)/(C_1 \, C_2)$$

where I_p is the charge pump current, K_{VCO} the V_{CO} gain, f_Q the crystal oscillator frequency and C_1, C_2 the capacitances in the loop filter (see application circuit). As the charge pump pulses at 62.5 kHz (= f_{REF}), it takes a maximum of 16 µs for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive f_{REF} periods. Therefore it takes between 128 µs and 144 µs for FL to be set after the loop regains lock.

Table 1
Bit Allocation Read/Write Data

	MSB	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB	Ack
Write Data									
Address Byte	1	1	0	0	0	MA1	MA0	0	Ack
Prog. Divider Byte 1	0	n14	n13	n12	n11	n10	n9	n8	Ack
Prog. Divider Byte 2	n7	n6	n5	n4	n3	n2	n1	n0	Ack
Control Byte 1	1	5I	T1	T0	1	1	1	OS	Ack
Control Byte 2	V/U	x	x	x	x	P2	P1	P0	Ack
Read Data									
Address Byte	1	1	0	0	0	MA1	MA0	1	Ack
Status Byte	POR	FL	x	I1	I0	A2	A1	A0	Ack

Note: MSB is shifted first.

Divider Ratio

N = 16384 × n14 + 8192 × n13 + 4096 × n12 + 2048 × n11 + 1024 × n10 + 512 × n9 + 256 × n8 + 128 × n7 + 64 × n6 + 32 × n5 + 16 × n4 + 8 × n3 + 4 × n2 + 2 × n1 + n0

Ports P0, P1, P2

1	Open-collector output is active
0	Open-collector output is inactive, TTL-inputs I1,I0 and ADC available

Bandswitch V/U

'HIGH'	switch to OSC/MIX UHF

Pump Current 5I

'HIGH'	switch to high current

Disabling Tuning Voltage OS

'HIGH'	disables TUNE

Power ON Reset Flag POR:	flag is set at power-on and reset at the end of READ operation
PLL Lock Flag FL:	flag is set when loop is locked
TTL-Inputs I1, I0:	input data from pins P1/I1, P0/I0

Table 2
Address Selection

Voltage at CAS	M1	M0
(0 … 0.1) × V_{VCCD}	0	0
Open circuit	0	1
(0.4 … 0.6) × V_{VCCD}	1	0
(0.9 … 1) × V_{VCCD}	1	1

Table 3
Test Modes

Test Mode	T1	T0
Normal operation	0	0
P1 = Cy output, P0 = f_{REF} output	1	0
Charge pump output CHGPMP is in high-impedance state	0	1
TTL-inputs I1/I0 are Cy/f_{REF} inputs of phase detector	1	1

Table 4
A/D Converter Levels

Voltage at P2/ADC	A2	A1	A0
(0 … 0.15) × V_{VCCD}	0	0	0
(0.15 … 0.3) × V_{VCCD}	0	0	1
(0.3 … 0.45) × V_{VCCD}	0	1	0
(0.45 … 0.6) × V_{VCCD}	0	1	1
(0.6 … 1) × V_{VCCD}	1	0	0

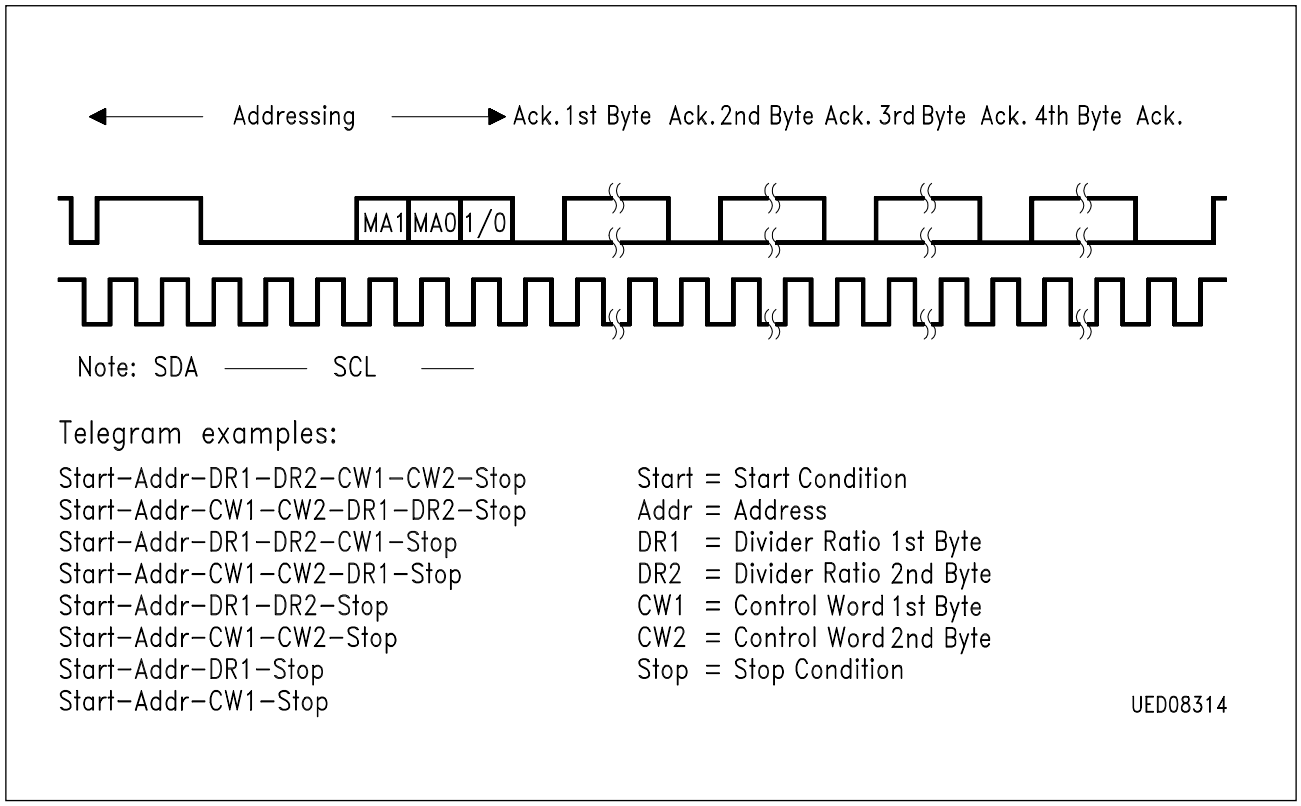

Addressing
Ack. 1st Byte
Ack. 2nd Byte
Ack. 3rd Byte
Ack. 4th Byte
Ack.
MA1
MA0
1/0
Note: SDA
SCL
Telegram examples:
Start–Addr–DR1–DR2–CW1–CW2–Stop
Start–Addr–CW1–CW2–DR1–DR2–Stop
Start–Addr–DR1–DR2–CW1–Stop
Start–Addr–CW1–CW2–DR1–Stop
Start–Addr–DR1–DR2–Stop
Start–Addr–CW1–CW2–Stop
Start–Addr–DR1–Stop
Start–Addr–CW1–Stop
Start = Start Condition
Addr = Address
DR1 = Divider Ratio 1st Byte
DR2 = Divider Ratio 2nd Byte
CW1 = Control Word 1st Byte
CW2 = Control Word 2nd Byte
Stop = Stop Condition
UED08314

Figure 3

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

T_A = – 20 °C to + 80 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
PLL					
Supply voltage	V_{VCCD}	– 0.3	6	V	
Current	I_{VCCD}		38	mA	
Output CHGPMP	V_{CHGPMP}	– 0.3	3.5	V	
Crystall oscillator pins Q, $\overline{Q}$	V_Q	– 0.3	V_{VCCD}	V	
Bus input/output SDA	V_{SDA}	– 0.3	6	V	
Bus input SCL	V_{SCL}	– 0.3	6	V	
Port outputs P0, P1, P2	V_P	– 0.3	13	V	
Chip address switch CAS	V_{CAS}	– 0.3	V_{VCCD}	V	
Output active filter TUNE	V_{TUNE}	– 0.3	33	V	
Bus output SDA	I_{SDAL}	– 1	5	mA	Open collector
Port outputs P0, P1, P2	I_{PL}	– 1	15	mA	Open collector
Total port output current	ΣI_{PL}		20	mA	
Junction temperature	T_J		125	°C	
Storage temperature	T_S	– 40	125	°C	
Thermal resistance (junction to ambient)	R_{thA}		75	K/W	
Mixer Oscillator					
Supply voltage	V_{VCCA}	– 0.3	6	V	
Current	I_{VCCA}		38	mA	
Output IF, $\overline{IF}$	$I_{IF, \overline{IF}}$		9	mA	Open collector

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{VCCD}	4.5	5.5	V	
	V_{VCCA}	4.5	5.5	V	
Supply current	I_{VCCD}	16	33	mA	
	I_{VCCA}	16	33	mA	
Mixer output voltage	$V_{IF, \overline{IF}}$	4.5	5.5	V	Open collector
Mixer output current	$I_{IF, \overline{IF}}$	4.0	8.0	mA	Open collector
Programmable divider factor	N	256	32767		
VHF mixer input frequency range	f_{MIXV}	30	500	MHz	
UHF mixer input frequency range	f_{MIXU}	400	900	MHz	
VHF oscillator frequency range	f_{OV}	30	500	MHz	
UHF oscillator frequency range	f_{OU}	400	900	MHz	
Ambient temperature	T_A	– 20	80	°C	

Note: In the operating range the functions given in the circuit description are fulfilled.

4.3 AC/DC Characteristics

V_{VCCD} = 4.5 V to 5.5 V, T_A = – 20 °C to 80 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
PLL						
Supply current	I_{VCCD}	19	24	29	mA	V_{VCCD} = 5 V
Crystal Oscillator Connections Q, $\overline{Q}$						
Crystal frequency	f_Q	3.2	4.0	4.8	MHz	Series resonance
Crystal resistance[1)]	R_Q	10		100	Ω	Series resonance
Oscillation frequency	f_Q	3.99975	4.000	4.00025	MHz	f_Q = 4 MHz
Drive current[1)]	I_Q	t.b.d.	t.b.d.	t.b.d.	µArms	f_Q = 4 MHz
Input impedance[1)]	Z_Q	– 600	– 750	– 900	Ω	f_Q = 4 MHz
Margin from 1st (fundamental) to 2nd and 3rd harmonics[1)]	a_H			20	dB	f_Q = 4 MHz

[1)] Design note only: no 100 % final inspection.

4.3 AC/DC Characteristics (cont'd)

V_{VCCD} = 4.5 V to 5.5 V, T_A = – 20 °C to 80 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Charge Pump Output CHGPMP (V_{VCCD} = 5 V)						
HIGH output current	I_{CPH}	± 90	± 220	± 300	µA	5I = '1', V_{CP} = 2 V
LOW output current	I_{CPL}	± 22	± 50	± 75	µA	5I = '0', V_{CP} = 2 V
Tristate current	I_{CPZ}		1		nA	T0 = '1', V_{CP} = 2 V
Output voltage	V_{CP}	1.0		2.5	V	locked
Drive Output TUNE (open collector)						
HIGH output current	I_{TH}			10	µA	V_{TH} = 33 V, T0 = '1'
LOW output voltage	V_{TL}			0.5	V	I_{TL} = 1.5 mA
Port Outputs P0, P1, P2 (open collector)						
HIGH output current	I_{POH}			10	µA	V_{POH} = 13.5 V
LOW output voltage	V_{POL}			0.5	V	I_{POL} = 15 mA

4.3 AC/DC Characteristics (cont'd)

V_{VCCD} = 4.5 V to 5.5 V, T_A = – 20 °C to 80 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
TTL Port Inputs P0, P1						
HIGH input voltage	V_{PIH}	2.7			V	
LOW input voltage	V_{PIL}			0.8	V	
HIGH input current	I_{PIH}			10	µA	V_{PIH} = 13.5 V
LOW input current	I_{PIL}		– 10		µA	V_{PIL} = 0 V
ADC Port Input P2						
HIGH input current	I_{ADCH}			10	µA	
LOW input current	I_{ADCL}	– 10			µA	
Address Selection Input CAS						
HIGH input current	I_{CASH}			50	µA	V_{CASH} = 5 V
LOW input current	I_{CASL}	– 50			µA	V_{CASL} = 0 V

4.3 AC/DC Characteristics (cont'd)

V_{VCCD} = 4.5 V to 5.5 V, T_A = – 20 °C to 80 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
I²C Bus						
Bus Inputs SCL, SDA						
HIGH input voltage	V_{IH}	3		5.5	V	
LOW input voltage	V_{IL}			1.5	V	
HIGH input current	I_{IH}			10	µA	$V_{IH} = V_S$
LOW input current	I_{IL}	– 20			µA	V_{IL} = 0 V
Bus Output SDA (open collector)						
HIGH output current	I_{OH}			10	µA	V_{OH} = 5.5 V
LOW output voltage	V_{OL}			0.4	V	I_{OL} = 3 mA
Edge Speed SCL, SDA						
Rise time	t_r			300	ns	
Fall time	t_f			300	ns	
Clock Timing SCL						
Frequency	f_{SCL}	0		400	kHz	
HIGH pulse width	t_H	0.6			µs	
LOW pulse width	t_L	1.3			µs	

4.3 AC/DC Characteristics (cont'd)

V_{VCCD} = 4.5 V to 5.5 V, T_A = – 20 °C to 80 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start Condition						
Set-up time	t_{susta}	0.6			µs	
Hold time	t_{hsta}	0.6			µs	
Stop Condition						
Set-up time	t_{susto}	0.6			µs	
Bus free	t_{buf}	1.3			µs	
Data Transfer						
Set-up time	t_{sudat}	0.1			µs	
Hold time	t_{hdat}	0			µs	
Input hysteresis SCL, SDA[1)]	V_{hys}		200		mV	
Noise immunity SCL, SDA[1), 2)]	V_N		5		Vpp	f_N = 2 MHz … 14 MHz
Capacitive load for each bus line	C_L			400	pF	

[1)] Design note only: no 100 % final inspection.

[2)] Sinusoidal noise signal applied via a 33 pF coupling capacitor.

4.3 AC/DC Characteristics

V_{VCCD} = 4.5 V to 5.5 V, T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Mixer Oscillator						
Current consumption	I_{VCCA}	15	21	27	mA	Bit V/U = 'L'
	I_{VCCA}	18	24	30	mA	Bit V/U = 'H'
Mixer output impedance	$R_{IF, \overline{IF}}$		20		kΩ	Parallel equivalent circuit
	$C_{IF, \overline{IF}}$		0.5		pF	Parallel equivalent circuit
VHF and HYPER Circuit Section						
Oscillator frequency range	f_{OSCV}	80		170	MHz	V_d = 0 … 28 V; VHF
	f_{OSCH}	140		450	MHz	V_d = 0 … 28 V; HYP
Oscillator drift	Δf_{OSCV}			400	kHz	V_S = 5 V ± 10 %
	Δf_{OSCV}			500	kHz	ΔT = 25 °C
	Δf_{OSCV}			100	kHz	t = 5 s up to 15 min after switching on
Oscillator pulling	V_{MIXV}	100	108		dBµV	Δf = 10 kHz in channel E2
	V_{MIXV}	100	108		dBµV	Δf = 10 kHz in channel S10
	V_{MIXV}	80	88		dBµV	Δf_{int} = E2 + N + 5 – 1 MHz
	V_{MIXV}	80	88		dBµV	Δf_{int} = S10 + N + 5 – 1 MHz
Mixer gain	G_{MixV}	11	14	17	dB	
Mixer noise figure	F_{MixV}		5	8	dB	Channel E2 (DSB)
	F_{MixV}		5	8	dB	Channel 10 (DSB)
Crosstalk f_{in}/LO	V_{MixV}	150	1000		mVrms	Max. input level for 10 dB distance f_{in}/LO
Mixer input impedance	R_{MixV}		20		Ω	Serial equivalent circuit
	L_{MixV}		10		nH	Serial equivalent circuit
IF suppression	a_{IF}		20		dB	V_{MixB} = 80 dBµV

4.3 AC/DC Characteristics (cont'd)

V_{VCCD} = 4.5 V to 5.5 V, T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
UHF Circuit Section						
Oscillator frequency range	f_{OSCU}	440		900	MHz	V_t = 0 … 28 V
Oscillator drift	Δf_{OSCU}			400	kHz	V_S = 5 V ± 10 %
	Δf_{OSCU}			800	kHz	ΔT = 25 °C
	Δf_{OSCU}			100	kHz	t = 5 s up to 15 min after switching on
Oscillator pulling	V_{MIXU}	100	108		BµV	Δf = 10 kHz in channel E21
	V_{MIXU}	100	108		BµV	Δf = 10 kHz in channel E68
	V_{MIXU}	80	88		dBµV	Δf_{int} = E21 + N + 5 – 1 MHz
	V_{MIXU}	80	88		dBµV	Δf_{int} = E68 + N + 5 – 1 MHz
Mixer gain	G_{MixU}	11	14	17	dB	
Mixer noise figure	F_{MixU}		6	9	dB	Channel E21 (DSB)
	F_{MixU}		7	10	dB	Channel E68 (DSB)
Crosstalk f_{in}/LO	V_{MixU}	150	1000		mVrms	Max. input level for 10 dB distance f_{in}/LO
Mixer input impedance	R_{MixU}		20		Ω	Serial circuit equivalent
	L_{MixU}		10		nH	Serial circuit equivalent
IF suppression	a_{IF}		20		dB	V_{MixB} = 80 dBµV

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Test Circuit 1

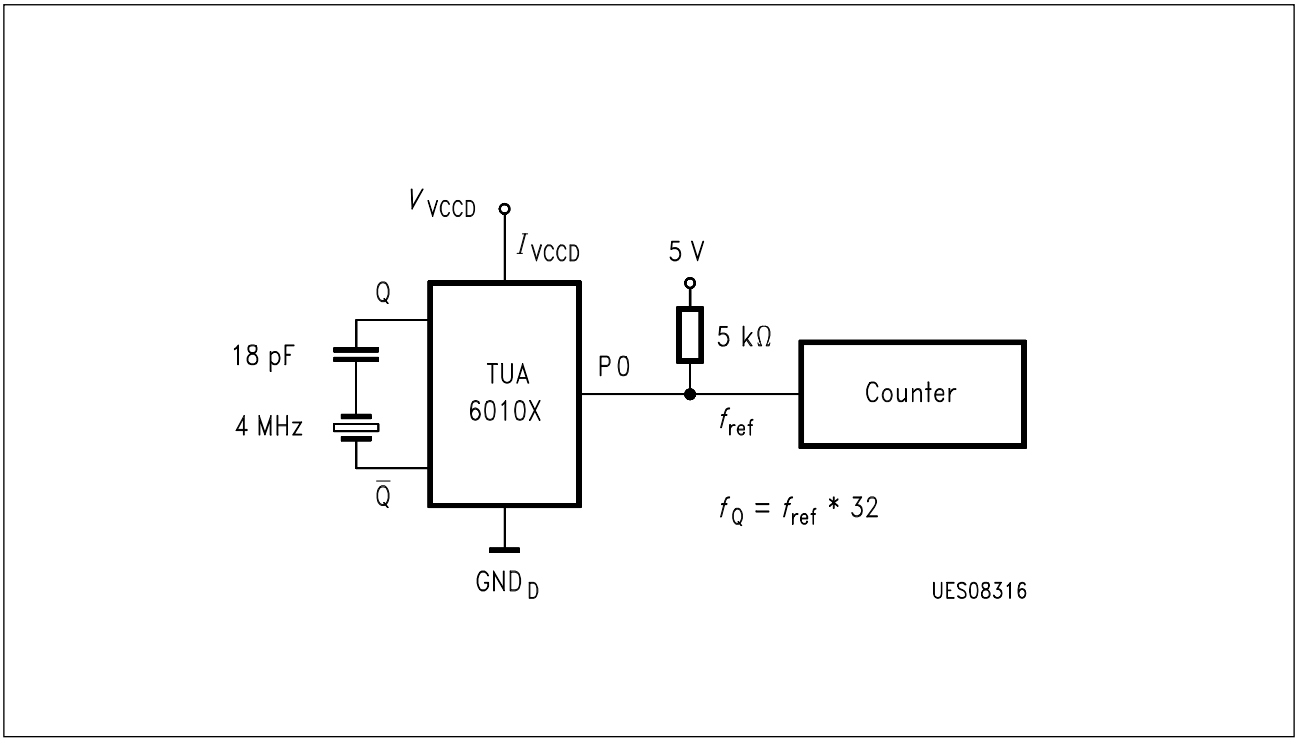


Figure 4
Measurement of Crystal Oscillator Frequency

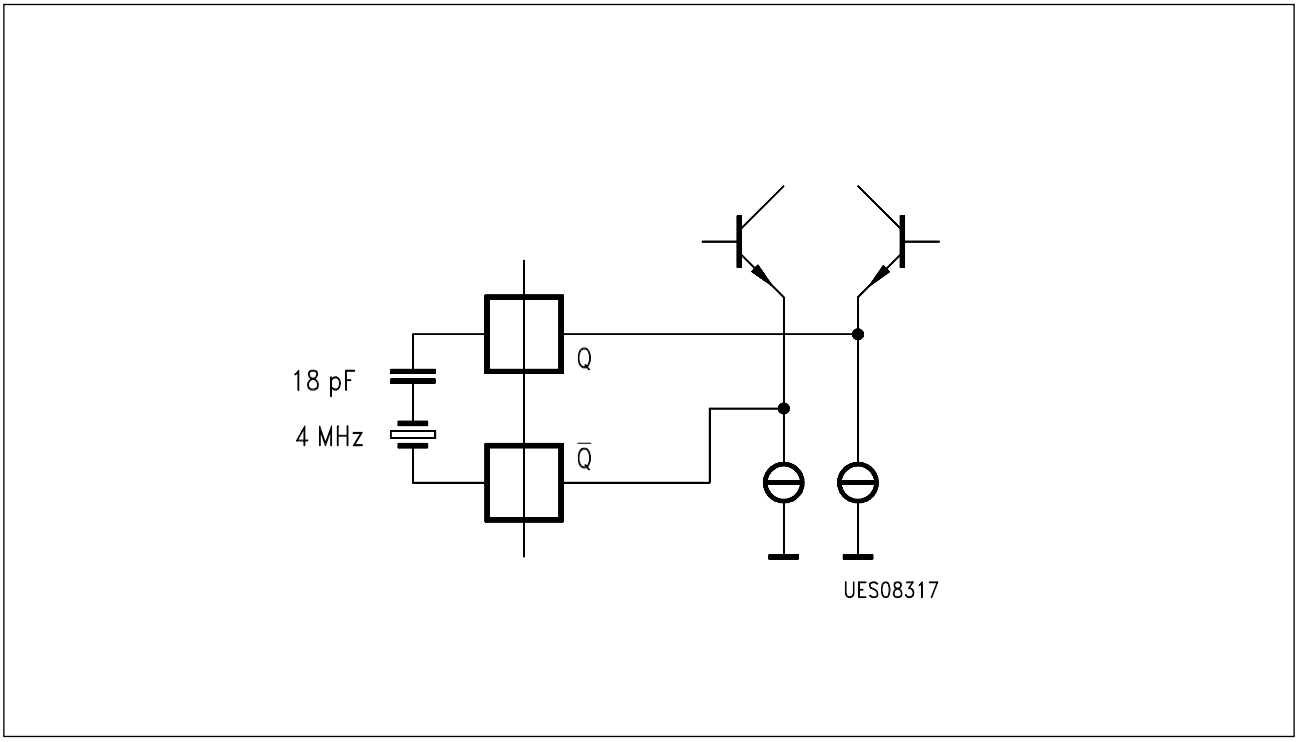


Figure 5
Equivalent I/O-Schematic

Test Circuit 2

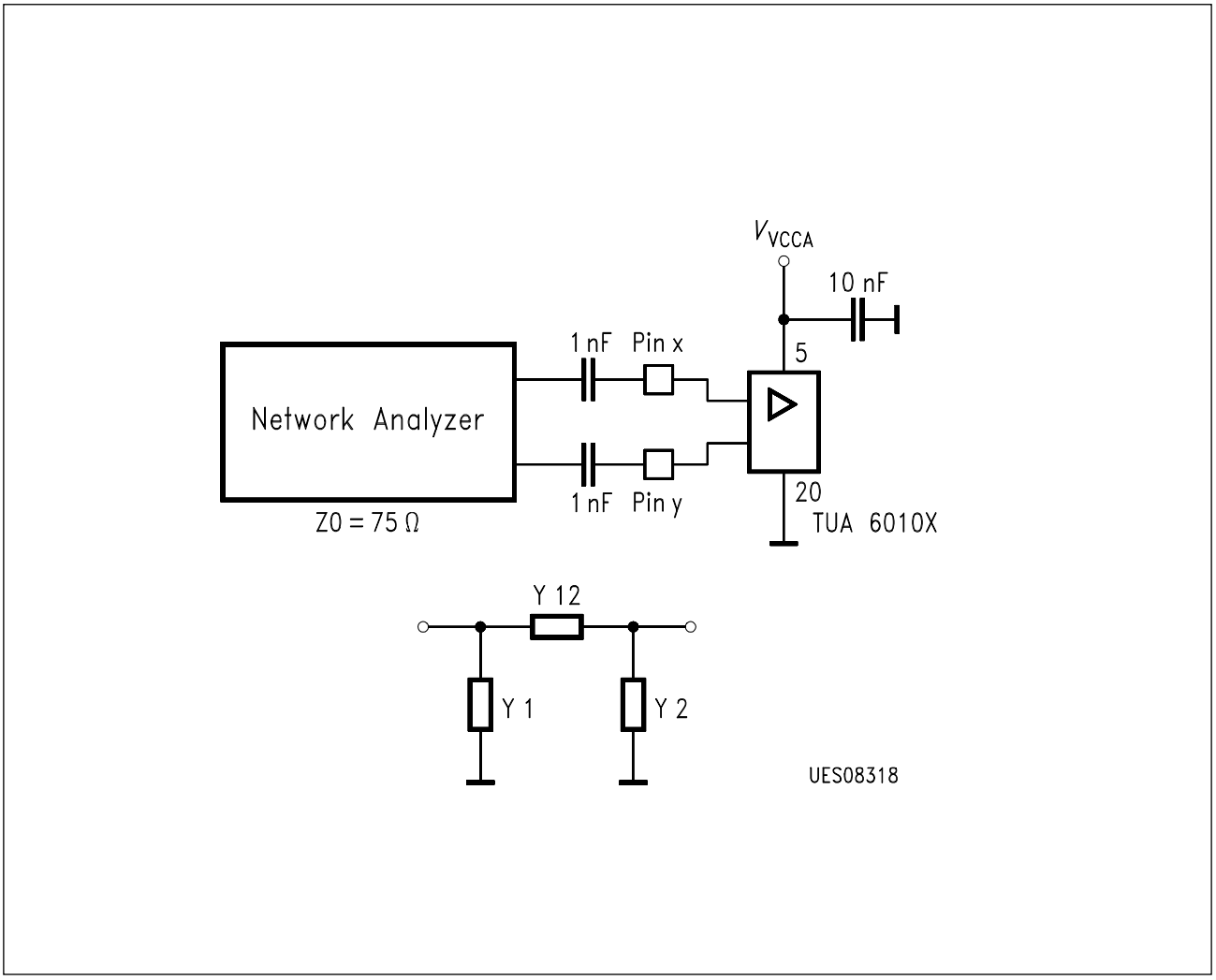


Figure 6
Measurement of S-Parameters S11, S12, S21, S22 and Calculation of π-Equivalent Circuit

Table 5
Test Frequency

Test Point	Test Frequency in MHz	Pin x	Pin y
Mixer input impedance VHF	300	3	4
Mixer input impedance UHF	600	1	2

Test Circuit 3

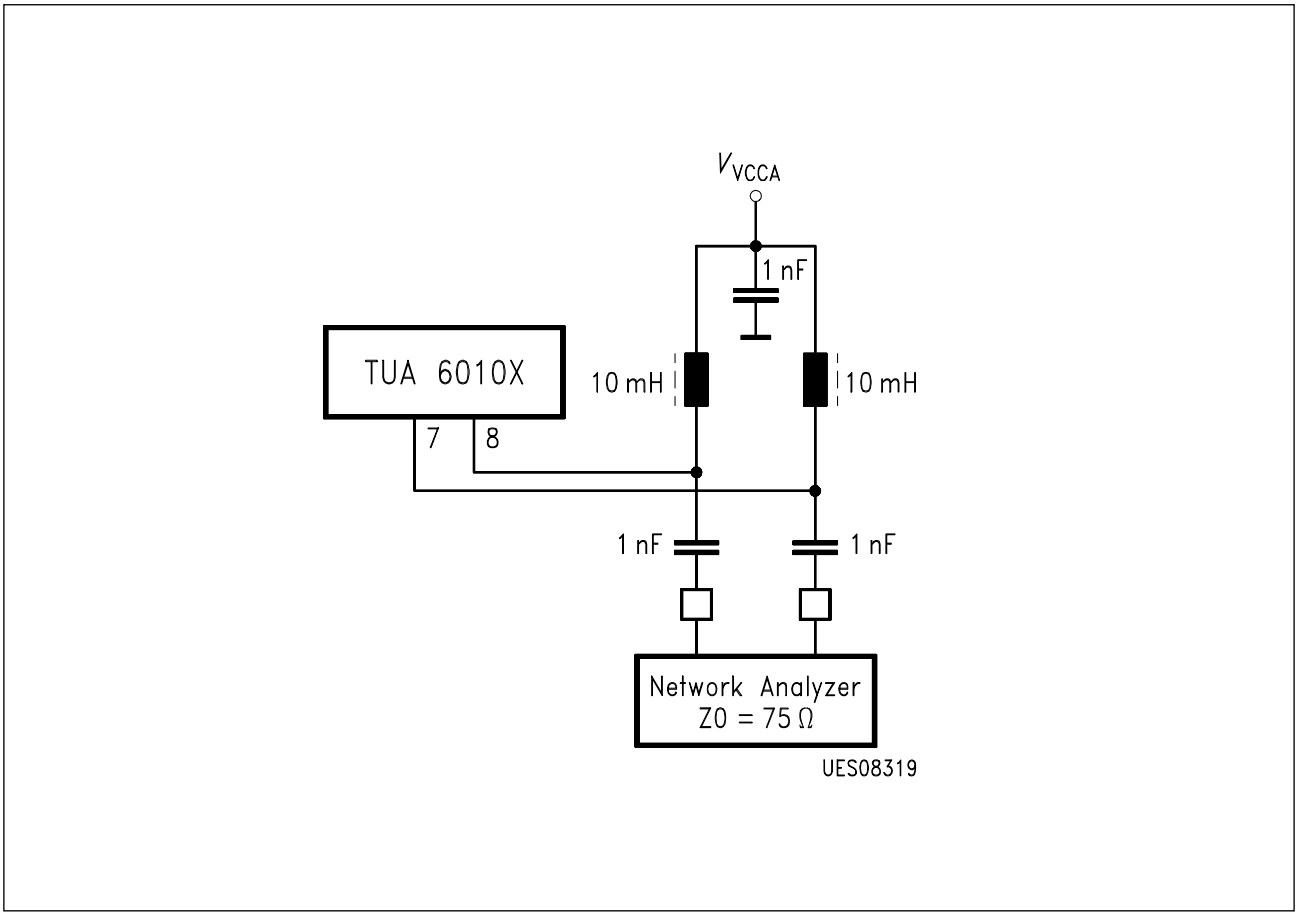


Figure 7
Measurement of Output Impedance
by Measurement of S-Parameters S11, S12, S21, S22 at 45 MHz

Test Circuit 4

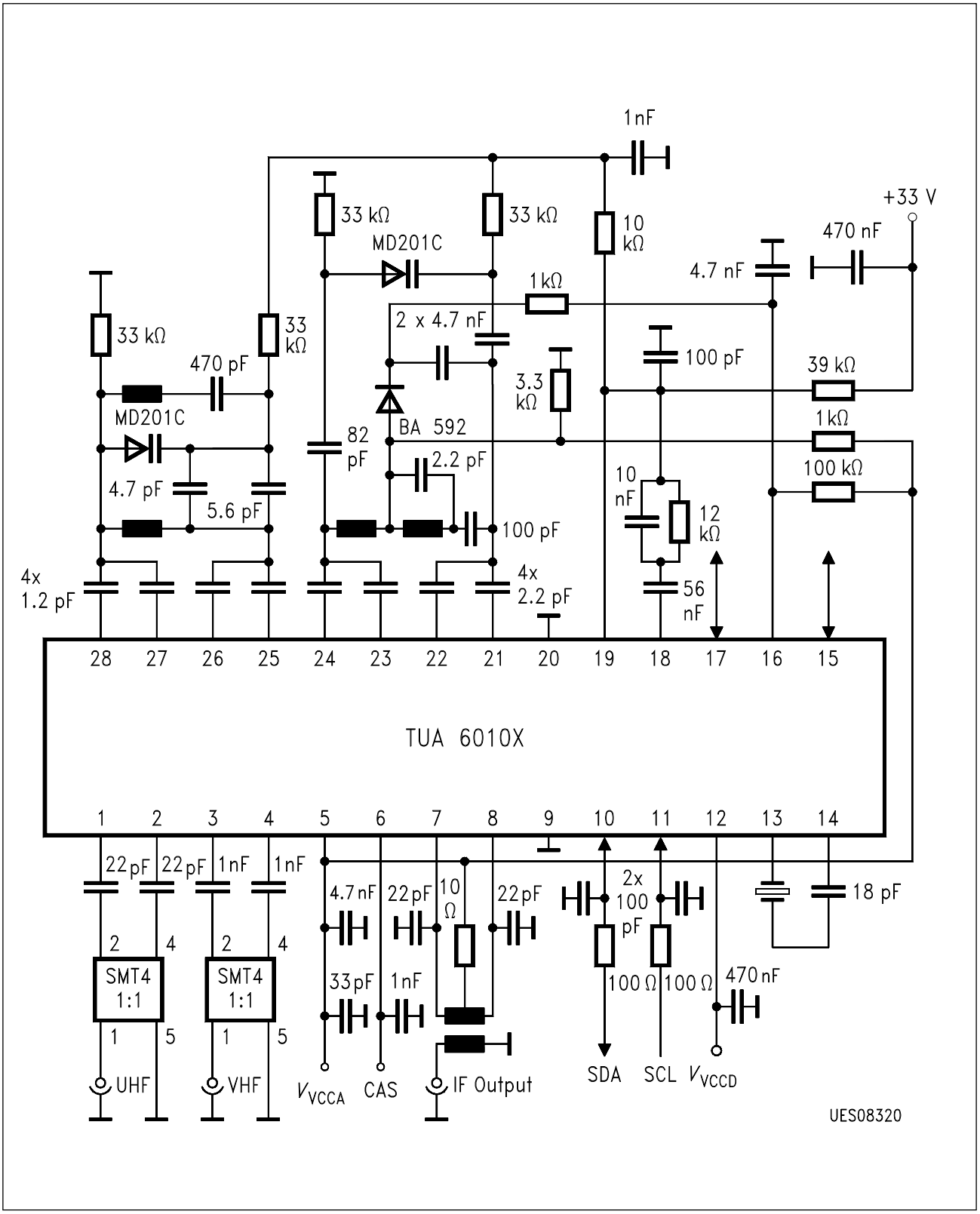


Figure 8

Equivalent I/O-Schematic

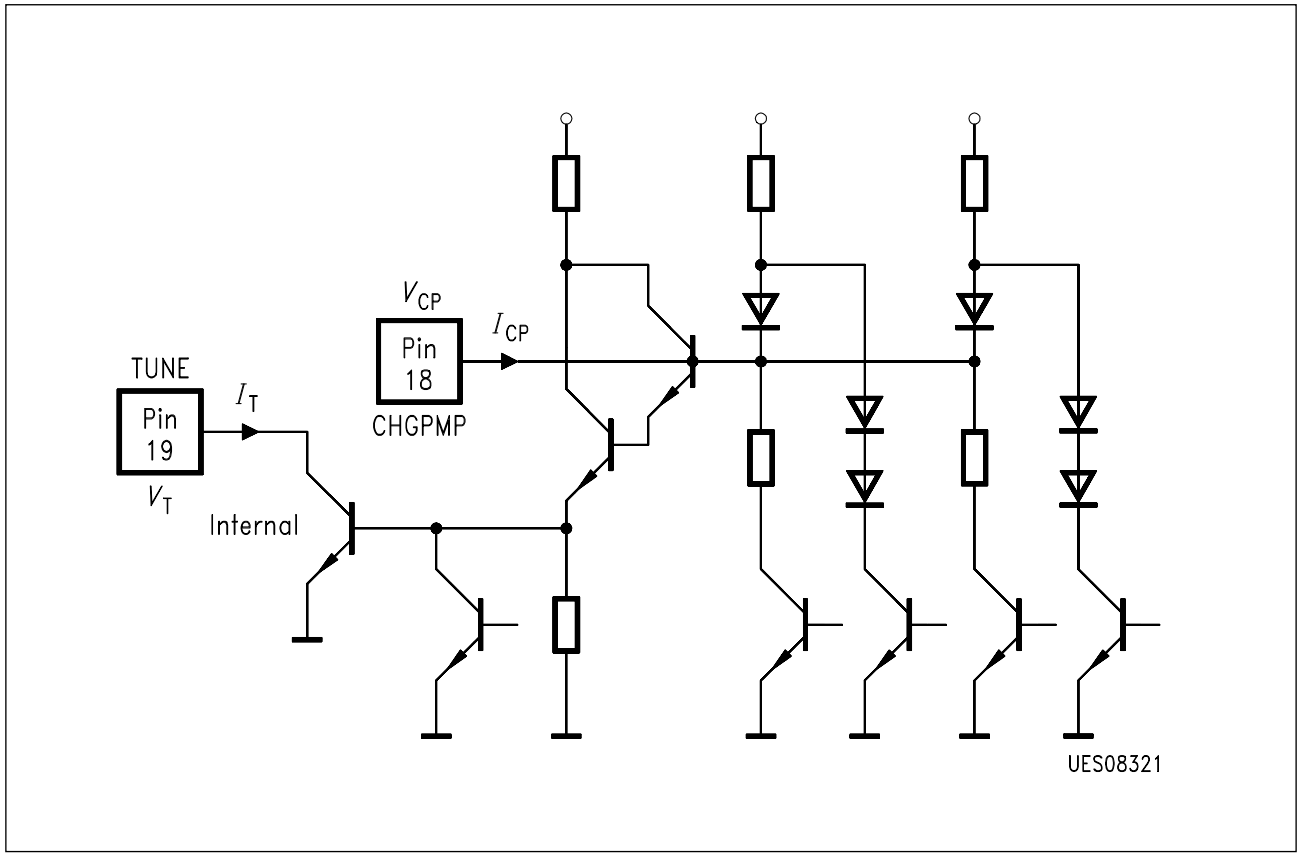


Figure 9
Equivalent I/O-Schematic of Charge Pump

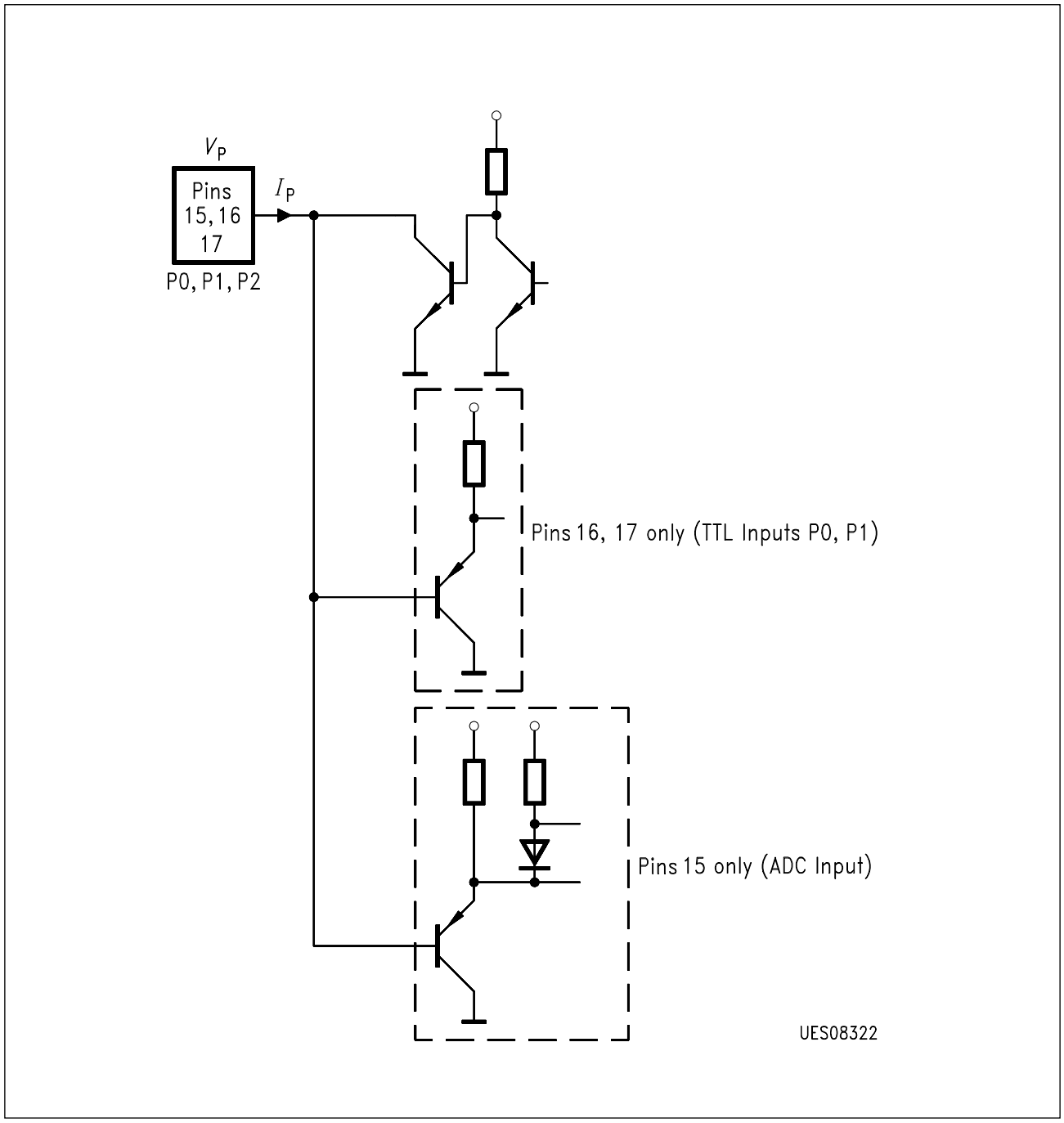


Figure 10
Equivalent I/O-Schematic of Port Pins

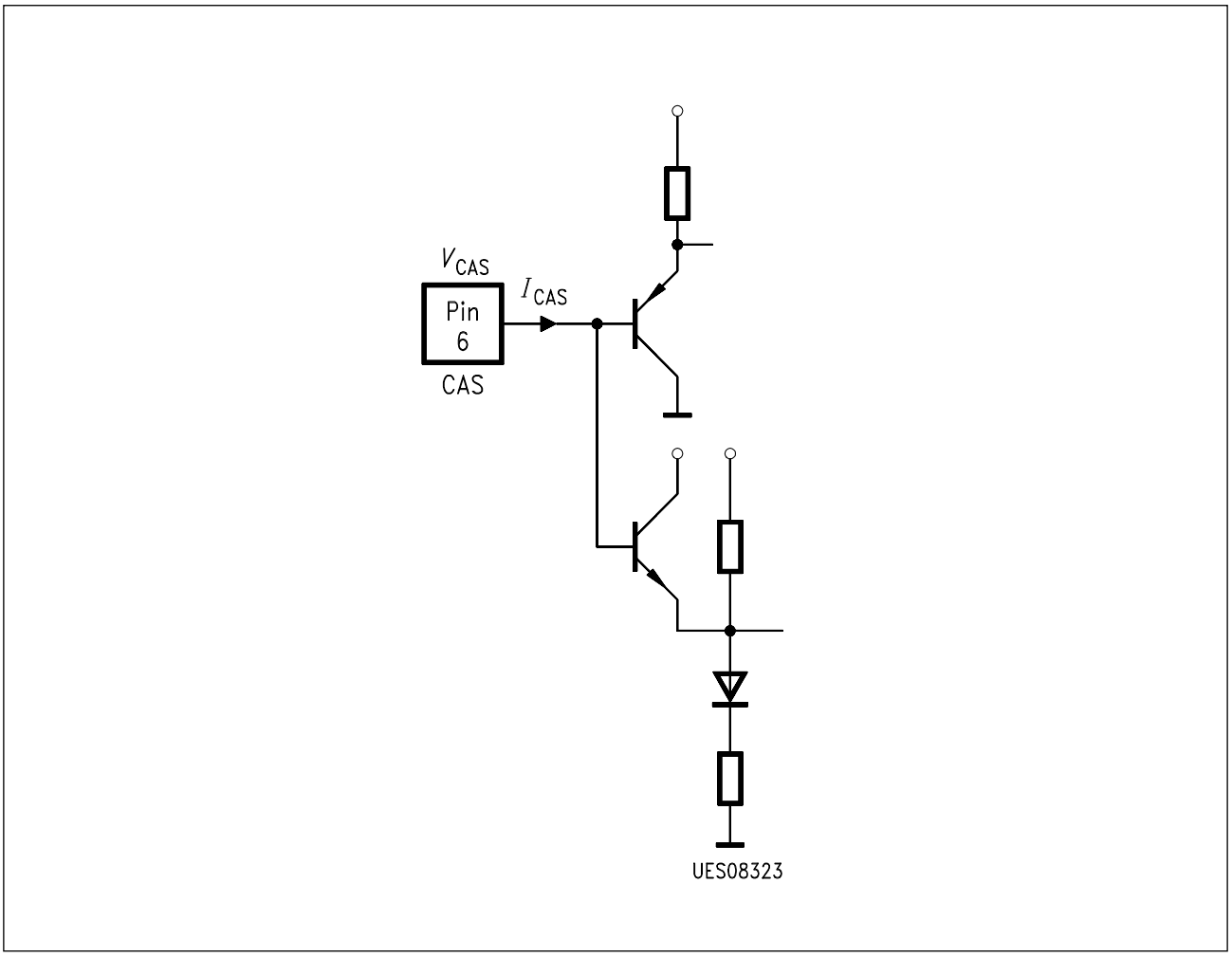


Figure 11
Equivalent I/O-Schematic of CAS Pin

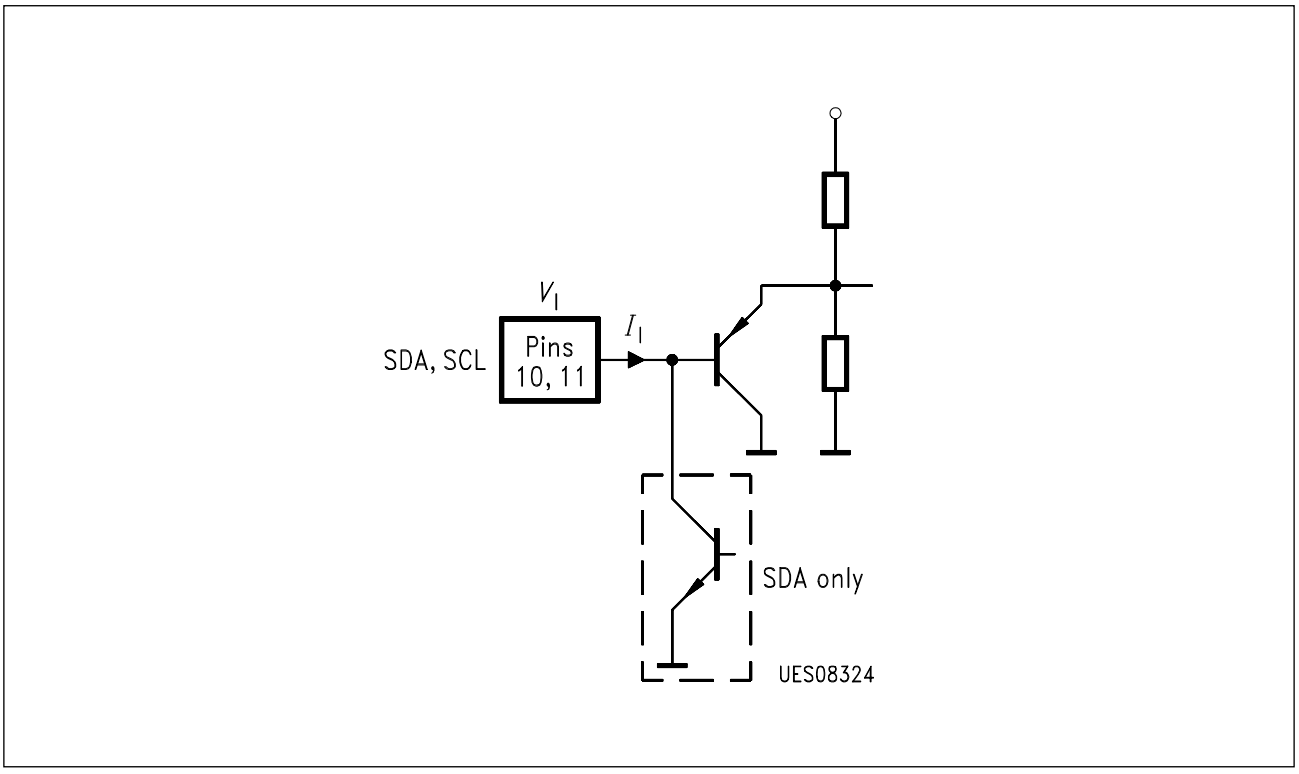


Figure 12
Equivalent I/O-Schematic of SDA/SCL Pins

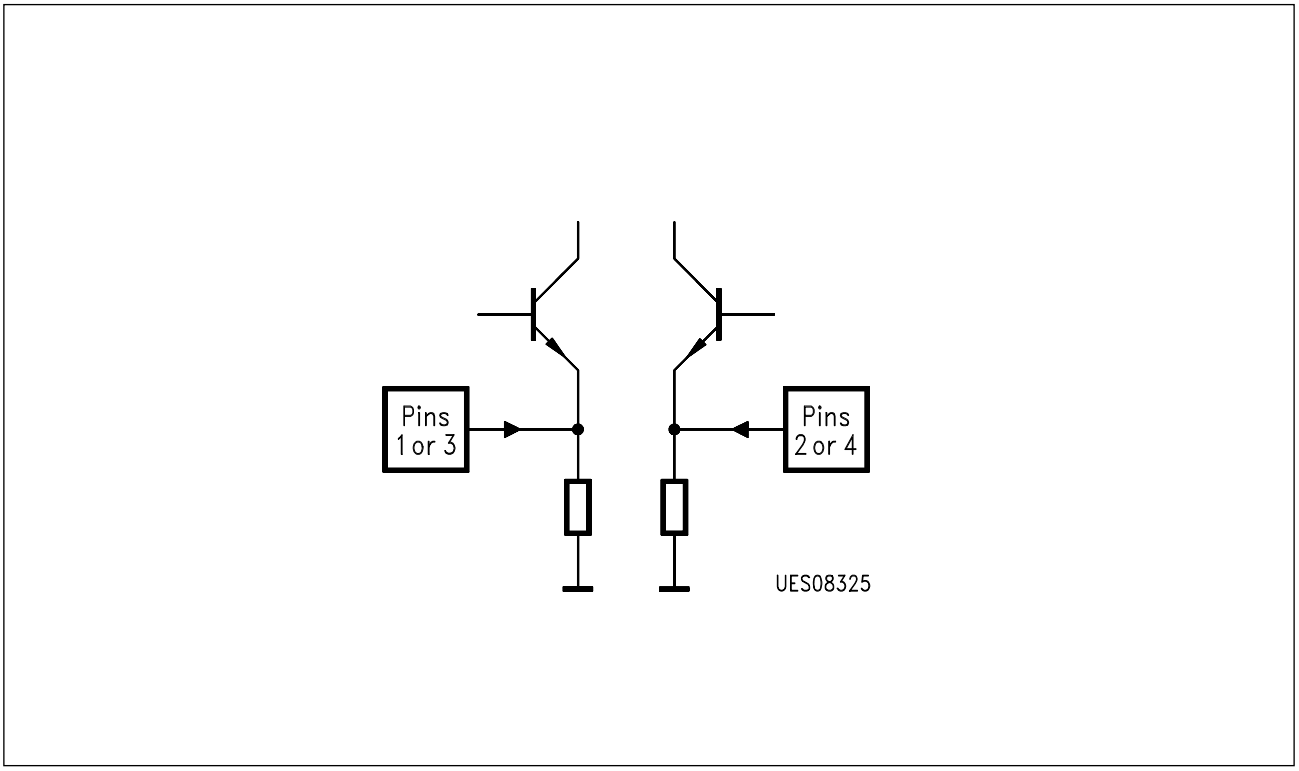


Figure 13
Equivalent I/O-Schematic of MIXU/$\overline{\text{MIXU}}$/MIXV/$\overline{\text{MIXV}}$ Pins

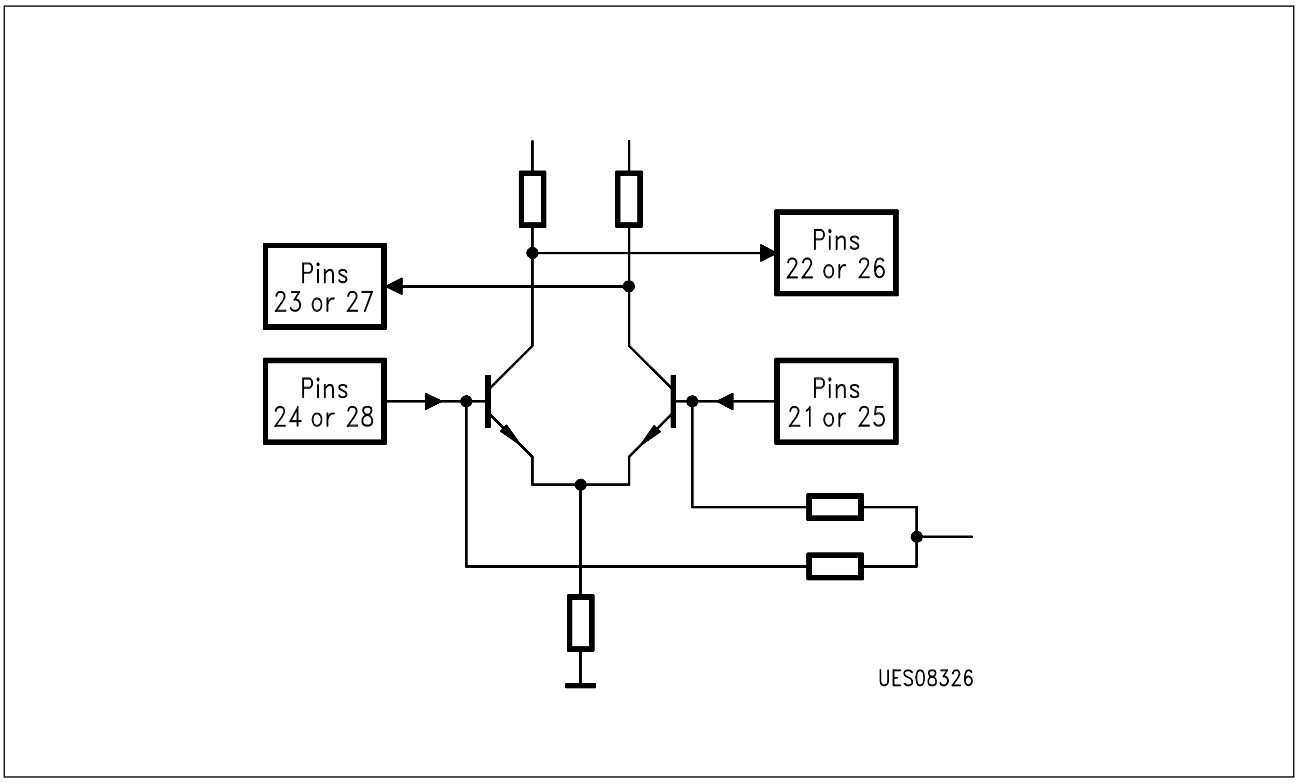


Figure 14
Equivalent I/O-Schematic of UHF- VHF-Oscillator Pins

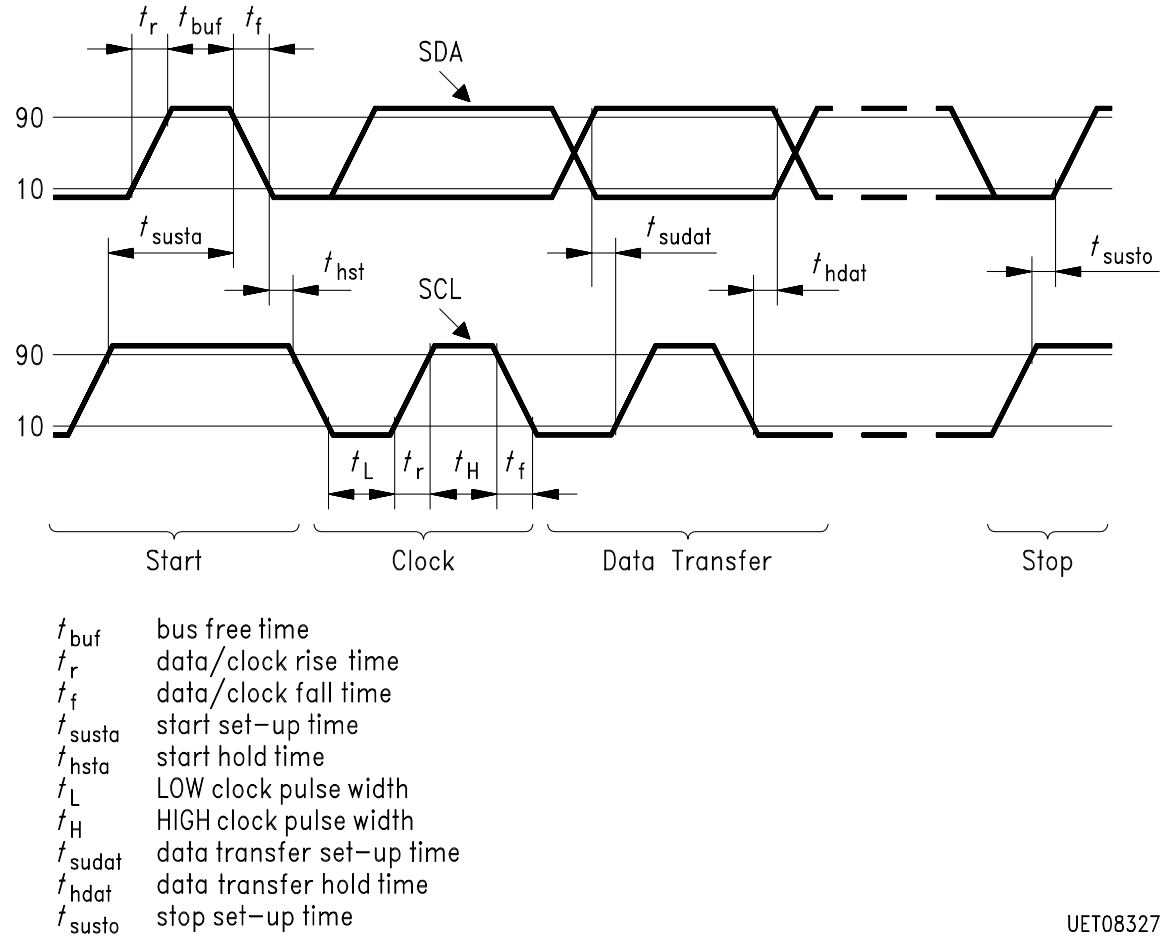
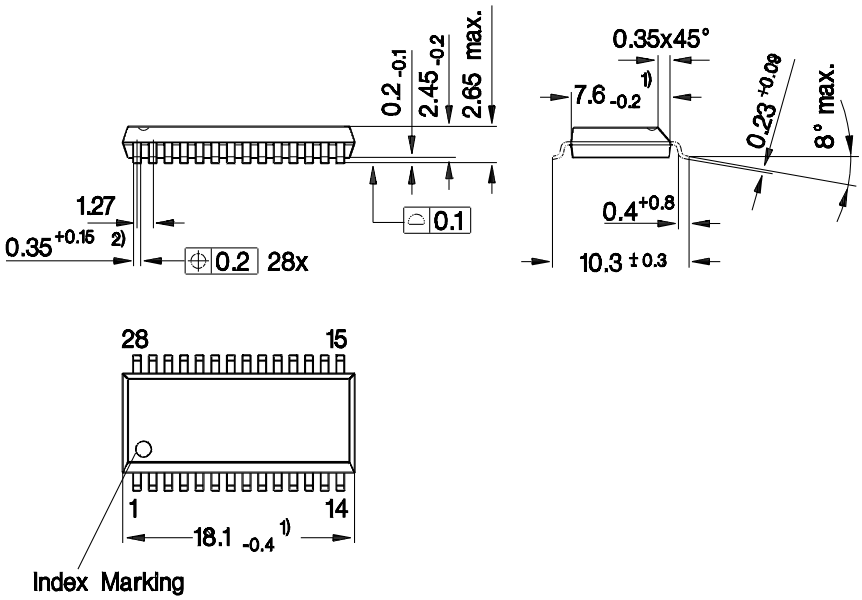


Figure 15
I²C Bus Timing

5 Package Outlines

P-DSO-28-1
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

GPS05123

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm