PM5313

SPECTRA-622

SONET/SDH PAYLOAD EXTRACTOR/ALIGNER

REVISION B DEVICE ERRATA

ISSUE 4: JUNE 2001

PRODUCTION

PROPRIETARY AND CONFIDENTIAL TO PMC-SIERRA INC., AND FOR ITS CUSTOMERS' INTERNAL USE

REVISION HISTORY

Issue No.	Issue Date	Details of Change
4	June 2001	Rev B errata updated to include known errors in issue 6 datasheet
3	September 2000	Rev B errata updated to reflect production release errata
2	May 2000	Rev A errata edited to reflect Rev B errata
1	January 2000	Document created.

CONTENTS

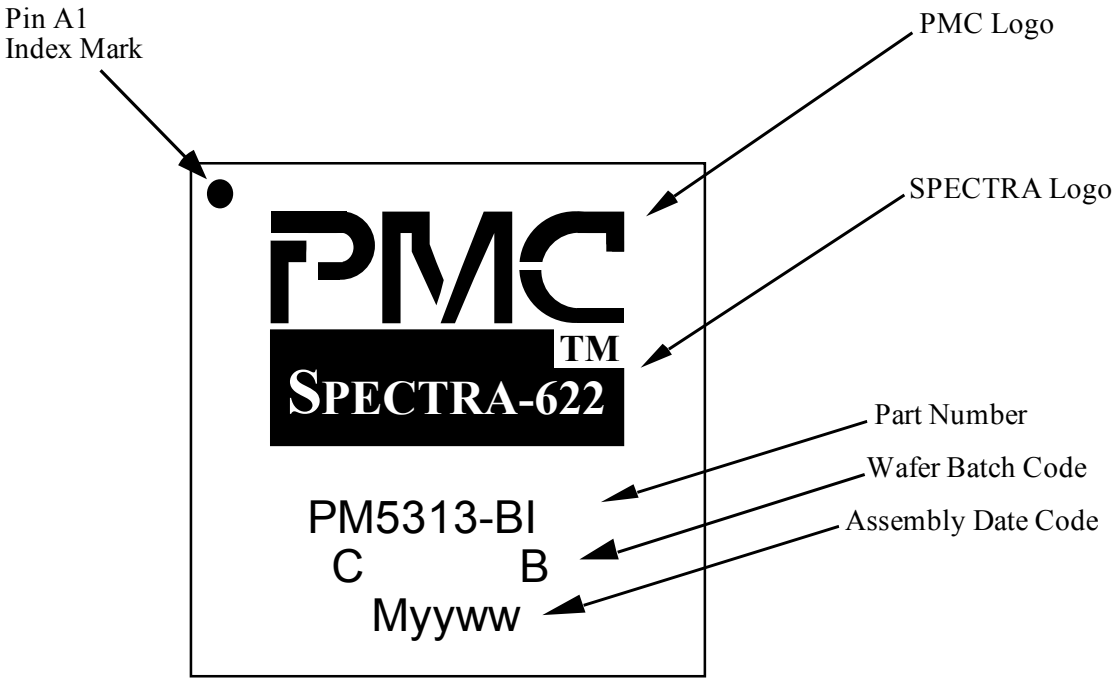
1 ISSUE 4 ERRATA

This document is the errata notice for Revision B, production release of the SPECTRA-622 (PM5313-BI) and issue 6 SPECTRA-622 datasheet. The issue 6 SPECTRA-622 datasheet (PMC-1981162) and issue 4 errata supersede all prior editions and versions of the datasheet.

1.1 Device Identification

The information in this document applies to the PM5313 SPECTRA-622 revision B device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1). PM5313 SPECTRA-622 Revision B is packaged in a 520 pin Super BGA package.

Figure 1: PM5313 SPECTRA-622 Branding Format



TOP VIEW
SCALE : 2:1
(APPROX.)

2 FUNCTIONAL DEFICIENCIES OVERVIEW

This section outlines the known functional discrepancies between the PM5313 SPECTRA-622 revision B production release device and the Issue 6 SPECTRA-622 datasheet. The errata are explained in more detail in sections 3 of this document. Please note that the errata contained in this document are preliminary.

Table 1 FUNCTIONAL DEFICIENCIES SUMMARY LIST

#	Discrepancy	Workaround?	Modes Affected
3.1 Rx Alarms			
3.1.1	Invalid PRDI code insertion	Yes	Rx PRDI codes
3.1.2	Rx alarms consequential action clearing	Yes	STS-12c mode, STS-3c mode

3 SPECTRA-622 REVISION B FUNCTIONAL DEFICIENCY DETAILS

3.1 Rx Alarms

3.1.1 Invalid PRDI code insertion

Description

For concatenated applications, PRDI & Enhanced PRDI codes for LOPCON and PAISCON are not reported correctly (for local reporting and RAD).

Workarounds

Correct RDI/ERDI events can be forced

- In software, by polling the LOPCON and PAISCON alarm indications in registers of slave slices, then forcing Path RDI/ERDI in the transmit stream by setting PERDIEN, PERDISRC (register 1n50h) PFDI, PERDI6, and PERDI7 (register 1n59h) according to the application requirements and Table 13 in the description of register 1n59h.

- In hardware, by monitoring the RDI/ERDI indications in the slave timeslots of the RAD port, and using external hardware (FPGA/CPLD) to set the RDI/ERDI bit times in the master timeslot of the TAD port.

Performance without workaround

- RDI and ERDI are not automatically asserted in the transmit stream of SPECTRA 622 when the receive path is in LOPCON or PAISCON alarm.

- On RAD port, correct PRDI values are observed on slave time slots but not on the master timeslot.

3.1.2 Receive Alarm Consequential Actions Clearing

Description

On the Drop bus, PAIS consequential action takes 10 frames to clear when exiting any received path error condition in STS-12c (STM-4-4c) mode, and 3 frames to clear when exiting loss of pointer (LOP) condition in STS-3c (STM-1/AU4) mode.

Workaround

Path BIP errors (B3) and H1, H2 values should be monitored on the Drop bus to ensure that the PAIS alarm condition has cleared, and that the Drop bus is again carrying valid payload and pointer.

Performance without Workaround

SPECTRA-622 will output an enabled NDF and a valid pointer value on the Drop bus when the path error condition has been cleared. However, the all-ones alarm indication is not cleared in all the path-processing slices until 10 frames after the enabled NDF appears. Therefore, the payload and concatenation indicators will be temporarily corrupted. After 10 frames, a valid pointer (with no enabled NDF), payload, and concatenation indicators are output on the Drop bus. The transition from PAIS to valid data cannot be easily detected without monitoring overhead.

4 SPECTRA-622 ISSUE 6 DATASHEET ERRATA

This section contains errata in the issue 6 SPECTRA-622 datasheet.

1. unaltered text is unchanged to add context to changes
2. ***new material is bold and italicized***
3. ~~***deleted material is bold and italicized with strikethrough***~~
4. *comments specific to this document are in italics*

4.1 TIU2PERDI Bit not defined

All references to TIU2PERDI bit should be ignored. The TIU2PERDI bit is not defined in the SPECTRA-622 device. Path enhanced RDI assertion due to path trace identifier (mode 1) unstable (TIU) events is enabled via the TIUPERDI bit only (register 0119H). The description of the TIUPERDI bit has not changed, and reads:

TIUPERDI:

When set high, the TIUPERDI bit enables path enhanced RDI assertion when path trace identifier (mode 1) unstable (TIU) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When TIUPERDI is set low, trace identifier (mode 1) unstable events have no effect on path RDI. In addition, this bit has no effect when PERDI_EN is set low.

4.2 DOOL (data out of lock) declaration – page 111

Section 11.1.1 Clock Recovery Unit , should state that the PLL will revert to the reference clock if there are no data transitions after 96 bit periods.

The clock recovery unit recovers the clock from the incoming bit serial data stream. The clock recovery unit is fully compliant with SONET/SDH jitter tolerance requirements. The clock recovery unit utilizes a low frequency reference clock to train and monitor its clock recovery PLL. Under loss of signal conditions, the clock recovery unit will continue to output a line rate clock that is locked to this reference for keep alive purposes. The clock recovery unit utilizes a

77.76 MHz reference clock. The clock recovery unit provides status bits that indicates whether it is locked to data or the reference and also supports diagnostic loopback and a loss of signal input that squelches normal input data.

Initially, the PLL locks to the reference clock, REFCLK+/-. When the frequency of the recovered clock is within 488 ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock, the PLL reverts to the reference clock if no data transitions occur in ~~***80***~~ ***96*** bit periods or if the recovered clock drifts beyond 488 ppm of the reference clock.

4.3 SLLBEN bit description correction – page 145, page 431

The following highlighted text should be removed from section 11.8.3 Transmit Pointer Interpreter Processor (TPIP):

The TPIP is held in reset in DS3 mode, DS3ADDSEL = '1' ~~***and when SLLBEN = '0' (reg 1n00)***~~. When held in reset, TPIP registers cannot be accessed.

In addition, the following highlighted sentence should be removed from the description of the SLLBEN bit in register 1n00H:

SLLBEN:

When set high, the system side line loopback enable bit (SLLBEN) activates line loopback of the receive STS-1 (STM-0/AU3) or equivalent stream processed by the corresponding RPPS. The receive stream replaces the transmit STS-1 (STM-0/AU3) or equivalent stream from the ADD bus. When SLLBEN is set low, system side line loopback of the corresponding receive stream is disabled, the data stream from the ADD bus is processed normally. The system side line loopback can only be enabled when the DS3 ADD Bus stream is disabled via the DS3ADDSEL register bit in the SPECTRA-622 TPPS Path and DS3 configuration register. SLLBEN has not effect when DS3ADDSEL is set high. ~~***When SLLBEN is low, TPIP is held in reset – TPIP registers cannot be accessed.***~~

4.4 TFPI Pin description – page 28

The TFPI pin description should be modified to include timing specifications in parallel mode:

In serial mode, TFPI is sampled on the rising edge of TCLK. ***In parallel mode, TFPI is sampled on the rising edge of TDCK***

4.5 Transmit Transport Overhead Input Timing – page 604

The following highlighted changes should be made to Table 49: Transmit Transport Overhead Input Timing to correctly indicate hold time requirements for the TSOW, TSUC, and TLOW signals.

Table 2 - Transmit Transport Overhead Input Timing

Symbol	Description	Min	Max	Units
t_{STLD}	TLD Set-up Time to TLDCLK	250		ns
t_{HTLD}	TLD Hold Time to TLDCLK	0		ns
t_{STSLD}	TSLD Set-up Time to TSLDCLK	250		ns
t_{HTSLD}	TSLD Hold Time to TSLDCLK	0		ns
t_{STOW}	TSOW, TLOW, TSUC Set-up Time to TOWCLK	250		ns
t_{HTOW}	TSOW, TLOW, TSUC Hold Time to TOWCLK ***(non-gapped mode)***	0		ns
t_{HTOW}	***TSOW, TLOW, TSUC Hold Time to TOWCLK (gapped mode)***	***250***		***ns***
t_{STOH}	TOH Set-up Time to TOHCLK	250		ns
t_{HTOH}	TOH Hold Time to TOHCLK	0		ns
t_{STTOH}	TTOH, TTOHEN Set-up Time to TTOHCLK	17		ns
t_{HTTOH}	TTOH, TTOHEN Hold Time to TTOHCLK	0		ns

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