PM5315

SPECTRA-2488™

SONET/SDH Payload Extractor/Aligner

Errata

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U.S. Patent No. 5,640,398

Canadian Patent No. 2,161,921

Relevant patent applications and other patents may also exist.

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Revision History

Issue No.	Issue Date	Details of Change
Issue 3	November 2001	Removed Erratum 3.1, 3.2, 3.4, 3.6 – 3.11, 3.13 – 3.15, 3.17 - 3.22, 3.24 – 3.25 and 3.27 from Issue 2 Added Erratum 3.8, 3.9, 4.1, 4.2 Updated Errata item 3.16 of Issue 2 with 3.7
Issue 2	July 2001	Added 'Fix in RevB' column to deficiencies overview. Added erratum 3.21 – 3.28, 4.1 – 4.10.
Issue 1	February 2001	Document created.

Table of Contents

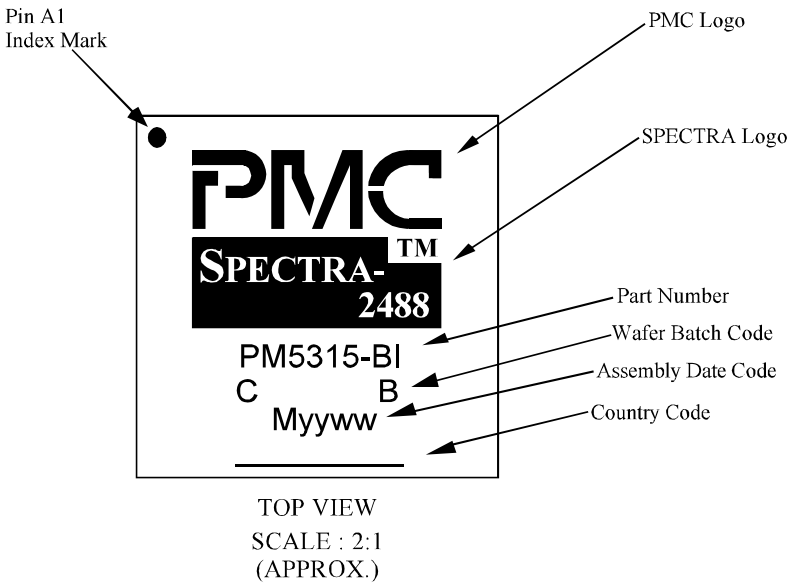
1 Issue 3 Errata

This document is the errata notice for Revision B of the SPECTRA-2488™ (PM5315-BI) device and issue 4 of the SPECTRA-2488 data sheet. Issue 4 of the SPECTRA-2488 data sheet (PMC-1990821) and issue 3 of this errata supersede all prior editions and versions of the data sheet.

1.1 Device Identification

The information in this document applies to revision B of the PM5315 SPECTRA-2488 device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1). PM5315 SPECTRA-2488 Revision B is packaged in a 520-pin Super-BGA package.

Figure 1 PM5315 SPECTRA-2488 Branding Format



2 Overview of Functional Deficiencies

This section outlines the known functional discrepancies between the PM5315 SPECTRA-2488 revision B device and issue 4 of the SPECTRA-2488 datasheet. The errata are explained in more detail in section 3 of this document.

Table 1 Summary of Functional Deficiencies

#	Discrepancy	Workaround	Affected Modes
3.1	Ring Control Port and RALM Port	Yes	All modes
3.2	Pointer Corruption Coming Out of Concatenated Mode	Yes	Payload reconfiguration
3.3	Transmit Add Bus Pointer Interpreter	Yes	All modes
3.4	J0 Movement Causes Reframing at Line Side	Yes	All modes
3.5	Z0DEF=1 Can Cause Loss of Frame Alignment	Yes	STS-48 mode
3.6	Busy Bits Not Auto-Cleared on Access to Invalid Registers	Yes	All Modes
3.7	New DJ0REF/TFPI Frame Alignment Can Cause Invalid H1/H2 Pointer Value Generation	Yes	All modes
3.8	TPOH Port Data Insertion Corruption	Yes	All modes
3.9	Missing J1 Characters on Drop Telecom Bus	No	All modes

3 Functional Deficiency Details for Revision B of the SPECTRA-2488 Device

3.1 Ring Control Port and RALM Port

Description

When configured for concatenated payloads, the ring control port and RALM port will incorrectly output alarms on slave STS-1s (slave STS-1s are the non master STS-1s in a concatenated stream. That is, an STS-3c will have a master STS-1, and two slave STS-1s).

Workarounds

When the ring control port is used between mate SPECTRA-2488 devices, the mate will filter these unwanted alarms. When using RALM, unwanted alarms on slave STS-1s should be filtered for concatenated payloads.

Performance Without Workaround

There will be no problems when using the ring control port to interconnect a SPECTRA-2488 with a mate SPECTRA-2488 using the ring control port. If this port is to be used to extract path defect conditions, then care must be taken to filter unwanted alarm status from the slave STS-1s.

3.2 Pointer Corruption Coming Out of Concatenated Mode

Description

Pointer corruption may occur when configuring SONET / SDH payload from a concatenated stream to a channelized stream.

Workarounds

Ensure that pointer is recalculated when payload is configured.

After payload configuration:

- Set SVCA indirect register #02 bit 5.
- Clear SVCA indirect register #02 bit 5.

Performance Without Workaround

After reconfiguration from a concatenated to a channelized payload, some receive SONET/SDH Virtual Container Aligners (SVCA) may be in an unknown state where they are incapable of transmitting correct pointers and/or J1 pulses

3.3 Transmit Add Bus Pointer Interpreter

Description

If Transmit Add Bus Pointer Interpreter (TAPI) is disabled while certain path alarms are in the active state (i.e. PAIS, PLOP, PAISC, PLOPC), these alarms will still be seen by the transmit SVCA.

Consequential and automatic (no user control) PAIS will be inserted into the transmit path by the transmit SVCA.

Workarounds

Disable the generation of the LOP-P and AIS-P alarms by the TAPI. Set PAISPTRCFG[1:0] and PLOPTRCFG[1:0] to 11b in register 0x0019.

Performance Without Workaround

Consequential and automatic (no user control) PAIS will be inserted into the transmit path by the transmit SVCA.

3.4 J0 Movement Causes Reframing at Line Side

Description

Movement of the AJ0J1 J0 reference signal on the Add bus will cause a change of frame alignment. This is the expected behavior of the device. In a system where multiple devices on multiple cards are connected to the Add bus of the SPECTRA-2488, there is a risk that extraction or removal of one of the devices will cause a glitch on the J0 reference, thereby forcing an undesired change of frame alignment.

Workarounds

It is the system designer's responsibility to ensure that J0 reference signals coming from the system backplane do not change alignment unless reframing is the desired effect. The SPECTRA-2488 does not require a frame pulse every frame; therefore, a simple workaround would be to gate the J0 reference signals from the backplane until the signal has reached a steady state. Then, compare the incoming J0 reference signal with the previous J0 reference signal (for instance, in a flywheel counter within an FPGA.) The FPGA could then raise an alarm (in the case where the alignments don't match) and optionally force the new alignment.

In systems where the PM5315 SPECTRA-2488 is connected to a PM5310 TBS device, this is not a problem, since the TBS will ensure that the J0 reference remains stable.

Performance Without Workaround

If the J0 reference signal changes alignment, there will be a change in frame alignment of the SPECTRA-2488. This may be undesirable in cases where live traffic is being carried in 3 of the 4 STS-12 slices, and a tributary card connected to the 4th slice is removed, inserted, or otherwise has an unstable J0 reference signal. If any of the J0 reference signals are changed, reframing will occur because the J0 signals are OR'd together internally.

3.5 Z0DEF=1 Can Cause Loss of Frame Alignment

Description

When Z0DEF=1, the SPECTRA-2488 will insert all zeros in the Z0 byte position. Over the entire STS-48 frame, the long string of 0s may cause the clock and data recovery unit at the far end equipment to fail, resulting in a loss of frame alignment and data.

Workarounds

In the TRMP, set Z0DEF=0 and J0Z0INCEN=1 in registers 0x1080, 0x1480, 0x1880, 0x1C80. This will force an incrementing pattern to be inserted in the Z0 byte position, ensuring transition density at the line side.

An alternate workaround is to set Z0DEF=0, J0Z0INCEN=0 in registers 0x1080, 0x1480, 0x1880, 0x1C80. Set Z0V[7:0] in registers 0x1083, 0x1483, 0x1883 and 0x1C83 to a pattern other than all zeros or all ones. Set Z0REGEN in registers 0x1081, 0x1481, 0x1881 and 0x1C81. This will force a set pattern to be inserted into the Z0 byte position, ensuring transition density at the line side.

If the above workarounds are not acceptable, a third workaround is to use the overhead insertion port on the device to gain full control over the transport overhead.

Performance Without Workaround

Without the workaround, the far end framer may lose frame alignment.

3.6 Busy Bits Not Auto-cleared on Access to Invalid Registers

Description

If an access to an invalid indirect register location is attempted, the BUSY bit for that set of indirect registers will remain high until a valid access is performed. An example of this would be if an attempt was made to access Indirect register 0x01 in the TTTP SECTION set of indirect registers. The corresponding BUSY bit (direct register 0x10A0, bit 15) would be set and remain set until such time that an access was made to a valid location in the TTTP SECTION indirect registers (for instance, 0x00).

Workarounds

There is no workaround. Software should ensure that invalid indirect register locations are not accessed.

3.7 New DJ0REF/TFPI Frame Alignment Can Cause Invalid H1/H2 Pointer Value Generation

Description

The DJ0REF pulse is used by the SPECTRA-2488 to set the frame alignment on the DROP TelecomBus. The TFPI input is used by the SPECTRA-2488 to set the frame alignment on the transmit line side. These pulses are expected to be 8 kHz cyclic pulses, distributed once every 125us (or multiple of this time). This reference pulse *must* remain fixed. Exactly one pulse every 9720 DCK clock cycles or multiple of 9720 for DJ0REF. Exactly one pulse every 9720 TDCLK clock cycles or multiple of 9720 for 4xOC12 mode. Exactly one pulse every 19440 TDCLK cycles or multiple of 19440 for OC48 mode.

The DJ0REF pulse is used in conjunction with the RJ0FP inputs of the PM5310 TBS and PM5372 TSE devices to set the switch fabric's frame alignment. The probability of error is very low; on the order of 10^-6. Changes in the SPECTRA-2488 frame alignment via the DJ0REF and TFPI pulses from their original position/setting can cause the H1/H2 pointer bytes to be invalid. The problem is characterized by H1 and H2 bytes containing a pointer value that corresponds to the true J1 byte location minus one. As a result, downstream devices will report B3 errors when interpreting the SPE location via the H1 and H2 bytes and payload will not be located correctly.

The J1 pulse on the DJ0J1 output will correctly mark the start of the SPE and can be used by other devices that support the J1 control pulse to locate the SPE. A CHESS-I fabric with the TBS and TSE configured for HPT mode will allow the SPE to be located correctly. But CHESS I devices configured in MST mode will not allow the correct determination of the SPE location. Interfacing the SPECTRA-2488 to a CHESS II fabric with the TBS-9953 and TSE-160 devices configured for 2.488 Gbps SONET scrambled links will not support the J1 control character and the H1/H2 bytes must be interpreted to locate the SPE for each STS-1/AU-3 path.

Workarounds

This issue is specifically a start up/reset problem. As long as the DJ0REF and TFPI frame pulses are consistent, the H1/H2 values will continue to be generated correctly. Any slip in the frame pulse +/- 1 DCK clock cycle (DJ0REF) or +/- 1 TDCLK clock cycle (TFPI) from the original frame pulse position will result in payload corruption.

After an initial or a new frame pulse has been intentionally provided to the DJ0REF and TFPI inputs, initiate an SVCA reset by setting and clearing the PTRRST bits in the SVCA Diagnostic/Configuration Indirect Register 02H for *all* STS-1/AU-3 paths. Either the transmit or receive SVCA will require this workaround depending on which input (DJ0REF or TFPI) underwent the frame alignment setting/change. This will prevent any incorrect pointer values from being generated. Once this reset is issued, there is no reason to redistribute this reset until a subsequent device reset or change in system or line side frame alignments has occurred.

Performance Without Workaround

The H1 and H2 bytes may contain an incorrect pointer value that will cause downstream pointer interpreters to determine an incorrect payload location and result in B3 errors and other path level errors.

3.8 TPOH Port Data Insertion Corruption

Description

When inserting POH via the TPOH port, switching back and forth between TPOH port insertion and POH pass through from the ADD TelecomBus can cause corruption on the POH bytes going to the transmit line side of the SPECTRA-2488. The corruption will occur for one frame after the POH source has changed, the new POH source data will be inserted correctly. All POH bytes that are not inserted via register control will experience this issue.

Workarounds

When inserting POH, maintain consistent insertion via either the TPOH port, or via internal register configuration. When using the TPOH port, ensure that the POH data is only inserted into the TPOH port once the TPOHRDY signal is asserted to indicate that the SPECTRA-2488 is prepared to accept the POH serial data stream.

Performance Without Workaround

Constant toggling between TPOH and POH pass through from the ADD TelecomBus will result in POH corruption for one frame after the transition.

3.9 Missing J1 Characters on Drop Telecom Bus

Description

When NDFs (New Data Flags) are received by the Spectra-2488, J1 may fail to appear at the Drop Telecom Bus for the current frame. J1 will be indicated on the next frame however. If NDFs are continuously received, J1 may continuously fail to appear at the Drop Telecom Bus, but will always appear on the frame following the last NDF. Note, however, that H1/H2 will always be generated correctly.

NDFs would occur, for example, during an APS switchover or a reconfiguration of the path.

Workarounds

Under the conditions where NDFs would occur, data loss is expected. The device connected to the drop side of the Spectra-2488 should re-synchronize to the next J1 character.

4 Documentation Deficiency List

4.1 SVCA Indirect Register Behaviour Clarification

When configured for concatenated payloads, the value written to SVCA indirect register 2 (diagnostics) of a master timeslot is automatically propogated to the indirect register 2 of all slave timeslots. This is the expected behaviour of the device, and is written here for clarification.

4.2 SARC Register Description Clarification

The SARC block is accessed through registers 0260H – 027DH for STS-12#1. The registers are indexed on the PATH[3:0] bits in register 0260H. Therefore, it should be noted that registers 0262H, 0263H… have a different meaning, depending on the setting of register 0260H.