

# DATA SHEET

**74LVC2G86**

Dual 2-input exclusive-OR gate

Product specification

2003 Aug 25

## Dual 2-input exclusive-OR gate

## 74LVC2G86

## FEATURES

- Wide supply voltage range from 1.65 to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 to 1.95 V)
  - JESD8-5 (2.3 to 2.7 V)
  - JESD8B/JESD36 (2.7 to 3.6 V)
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- SOT505-2 package
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from  $-40$  to  $+85$  °C and  $-40$  to  $+125$  °C.

## DESCRIPTION

The 74LVC2G86 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

This device is fully specified for partial power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC2G86 provides the dual 2-input exclusive-OR gate.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay inputs nA, nB to outputs nY	$V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ k $\Omega$	3.8	ns
		$V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ $\Omega$	2.5	ns
		$V_{CC} = 2.7$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	3.0	ns
		$V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	2.3	ns
		$V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	1.9	ns
$C_I$	input capacitance		2.5	pF
$C_{PD}$	power dissipation capacitance per gate	$V_{CC} = 3.3$ V; notes 1 and 2	15.8	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

2. The condition is  $V_i = \text{GND}$  to  $V_{CC}$ .

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**FUNCTION TABLE**

See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

**Note**

- H = HIGH voltage level;  
L = LOW voltage level.

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC2G86DP	-40 to +125 °C	8	TSSOP8	plastic	SOT505-2	V86

**PINNING**

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	2Y	data output
4	GND	ground (0 V)
5	2A	data input
6	2B	data input
7	1Y	data output
8	V <sub>CC</sub>	supply voltage

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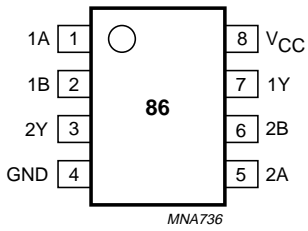


Fig.1 Pin configuration.

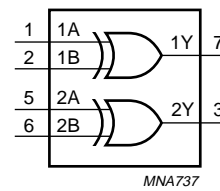


Fig.2 Logic symbol.

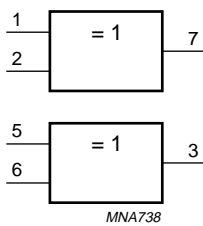


Fig.3 Logic symbol (IEEE/IEC).

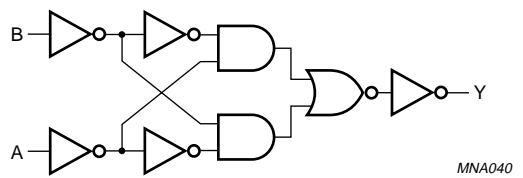


Fig.4 Logic diagram (one driver).

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	active mode	0	$V_{CC}$	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
$T_{amb}$	operating ambient temperature		-40	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 1.65$ to $2.7$ V	0	20	ns/V
		$V_{CC} = 2.7$ to $5.5$ V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input diode current	$V_I < 0$	-	-50	mA
$V_I$	input voltage	note 1	-0.5	+6.5	V
$I_{OK}$	output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
$V_O$	output voltage	active mode; notes 1 and 2	-0.5	$V_{CC} + 0.5$	V
		Power-down mode; notes 1 and 2	-0.5	+6.5	V
$I_O$	output source or sink current	$V_O = 0$ to $V_{CC}$	-	±50	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	±100	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_D$	power dissipation	$T_{amb} = -40$ to $+125$ °C	-	300	mW

## Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When  $V_{CC} = 0$  V (Power-down mode), the output voltage can be 5.5 V in normal operation.

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.65 to 1.95	0.65 × V <sub>CC</sub>	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V <sub>CC</sub>	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V <sub>CC</sub>	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	1.65 to 5.5	–	–	0.1	V
		I <sub>O</sub> = 4 mA	1.65	–	0.07	0.45	V
		I <sub>O</sub> = 8 mA	2.3	–	0.12	0.3	V
		I <sub>O</sub> = 12 mA	2.7	–	0.17	0.4	V
		I <sub>O</sub> = 24 mA	3.0	–	0.33	0.55	V
		I <sub>O</sub> = 32 mA	4.5	–	0.39	0.55	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 μA	1.65 to 5.5	V <sub>CC</sub> - 0.1	–	–	V
		I <sub>O</sub> = -4 mA	1.65	1.2	1.54	–	V
		I <sub>O</sub> = -8 mA	2.3	1.9	2.15	–	V
		I <sub>O</sub> = -12 mA	2.7	2.2	2.50	–	V
		I <sub>O</sub> = -24 mA	3.0	2.3	2.62	–	V
		I <sub>O</sub> = -32 mA	4.5	3.8	4.11	–	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	5.5	–	±0.1	±5	μA
I <sub>off</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	–	±0.1	±10	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	0.1	10	μA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.3 to 5.5	–	5	500	μA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.65 to 1.95	0.65 × V <sub>CC</sub>	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V <sub>CC</sub>	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V <sub>CC</sub>	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	1.65 to 5.5	–	–	0.1	V
		I <sub>O</sub> = 4 mA	1.65	–	–	0.70	V
		I <sub>O</sub> = 8 mA	2.3	–	–	0.45	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.60	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.80	V
		I <sub>O</sub> = 32 mA	4.5	–	–	0.80	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 μA	1.65 to 5.5	V <sub>CC</sub> - 0.1	–	–	V
		I <sub>O</sub> = -4 mA	1.65	0.95	–	–	V
		I <sub>O</sub> = -8 mA	2.3	1.7	–	–	V
		I <sub>O</sub> = -12 mA	2.7	1.9	–	–	V
		I <sub>O</sub> = -24 mA	3.0	2.0	–	–	V
		I <sub>O</sub> = -32 mA	4.5	3.4	–	–	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	5.5	–	–	±20	μA
I <sub>off</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	–	–	±20	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	40	μA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.3 to 5.5	–	–	5000	μA

**Note**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

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AC CHARACTERISTICS

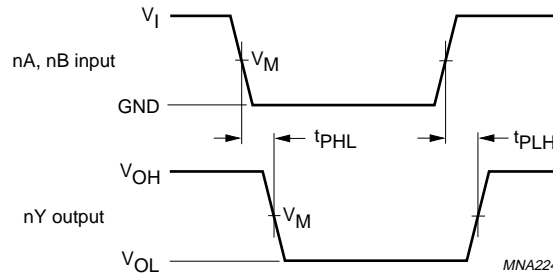
GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay inputs nA, nB to outputs nY	see Figs 5 and 6	1.65 to 1.95	1.4	3.8	9.9	ns
			2.3 to 2.7	0.8	2.5	5.7	ns
			2.7	0.8	3.0	5.7	ns
			3.0 to 3.6	0.8	2.3	4.7	ns
			4.5 to 5.5	0.6	1.9	3.6	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay inputs nA, nB to outputs nY	see Figs 5 and 6	1.65 to 1.95	1.4	3.8	12.4	ns
			2.3 to 2.7	0.8	2.5	7.2	ns
			2.7	0.8	3.0	7.2	ns
			3.0 to 3.6	0.8	2.3	5.9	ns
			4.5 to 5.5	0.6	1.9	4.5	ns

Note

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

AC WAVEFORMS



V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.65 to 1.95 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns
2.3 to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns

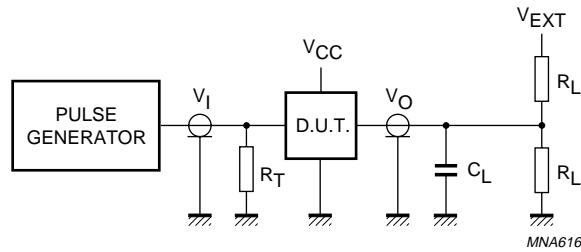
V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.5 The inputs nA, nB to outputs nY propagation delays and the output transition times.



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V <sub>CC</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>EXT</sub>		
				t <sub>PLH</sub> /t <sub>PHL</sub>	t <sub>PZH</sub> /t <sub>PHZ</sub>	t <sub>PZL</sub> /t <sub>PLZ</sub>
1.65 to 1.95 V	V <sub>CC</sub>	30 pF	1 kΩ	open	GND	2 × V <sub>CC</sub>
2.3 to 2.7 V	V <sub>CC</sub>	30 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 to 5.5 V	V <sub>CC</sub>	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>

Definitions for test circuit:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

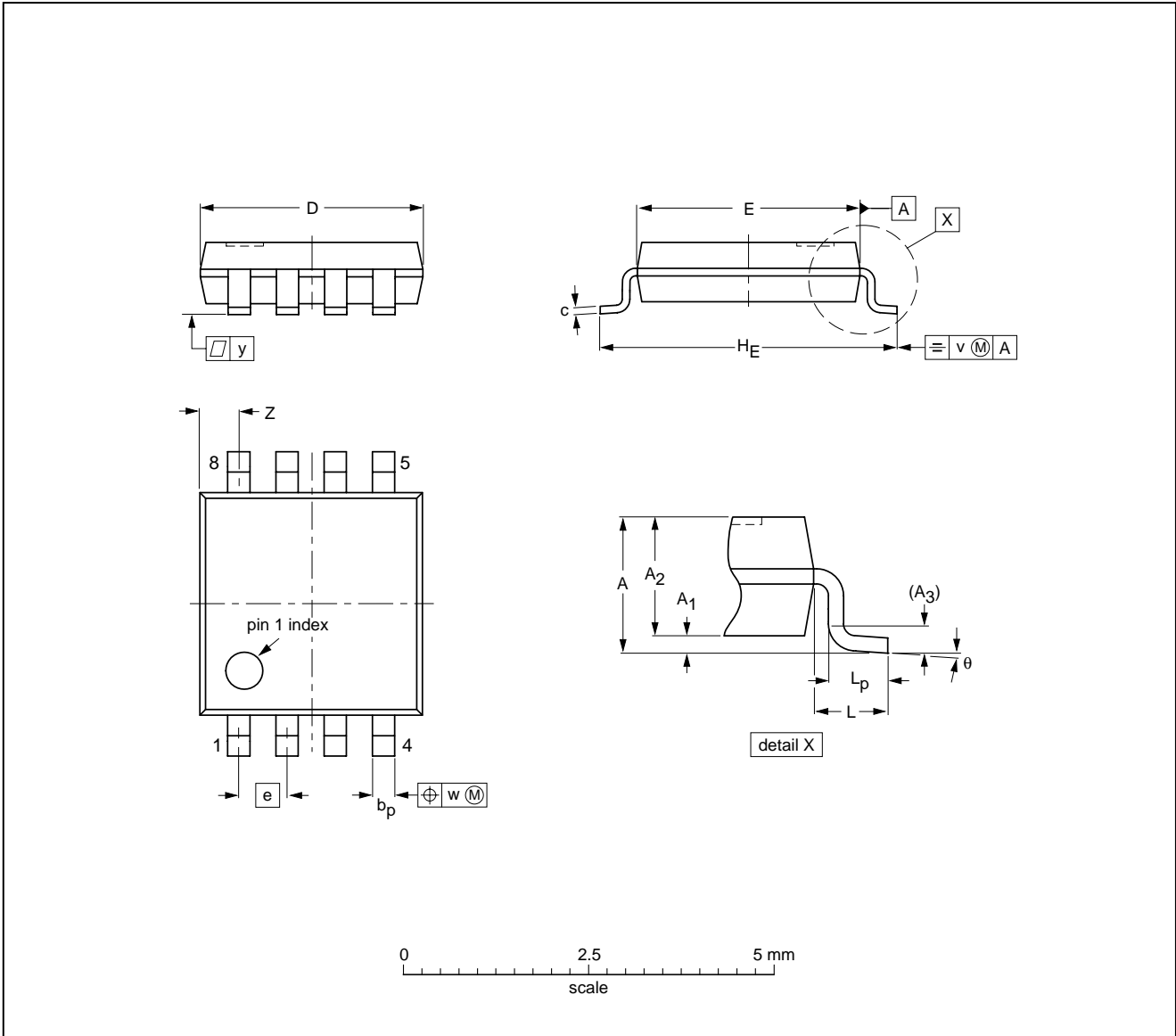
Fig.6 Load circuitry for switching times.

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PACKAGE OUTLINE

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT505-2		---			02-01-16

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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