AN1149NFHK

6-ch DC-DC Converter

■ Overview

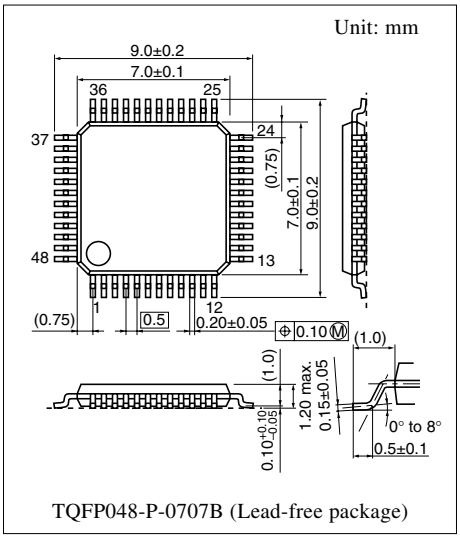
4 channels of step-up, 1 channel of step-down and 1 channel of step-up/down voltage, 6 channels in total have been integrated onto a single chip. Each channel can be remote-controlled and work with two dry cells. A high precision output voltage can be obtained thanks to the accurate reference of V_{REF} ±1%.

■ Features

- Low voltage operation (1.5 V min.)
- High precision reference voltage (±1%)
- Remote control for each channel

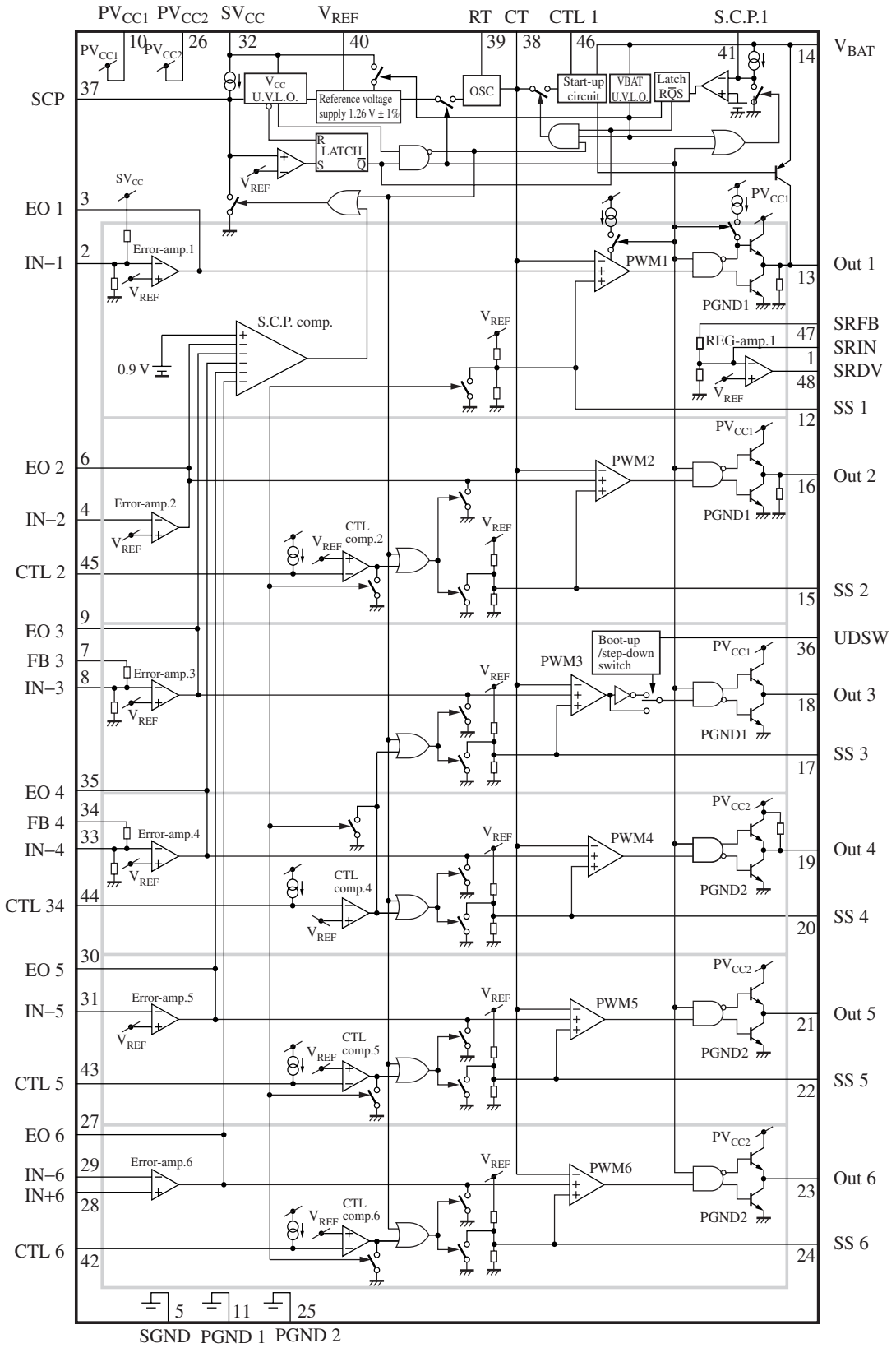
■ Applications

- Digital still cameras



TQFP048-P-0707B (Lead-free package)

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	SRIN	Regulator amplifier input pin	27	EO 6	Output pin for part-6 error amplifier
2	IN−1	Inverse input for part-1 error amplifier	28	IN+6	Non-inverted input pin for part-6 error amplifier
3	EO 1	Output for part-1 error amplifier	29	IN−6	Inverted input pin for part-6 error amplifier
4	IN−2	Inverse input for part-2 error amplifier	30	EO 5	Output pin for part-5 error amplifier
5	SGND	Signal GND pin	31	IN−5	Inverted input pin for part-5 error amplifier
6	EO 2	Output for part-2 error amplifier	32	SV_{CC}	Supply voltage application pin for signal block
7	FB 3	CH 3 output voltage detection pin	33	IN−4	Inverted input pin for part-4 error amplifier
8	IN−3	Inverse input for part-3 error amplifier	34	FB 4	CH 4 output voltage detection pin
9	EO 3	Output for part block-3 error amplifier	35	EO 4	Output pin for part-4 error amplifier
10	PV_{CC1}	Voltage application pin 1 for output block	36	UDSW	Step-down output setup pin for CH 3
11	PGND1	Output GND pin 1	37	SCP	Short-circuit protection time constant setup capacitance connection pin for CH 2-6
12	SS-1	CH 1 soft start setting pin			
13	Out-1	Push-pull output pin for out-1 block	38	CT	Oscillator frequency setup capacitor connection pin
14	V_{BAT}	Battery voltage application pin			
15	SS-2	CH 2 soft start setting pin	39	RT	Oscillator frequency setup resistor connection pin
16	Out-2	Totem pole output pin for out-2 block			
17	SS-3	CH 3 soft start setting pin	40	V_{REF}	Reference voltage output pin
18	Out-3	Totem pole output pin for out-3 block	41	SCP 1	Output short-circuit protection time constant setup capacitor connection pin for CH 1
19	Out-4	Totem pole output pin for out-4 block			
20	SS-4	CH 4 soft start setting pin	42	CTL 6	CH 6. on-off control pin
21	Out-5	Totem pole output pin for out-5 block	43	CTL 5	CH 5. on-off control pin
22	SS-5	CH 5 soft start setting pin	44	CTL 34	CH 3, CH 4. on-off control pin
23	Out-6	Totem pole output pin for out-6 block	45	CTL 2	CH 2. on-off control pin
24	SS-6	CH 6 soft start setting pin	46	CTL 1	CH 1. on-off control pin
25	PGND2	Output GND pin 2	47	SRFB	Regulator amplifier output voltage detection pin
26	PV_{CC2}	Voltage application pin 2 for output block	48	SRDV	Regulator amplifier drive pin

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	SV_{CC}	9.2	V
Power V_{CC1} allowable application voltage	PV_{CC1}	9.2	V
Power V_{CC2} allowable application voltage	PV_{CC2}	9.2	V
Battery input allowable application voltage	V_{BAT}	9.2	V
Allowable application voltage to regulator output voltage detection input pin	V_{SRFB}	SV_{CC}	V

Note) 1. Do not apply external currents or voltages to any pins not specifically mentioned.
For the circuit currents, '+' denotes current flowing into the IC, and '−' denotes current flowing out of the IC.
2. Except for the power dissipation, operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

■ Absolute Maximum Ratings (continued)

Parameter	Symbol	Rating	Unit
Step up / down switch input allowable application voltage *2	V_{UDSW}	SV_{CC}	V
Allowable application voltage to output voltage detection input 3	V_{FB3}	SV_{CC}	V
Allowable application voltage to output voltage detection input 4	V_{FB4}	SV_{CC}	V
Allowable application voltage to control input 1	V_{CTL1}	V_{BAT}	V
Allowable application voltage to control input 2	V_{CTL2}	SV_{CC}	V
Allowable application voltage to control input 3, 4	V_{CTL34}	SV_{CC}	V
Allowable application voltage to control input 5	V_{CTL5}	SV_{CC}	V
Allowable application voltage to control input 6	V_{CTL6}	SV_{CC}	V
Error amplifier allowable application voltage to input pin	V_{IN}	− 0.2 to SV_{CC}	V
Supply current	I_{CC}	—	mA
Output 2 allowable peak current	I_{OP2}	±400	mA
Output 3 allowable peak current	I_{OP3}	±400	mA
Output 4 allowable peak current	I_{OP4}	±400	mA
Output 5 allowable peak current	I_{OP5}	±400	mA
Output 6 allowable peak current	I_{OP6}	±400	mA
Output 1 allowable sequence current	I_{O1}	−50	mA
Output 2 allowable sequence current	I_{O2}	±100	mA
Output 3 allowable sequence current	I_{O3}	±100	mA
Output 4 allowable sequence current	I_{O4}	±100	mA
Output 5 allowable sequence current	I_{O5}	±100	mA
Output 6 allowable sequence current	I_{O6}	±100	mA
Reference voltage allowable application current	I_{REF}	−5	mA
Power dissipation *1	P_D	160	mW
Operating ambient temperature	T_{opr}	−20 to +85	°C
Storage temperature	T_{stg}	−55 to +125	°C

Note) 1. Do not apply external currents or voltages to any pins not specifically mentioned.
For the circuit currents, '+' denotes current flowing into the IC, and '−' denotes current flowing out of the IC.

2. Except for the power dissipation, operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

3. ∗1: T_a = 85°C. For the independent IC without a heat sink. Note that applications must observe the derating curve for the relationship between the IC power consumption and the ambient temperature.

∗2: Allowable application voltage shall be 8.2 V or less when $SV_{CC} \geq 8.2$ V.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{BAT}	1.5 to 9	V
	SV_{CC}	4.5 to 9	V

■ Recommended Operating Conditions

Parameter	Symbol	Range	Unit
Out-1 source current	I_{OUT1}	30 (max.)	mA
Out-2 to Out-6 peak current	$I_{OUT2\ to\ 6}$	–400 to 400	mA
Timing resistance	R_T	8 to 100	kΩ
Timing capacitance	C_T	560 (fixed)	pF
Oscillation frequency	f_{OUT}	100 to 1 000	kHz
Short-circuit protection time constant setting capacitance	$C_{SCP1, 2}$	1 000 (min.)	pF

■ Electrical Characteristics at V_{BAT} = 3 V, SV_{CC} = PV_{CC1} = PV_{CC2} = 5 V, C_{REF} = 0.1 µF, T_a = 25°C

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Reference voltage							
Reference voltage	V_{REF}	I_{REF} = – 0.1 mA		1.247	1.26	1.273	V
Line regulation	Line	V_{CC} = 4.5 V to 9 V		—	3	20	mV
Load regulation	Load	I_{REF} = – 0.1 mA to –1 mA		–20	–5	—	mV
SV_{CC} low voltage protection							
Circuit operation start voltage	SV_{CCON}			3.9	4.1	4.3	V
Circuit operation stop voltage	SV_{CCOFF}			3.7	3.9	4.1	V
V_{BAT} low voltage protection							
Circuit operation start voltage	V_{BATON}			1.36	1.43	1.5	V
Circuit operation stop voltage	V_{BATOFF}			1.33	1.39	1.45	V
Oscillator							
CH 1 oscillation frequency at startup	f_{ST}	CT = 560 pF SV_{CC} = PV_{CC1} = PV_{CC2} = 1 V		55	80	105	kHz
CH 1 to CH 6 oscillation frequency	$f_{OUT1\ to\ 6}$	RT = 20 kΩ CT = 560 pF		490	540	590	kHz
Output block							
CH 1 to CH 6 output maximum	$D_{U1\ to\ 6}$	RT = 20 kΩ	CH 4	78	84	90	%
duty ratio		CT = 560 pF	except CH 4	82	88	94	%
CH 1 output duty ratio at startup	D_{UST}	CT = 560 pF SV_{CC} = PV_{CC1} = PV_{CC2} = 1 V		60	68	76	%
Output high voltage 1 (CH 1)	V_{OH1}	I_{OUT1} = 20 mA		V_{CC} – 2	—	—	V
Output source current	I_{OL1}	V_{OUT1} = 0.7 V		20	—	—	mA
Output high voltage 2 to 6 (CH 2 to CH 6)	$V_{OH2\ to\ 6}$	$I_{OUT2\ to\ 6}$ = – 0.1 mA		V_{CC} – 1	—	—	V
Output low voltage 2 to 6 (CH 2 to CH 6)	$V_{OL2\ to\ 6}$	$I_{OUT2\ to\ 6}$ = 0.1 mA		—	—	1	V

■ Electrical Characteristics at V_{BAT} = 3 V, SV_{CC} = PV_{CC1} = PV_{CC2} = 5 V, C_{REF} = 0.1 µF, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output block (continued)						
Output high voltage at standby (CH 3, CH 4)	$V_{OHS3, 4}$	$I_{OUT3, 4}$ = − 0.1 mA	V_{CC} − 1	—	—	V
Output low voltage at standby (CH 2, CH 3, CH 5, CH 6)	$V_{OLS2 to 6}$	$I_{OUT2, 3, 5, 6}$ = 0.1 mA	—	—	1.0	V
CH 3 output setup block						
Threshold voltage	V_{CTH}		1.56	1.96	2.36	V
Error amplifier (CH 1 to CH 6)						
Input threshold voltage 1 to 6	$V_{TH1 to 6}$		1.241	1.26	1.279	V
Input bias current 2, 5, 6	$I_{B2, 5, 6}$		− 0.22	− 0.12	—	µA
High-level output voltage 1 to 6	$V_{EH1 to 6}$		1.0	—	—	V
Low-level output voltage 1 to 6	$V_{EL1 to 6}$		—	—	0.2	V
Output source current 1 to 6	$I_{SO1 to 6}$		–45	–38	–32	µA
Output sink current 1 to 6	$I_{SI1 to 6}$		0.5	—	—	mA
CH 6 offset voltage	V_{OFF6}		–6	—	6	mV
CH 1, CH 3, CH 4 output detection resistance division ratio	$R_{O1, 3, 4}$		–1	—	1	%
CH 1 short-circuit protection circuit block						
Pin voltage at standby	V_{STB1}		—	—	0.1	V
Latch threshold voltage	V_{LTH1}		0.27	0.3	0.33	V
Pin voltage at latch operation	V_{SLT1}		—	—	0.1	V
Charge current	I_{CHG1}	V_{SCP1} = 0 V	–3.1	–2.4	–1.7	µA
CH 2 to CH 6 short-circuit protection circuit block						
Pin voltage at standby	V_{STB1}		—	—	0.1	V
Latch threshold voltage 2 to 6	$V_{LTH2 to 6}$		0.8	0.9	1.0	V
Pin voltage 2 to 6 at latch operation	$V_{SLT2 to 6}$		—	—	0.1	V
Charge current	I_{CHG1}	V_{SCP} = 0 V	–1.53	–1.2	– 0.87	µA
Control						
Pin current (CH 2, CH 34, CH 5, CH 6)	$I_{CTL2 to 6}$		–1.53	–1.2	– 0.87	µA
CH 1 threshold voltage	V_{CTL1}		—	1.0	1.5	V
CH 2, CH 34, CH 5, CH 6 threshold voltage	$V_{CTL2 to 6}$		1.07	1.26	1.45	V
Regulator amplifier						
Output high voltage	V_{HRA}	V_{CC} = 5 V I_{SRDV} = 10 mA	—	—	1	V
Pin voltage when external PNP transistor is connected	V_{RA}	SV_{CC} = 5.5 V to 7.5 V	4.9	5.0	5.1	V
Output detection resistance division ratio	ROR		–1	—	1	%

■ Electrical Characteristics at V_{BAT} = 3 V, SV_{CC} = PV_{CC1} = PV_{CC2} = 5 V, C_{REF} = 0.1 µF, T_a = 25°C (continued)

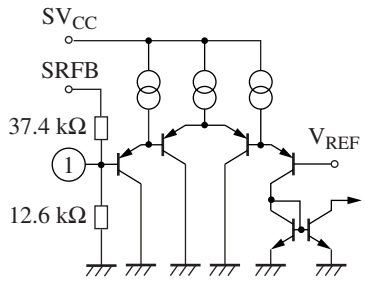
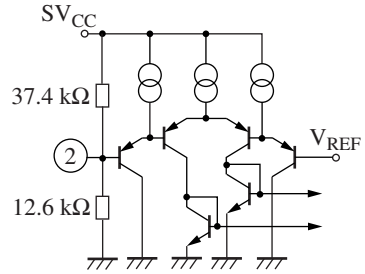
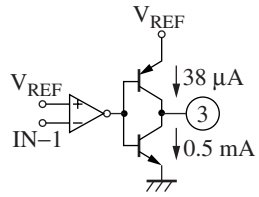
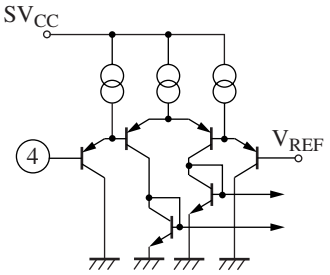
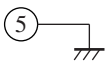
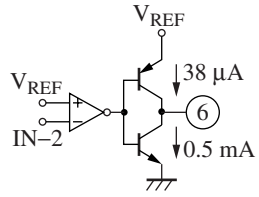
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current consumption						
Current consumption at startup	I_{BAT}	V_{BAT} = 3 V SV_{CC} = 1 V	—	440	655	µA
Average current consumption	$I_{CC(AV)}$	Duty = 50%	—	9	12	mA
Standby current	I_{SB}	V_{BAT} = 3 V, SV_{CC} = 1 V V_{CTL1} = 0 V	34	42	50	µA

• Design reference data

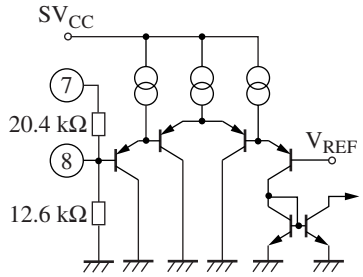
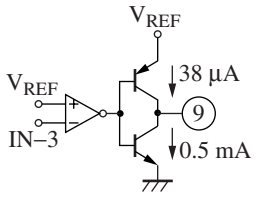
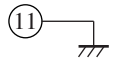
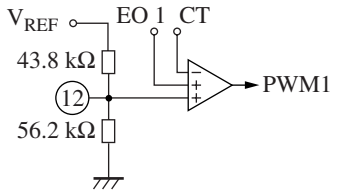
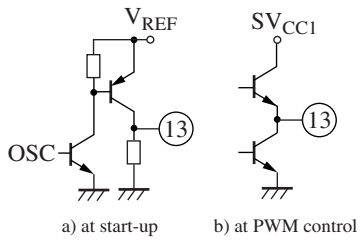
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference voltage						
V_{REF} temperature characteristics	V_{REFdT}	T_a = −20°C to 85°C	−1.5		+1.5	%
RT pin voltage	V_{RT}			0.7		V
SV_{CC} low voltage protection						
Voltage difference between operation start and stop	ΔSV_{CC}	$SV_{CCON} - SV_{CCOFF} > 0$		0.2		V
V_{BAT} low voltage protection						
Voltage difference between operation start and stop	ΔV_{BAT}	$V_{BATON} - V_{BATOFF} > 0$		0.04		V
Error amplifier (CH 1 to CH 6)						
VTH temperature characteristics	V_{THdT}	T_a = −30°C to 85°C	−1.5		+1.5	%
Open loop gain	A_V			80		dB
Oscillator						
Frequency supply voltage characteristics	f_{dV}	V_{CC} = 4.5 V to 9 V RT = 20 kΩ, CT = 560 pF	−16		+16	%
Frequency temperature characteristics	f_{dT}	T_a = −30°C to 85°C RT = 20 kΩ, CT = 560 pF	−3		+3	%
Short-circuit protection circuit						
Comparator threshold voltage	V_{THS}			1.26		V
Control (CTL 1)						
CTL 1 pin current	I_{CTL1}	V_{CTL1} = 3 V		230		µA

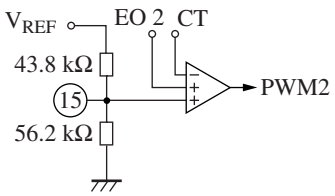
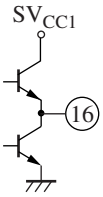
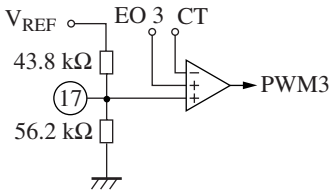
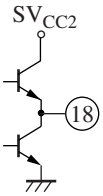
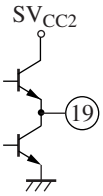
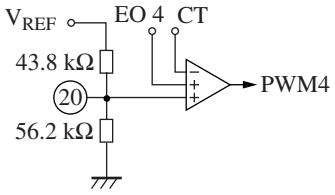
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	I/O
1		SRIN : Output voltage detection pin / inverting input pin for regulator amplifier. 12.6 kΩ built in between SRIN and SGND, 37.4 kΩ between SRIN and SRFB.	I
2		IN−1 : Non-inverting input pin for CH 1 error amplifier 1. 12.6 kΩ built in between IN-1 and SGND, and 37.4 kΩ between IN-1 and SV_{CC}. Set CH 1, DC-DC output to 5 V.	I
3		EO 1 : Output pin for CH 1 error amplifier. Source current: −38 µA, sink current: min. 0.5 mA.	O
4		IN−2 : Non-inverting input pin for CH 2 error amplifier.	I
5		SGND : Signal GND pin.	—
6		EO 2 : Output pin for CH 2 error amplifier. Source current: −38 µA, sink current: min. 0.5 mA.	O

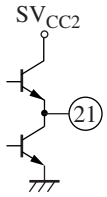
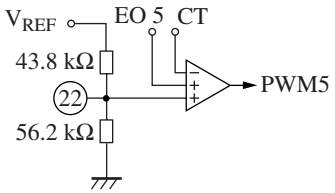
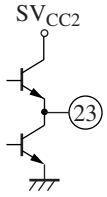
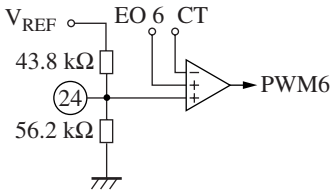
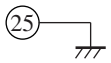
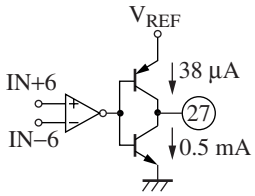
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
7		FB 3 : CH 3 output voltage detection pin. 12.6 kΩ built in between IN-3 and SGND, and 20.4 kΩ between IN-3 and FB 3. DC-DC output of CH 3 is set to 3.3 V.	I
8		IN−3 : Non-inverting input pin for CH 3 error amplifier 3.	I
9		EO 3 : Output pin for CH 3 error amplifier. Source current: −38 µA, sink current: min. 0.5 mA.	O
10		PV_{CC1} : CH 1, CH 2 power supply pin for output block.	—
11		PGND1 : CH 1, CH 2 output block GND pin.	—
12		SS 1 : CH 1 soft start time setting pin. Connect a capacitor between this pin and GND. CH 1 max. duty ratio is set to 88% (in-house), but max. of on period can be adjusted by connecting a resistor between this pin and V_{REF} pin. See Application Notes [3] 8.	I
13		Out 1 : Output SW Tr. driver pin at start-up and push-pull output pin at PWM control. Absolute maximum rating of output source current at PWM is −50 mA.	O
14		V_{BAT} : Battery voltage application pin.	—

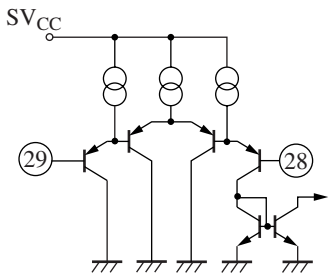
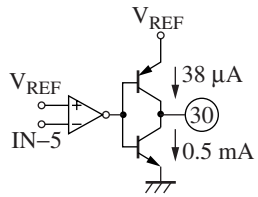
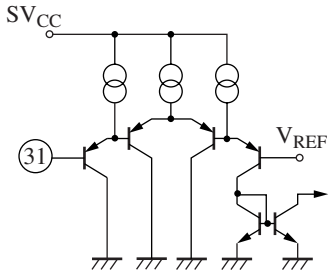
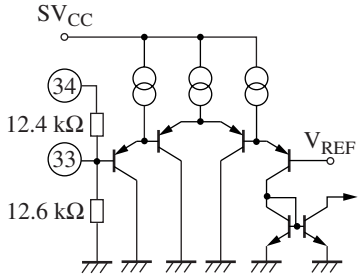
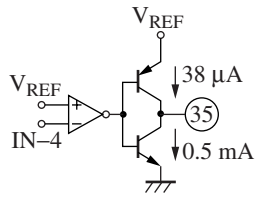
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
15		SS 2 : CH 2 soft start time setting pin. Connect a capacitor between this pin and GND. CH 2 max. duty ratio is set to 88% (in-house), but max. of on period can be adjusted by connecting a resistor between this pin and V_{REF} pin. See Application Notes [3] 8.	I
16		Out 2 : Totem pole type output pin. Normal output current ±100 mA and a peak current ±400 mA can be taken out.	O
17		SS 3 : CH 3 soft start time setting pin. Connect a capacitor between this pin and GND. CH 3 max. duty ratio is set to 88% (in-house), but max. of on period can be adjusted by connecting a resistor between this pin and V_{REF} pin. See Application Notes [3] 8.	I
18		Out 3 : Totem pole type output pin. Normal output current ±100 mA and a peak current ±400 mA can be taken out.	O
19		Out 4 : Totem pole type output pin. Normal output current ±100 mA and a peak current ±400 mA can be taken out.	O
20		SS 4 : CH 4 soft start time setting pin. Connect a capacitor between this pin and GND. CH 4 max. duty ratio is set to 84% (in-house), but max. of on period can be adjusted by connecting a resistor between this pin and V_{REF} pin. See Application Notes [3] 8.	I

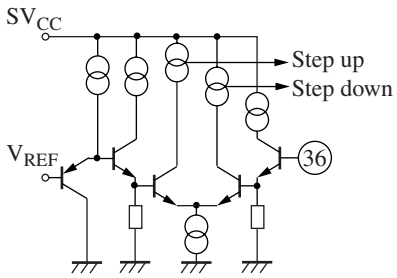
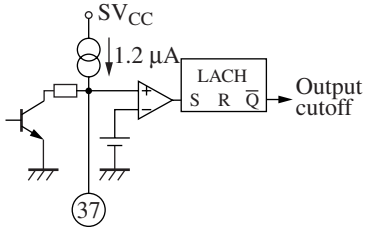
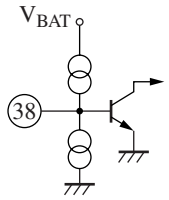
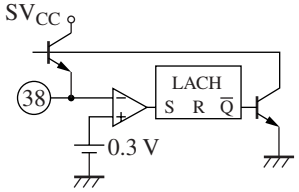
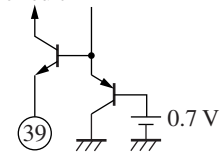
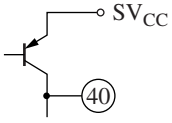
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
21		Out 5 : Totem pole type output pin. Normal output current ±100 mA and a peak current ±400 mA can be taken out.	O
22		SS 5 : CH 5 soft start time setting pin. Connect a capacitor between this pin and GND. CH 5 max. duty ratio is set to 88% (in-house), but max. of on period can be adjusted by connecting a resistor between this pin and V_{REF} pin. See Application Notes [3] 8.	I
23		Out 6 : Totem pole type output pin. Normal output current ±100 mA and a peak current ±400 mA can be taken out.	O
24		SS 6 : CH 6 soft start time setting pin. Connect a capacitor between this pin and GND. CH 6 max. duty ratio is set to 88% (in-house), but max. of on period can be adjusted by connecting a resistor between this pin and V_{REF} pin. See Application Notes [3] 8.	I
25		PGND2 : CH 3 to CH 6 output block GND pin.	—
26		PV_{CC2} : CH 3 to CH 6 power supply pin for output block.	—
27		EO 6 : Output pin for CH 6 error amplifier. Source current: −38 µA, sink current: min. 0.5 mA.	O

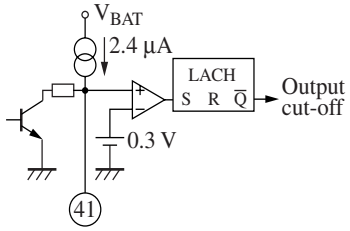
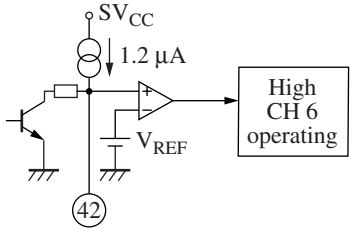
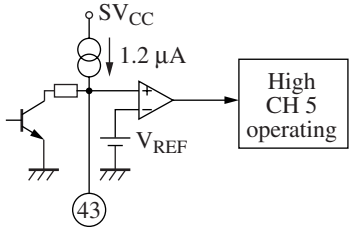
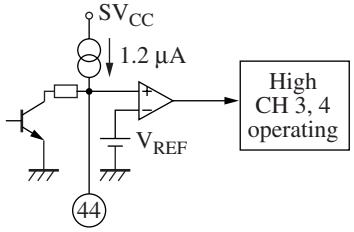
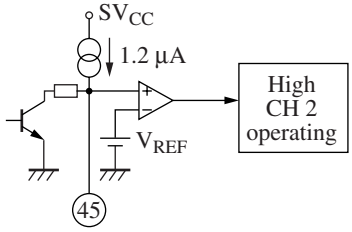
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
28		IN+6 : Inverting input pin for CH 6 error amplifier.	I
29		IN−6 : Non-inverting input pin for CH 6 error amplifier.	I
30		EO 5 : Output pin for CH 5 error amplifier. Source current: −38 µA, sink current: min. 0.5 mA.	O
31		IN−5 : Non-inverting input pin for CH 5 error amplifier.	I
32		SVCC : Power supply pin for signal block.	—
33		IN−4 : Non-inverting input pin for CH 4 error amplifier.	I
34		FB 4 : CH 4 output voltage detection pin. 12.6 kΩ built in between IN-4 and SGND, and 12.4 kΩ between IN-4 and FB 3. DC-DC output of CH 4 is set to 2.5 V.	I
35		EO 4 : Output pin for CH 4 error amplifier. Source current: −38 µA, sink current: min. 0.5 mA.	O

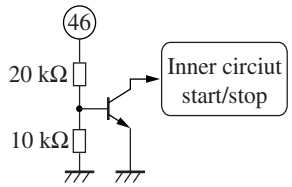
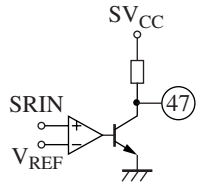
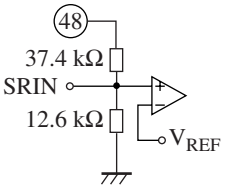
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
36		UDSW : CH 3 step down / step-up output setup pin. N-channel drive and voltage step-up operation with UDSW of SV_{CC} potential, P-channel drive and voltage step-down operation with UDSW of GND potential.	I
37		SCP : A capacitor connecting pin to set a time constant of timer latch short-circuit protection circuit to protect from CH 2 to CH 6 output short circuit. Use within 1 000 pF or more of capacitance. Charged current I_{CHG} is 1.2 µA typ.	O
38	at start-up  at PWM control 	CT : Frequency setting capacitor connecting pin for start-up and for PWM control. 80 kHz fixed inside at startup, and use in the range of 100 kHz to 1 MHz by setting up the resistor at RT pin in PWM control. Here, use the 560 pF fixed capacitor.	O
39	Dischavging current circuit 	RT : Frequency setting resistor connection pin at PWM control. Use within 100 kHz to 1 MHz of oscillation frequency using a 8 kΩ to 100 kΩ resistor in combination with the capacitor at CT pin.	O
40		V_{REF} : Inner reference voltage output pin. Reference voltage is 1.26 V±1% at I_{REF} = − 0.1 mA, and SV_{CC} = 5 V. Connect a capacitor of 0.1 µF or more between V_{REF} and GND for phase compensation.	O

■ Terminal Equivalent Circuits (continued)

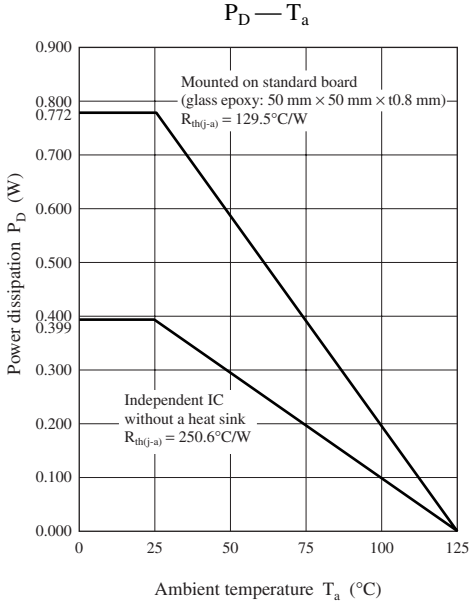
Pin No.	Equivalent circuit	Description	I/O
41		SCP1 : A capacitor connecting pin to set the time constant of a timer latch short circuit protection circuit at CH 1 output short circuit. Use the IC within 1 000 pF or more of capacitance. Charged current I_{CHG1} is 2.4 µA typ.	O
42		CTL 6 : CH 6 on-off control pin. By connecting a capacitor between this pin and GND, you can make delay for a rise time. Input voltage range at on / off control by outer signal is 0 to SV_{CC}.	I
43		CTL 5 : CH 5 on-off control pin. By connecting a capacitor between this pin and GND, you can make delay for a rise time. Input voltage range at on / off control by outer signal is 0 to SV_{CC}.	I
44		CTL 34 : CH 3, CH 4 on-off control pin. By connecting a capacitor between this pin and GND, you can make delay for a rise time. Input voltage range at on / off control by outer signal is 0 to SV_{CC}.	I
45		CTL 2 : CH 2 on-off control pin. By connecting a capacitor between this pin and GND, you can make delay for a rise time. Input voltage range at on / off control by outer signal is 0 to SV_{CC}.	I

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
46		CTL 1 : On / off control pin for all CHs and CH 1. Inner circuit and CH 1 output start at $V_{CTL1} \geq 1$ V typ. Standby current at V_{CTL1} of off is 42 µA typ. at $V_{BAT} = 3$ V. Input voltage range of CTL 1 pin is 0 to V_{BAT}.	I
47		SRDV : External PNP transistor driving pin for a regulator amplifier. The sink current capability is more than 10 mA and a pull-up resistor of 200 kΩ to SV_{CC} is built in.	O
48		SRFB : Output voltage detection input pin in regulator amplifier. There are built in 12.6 kΩ between SRIN and SGND, 37.4 kΩ between SRIN and SRFB and regulator output is set to 5 V.	I

■ Application Notes

[1] P_D — T_a curves of TQFP048-P-0707B



■ Application Notes (continued)

[2] Usage Notes

1. CH 1 operates first and steps up input voltage to 5 V allowing a low input power operation from 1.5 V. This 5 V for CH 1 is used as supply voltage for entire IC. Since the protection circuit is designed for the above operation, you are required to refrain from using for other than the application circuit. For instance, do not use in applying the voltage directly to SV_{CC}.
2. Power dissipation

   Power dissipation P_D is proportionate to supply voltage and varies according to CH 1 output load, FET input capacitance of CH 1 to CH 6 and oscillation frequency, etc. On use, refer to the P_D — T_a curve and be careful not to exceed power dissipation of the package, according to the following equation:

$$P = (SV_{CC} - V_{BEQ1} - \frac{V_{OUT1} \times I_{OUT1} \times R_{OUT}}{h_{feQ1} \times V_{BAT}}) \times \frac{(V_{OUT1} - V_{BAT}) \times I_{OUT}}{h_{feQ1} \times V_{BAT}} + 5 \times SV_{CC} \times Ciss \times f$$

$$+ SV_{CC} \times I_{CC} + V_{BAT} \times I_{BAT} < Pd$$

V_{BEQ1} : Base-emitter voltage of CH 1 NPN transistor
H_{feQ1} : Current amplification ratio of CH 1 NPN transistor
R_{OUT} : Bias current limit resistance to CH 1 NPN transistor
Ciss : Input capacitance of CH 2 to CH 6 output connecting FET
f : Oscillation frequency
I_{CC} : SV_{CC}, PV_{CC1}, PV_{CC2} pin current
I_{BAT} : V_{BAT} pin current

[3] Function descriptions

1. Reference voltage block

   The reference voltage block is constructed with a band gap circuit and it outputs temperature-compensated reference of 1.26 V typ. and of precision ±1%. The reference voltage is stabilized with 4.5 V or more of supply voltage. It is also used as reference for an error amplifier 1 to 6 and the regulator amplifier as well.

2. The triangular wave generator block

   a) At start-up

   Due to the capacitor 560 pF connected to CT pin (pin 38), a triangle wave of approx. 0.76 V high, 0.69 V low and frequency of 80 kHz is generated.

   b) A PWM operation

   When SV_{CC} potential reaches 4.1 V typ. by start of CH 1, the oscillation switches to a saw-tooth wave of approx. 0.76 V high and approx. 0.3 V low from start oscillation due to a timing capacitor and RT pin (pin 39) connection resistor. And it is connected to non-inverting input of PWM comparator IC inside. An oscillation frequency abruptly can be set 100 kHz to max. 1 MHz by the external RT pin-connected resistor.

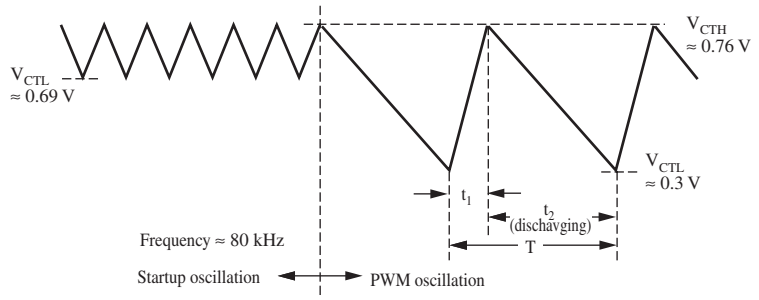


Figure 1-1. Triangular oscillation waveform

■ Application Notes (continued)

[3] Function descriptions (continued)

2. The triangular wave generator block (continued)

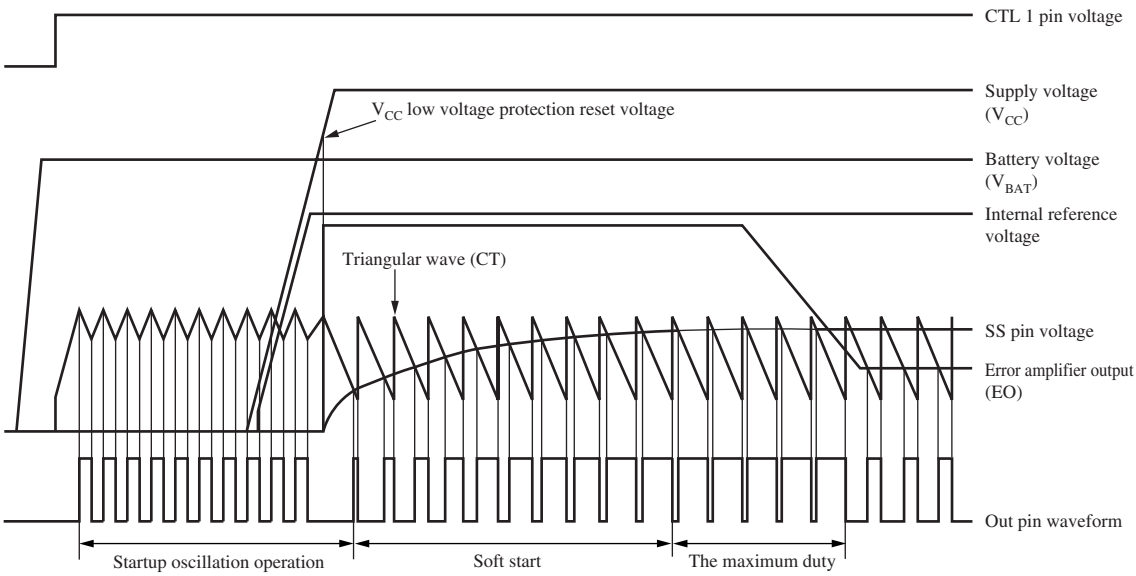


Figure 1-2. The operation from startup to PWM control

Moreover, please calculate the oscillation frequency from below equation.

$$f \approx \frac{4 \times V_{RT}}{RT \times CT \times (V_{CTH} - V_{CTL})} \approx \frac{1.09 \times 10^{10}}{RT} \text{ [Hz]}$$

*$V_{RT} \approx 0.7$ V, CT = 560 pF, $V_{CTH} - V_{CTL} \approx 0.46$ V

As the above formula is intended to calculate the oscillation frequency of 540 kHz in the product specifications, a rapid charging time at frequency change, overshoot and undershoot amount are not considered. The calculated value in the above formula is no more than estimation. In this respect, your final confirmation better be done by using an actual product. See "Application Note [4] Characteristic curves" for the characteristics of oscillation frequency vs. RT pin resistance.

Note) When setting an oscillation frequency, never fail to set a timing capacitor connected to CT pin (pin 38) to 560 pF, and set with RT pin connecting resistor.

3. V_{BAT} operation error prevention circuit at a low input voltage

It protects the system from damage or deterioration due to operation error of control in a transient state of V_{BAT} start or halt. From the rise of V_{BAT} up to 1.43 V typ, set SCP 1 pin (pin 41) to 0 V and cut off the bias to a startup oscillation circuit so as to halt CH 1 output completely.

4. SV_{CC} operation error prevention circuit at a low input voltage

This circuit protects from damage or deterioration of the system due to operation error of control in an IC self bias forming and transient state by starting and halting CH 1. It also sets SCP pin (pin 37) , each SS pin (pin 12 , pin 15, pin 17, pin 20, pin22 and pin 24) and each EO pin (pin 3, pin 6, pin 9, pin 27, pin 30 and pin 35) to 0 V upto 4.1 V typ. at SV_{CC} rise-up in order to shut down an output drive transistor or keep a halt time to 100%.

CT pin (pin 38) is in a pre-oscillation state during the above-mentioned period (a triangular wave) and is switched to a normal oscillation (saw-tooth wave) in sync with the release of error prevention function ($SV_{CC} > 4.1$ V) at SV_{CC} low input voltage. At this time, each SS and EO pin is also released and moves to PWM.

■ Application Notes (continued)

[3] Function descriptions (continued)

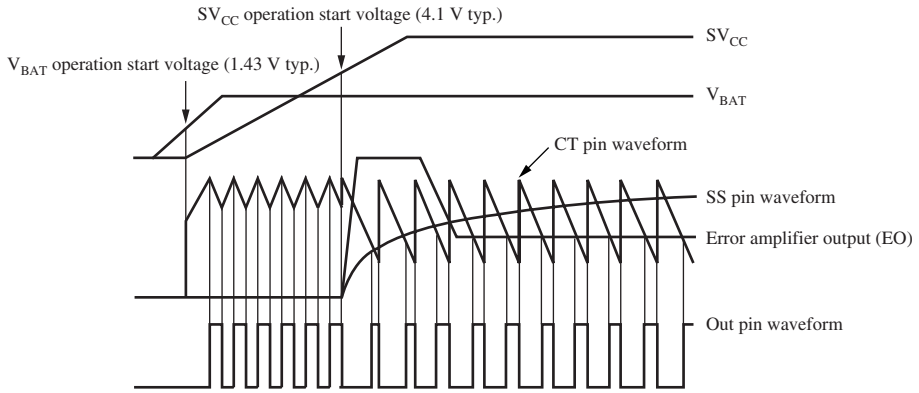


Figure 2. Low input operation error prevention timing chart at V_{BAT}, SV_{CC} startup

5. Error amplifier block

The PNP transistor input error amplifier detects the output voltage of DC-DC converter and inputs the amplified signal to PWM comparator. Non-inverting input (reference side) of each CH except for CH 6 is set to 1.26 V of inner reference voltage. As shown in the following figures, connecting resistors and capacitors between EO pin and In-pin of each CH allows your arbitrary gain setting and phase compensation.

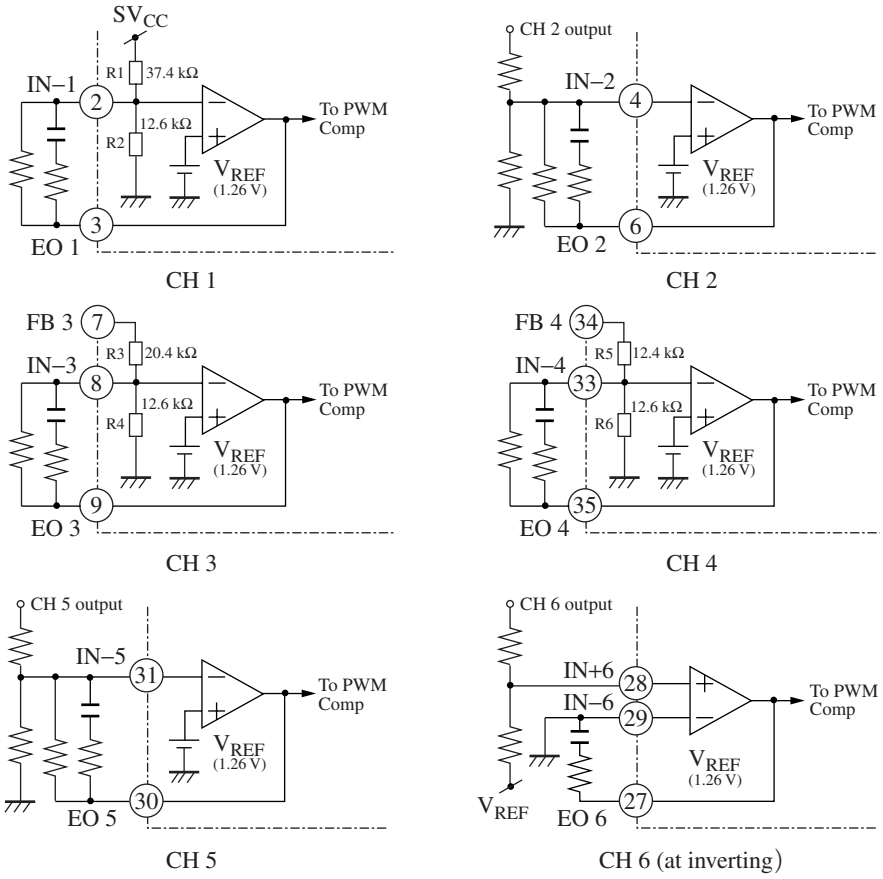


Figure 3. Connection method of error amplifier

■ Application Notes (continued)

[3] Function descriptions (continued)

5. Error amplifier block (continued)

Further, CH 1, CH 3 and CH 4 have a built-in output voltage detection resistor of precision of ±1% so that DC-DC output can be set to 5 V, 3.3 V and 2.5 V respectively. But it is also possible to set an output voltage arbitrarily by an external resistor. When you make the output voltages of CH 1, CH 3 and CH 4 variable, it is recommended to set them by connecting the resistors as shown in the figure 4. Setting of resistance value (equation) and its approximate value can be found in the following equation:

Equation to set output voltages for CH 1, CH 3 and CH 4:

$$\text{Output voltage} = \left(1 + \frac{R_{O1}}{R_{O2}} \cdot \frac{R1}{R2} \cdot \frac{R_{O2} + R2}{R_{O1} + R1}\right) V_{IN}$$

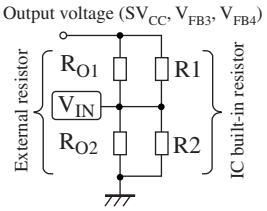


Figure 4. Resistor connecting diagram to set output voltage

The resistor values are selected assuming CH 1 is varied from 4.5 V to 6.0 V

V_{IN} (V)	1.26	1.26	1.26	1.26	1.26	1.26	1.26
R1 (kΩ)	37.4	37.4	37.4	37.4	37.4	37.4	37.4
R2 (kΩ)	12.6	12.6	12.6	12.6	12.6	12.6	12.6
R_{O1} (kΩ)	23.3	26.3	29.7	33.4	37.7	42.4	47.8
R_{O2} (kΩ)	10	10	10	10	10	10	10
SV_{CC} (V)	4.50	4.75	5.00	5.25	5.50	5.75	6.00

The resistor values are selected assuming CH 3 is varied from 3.0 V to 3.6 V

V_{IN} (V)	1.26	1.26	1.26	1.26	1.26	1.26	1.26
R1 (kΩ)	20.4	20.4	20.4	20.4	20.4	20.4	20.4
R2 (kΩ)	12.6	12.6	12.6	12.6	12.6	12.6	12.6
R_{O1} (kΩ)	12.4	13.6	14.8	16.2	17.7	19.3	21
R_{O2} (kΩ)	10	10	10	10	10	10	10
V_{FB3} (V)	3.00	3.10	3.20	3.30	3.40	3.50	3.60

The resistor values are selected assuming CH 4 is varied from 1.6 V to 2.8 V

V_{IN} (V)	1.26	1.25	1.25	1.25	1.25	1.25	1.25
R1 (kΩ)	12.4	12.4	12.4	12.4	12.4	12.4	12.4
R2 (kΩ)	12.6	12.6	12.6	12.6	12.6	12.6	12.6
R_{O1} (kΩ)	1.71	3.06	4.58	6.44	8.75	11.7	15.6
R_{O2} (kΩ)	10	10	10	10	10	10	10
V_{FB4} (V)	1.60	1.80	2.00	2.20	2.40	2.60	2.80

■ Application Notes (continued)

[3] Function descriptions (continued)

6. Timer latch short circuit protection circuit for CH 1

When overload or short circuit state lasts for a certain period of time, this circuit protects a main switch element, a fly-wheel diode, choke coil, etc. from damage or deterioration. This protection circuit considers CH 1 output voltage drop as output short circuit and actuates protective function.

If CH 1 output voltage (SV_{CC}) lowers down to 3.9 V typ. or less, a timer circuit is actuated by output inversion of short circuit detection comparator, and the protection-enable capacitor attached at SCP 1 pin (pin 41) starts recharging.

Unless CH 1 output (SV_{CC}) returns to the normal voltage range (SV_{CC} > 4.3 V) by the time when a capacitor voltage reaches 0.3 V, a latch circuit is set, shuts down the output drive transistor and makes halt time 100%.

As this short circuit protection circuit works in short circuit of CH 1 output i.e. that of SV_{CC}, if it works, CH 2 to CH 6 all also halt. Short circuit protection can be released by either of the following two ways:

1. Once lower V_{BAT} potential down to under-limit threshold voltage or less of V_{BAT} low voltage protection circuit and then reset.
2. Bring CTL 1 to Low and then reset.

Note) It is regarded as output short-circuit at power on and SCP 1 pin voltage starts recharging. Therefore, it is necessary to set the SCP 1 pin capacitance so that output voltage of DC-DC converter may be actuated before IC sets a short circuit detection latch circuit.

DC-DC output start time < Timer latch time

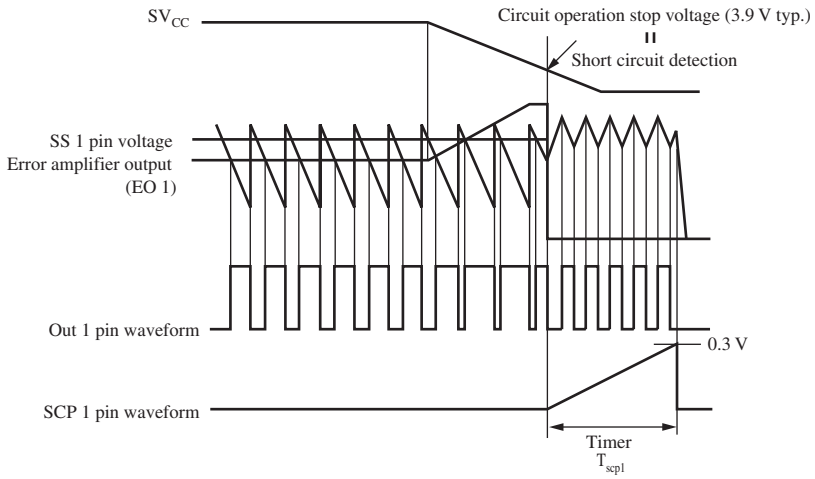


Figure 5. CH 1 output short circuit protect operation

Equation for timer:

$$T_{scp1} = \frac{C_{scp1} \times 0.3}{2.4\ \mu A} = \frac{C_{scp1} \times 10^6}{8}\ [sec]$$

* C_{scp1} : capacitor connected to SCP 1 pin

■ Application Notes (continued)

[3] Function descriptions (continued)

7. Timer latch short circuit protection circuit for CH 2 to CH 6

This circuit protects the external main switch element, fly-wheel diode and choke coil from damage or degradation caused when over load or short circuit of each channel lasts for a certain period. This protection circuit can detect short circuit by the output signal from each error amplifier.

When an output voltage of DC-DC converter is lowered and any pin (EO 2 to EO 6 pin) of pin 6, pin 9, pin 27, pin 30 and pin 35 becomes 1.26 V or more, a time circuit starts to work due to an output voltage inversion of a short circuit detection comparator, and a protection-enable capacitor attached to SCP pin (pin 37) starts re-charging. If an output of error amplifier does not return to a normal voltage until this capacitor voltage reaches 0.9 V , a halt period is set to 100% by setting a latch circuit and shutting down an output drive transistor. This short circuit protection circuit will stop all CH operations including CH 1 when one of CH 2 to CH 6 short-circuits.

Meanwhile, a short-circuit protection can be released in either of the following two methods:

1. Once lower V_{BAT} potential down to under-limit threshold voltage or less of V_{BAT} low voltage protection circuit and then reset.
2. Bring CTL 1 to Low and then reset.

Note) It is regarded as output short-circuit at power on and SCP 1 pin voltage starts recharging. Therefore, it is necessary to set the SCP 1 pin capacitance so that output voltage of DC-DC converter may be actuated before IC sets a short circuit detection latch circuit. Note that a startup time will be delayed especially for a soft start.

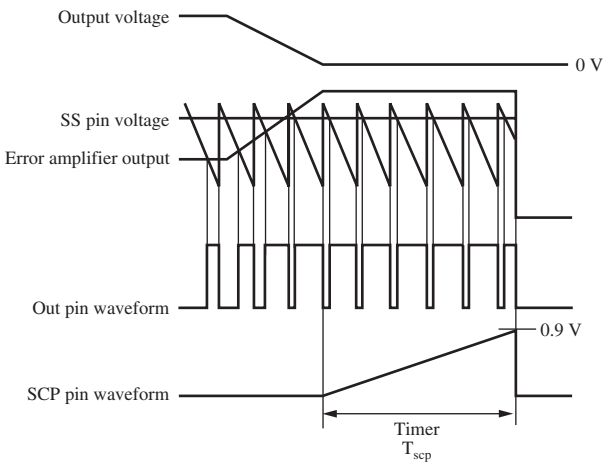


Figure 6. CH 2 to CH 6 output short circuit protect operation

Equation for timer:

$$T_{scp} = \frac{C_{scp} \times 0.9}{1.2\ \mu A} = 0.75.C_{scp} \times 10^6 \quad [sec]$$

* C_{scp} : capacitor connected to SCP pin

■ Application Notes (continued)

[3] Function descriptions (continued)

8. PWM comparator block

A PWM comparator controls the on period of output pulse according to an input voltage. The saw-tooth wave of a CT pin turns on the output transistor during its lower period than SS / EO pin. A maximum duty ratio is set to 84% for CH 4 and 88% typ. for others, but if you connect a resistor between each SS pin and SGND or V_{REF}, you can set to 0% to 100%.

Further, if you connect a capacitor between each SS pin and GND, a soft start which spreads gradually the on period of output pulse at start up operation.

Equation for Max-Du setting:

$$MaxD_U = \frac{V_{SS} - V_{CTL}}{V_{CTH} - V_{CTL}} \times 100 \quad [\%] \qquad * V_{SS} = \frac{56.2 \times R_{O2} \times (R_{O1} + 43.8)}{100 \times R_{O1} \times R_{O2} + 56.2 \times 43.8 \times (R_{O1} + R_{O2})} \quad [V]$$

$*V_{CTH} = 0.76$ V, $V_{CTL} = 0.3$ V

Equation for soft start setting:

$$T_{SS} = C_{SS} \times 56.2k \times 1n \left(\frac{1}{1 - \frac{V_{DTC}}{V_{SS}}} \right)$$

$*V_{SS} \approx 0.7$ V, V_{DTC} : SS pin voltage after T_{SS} time

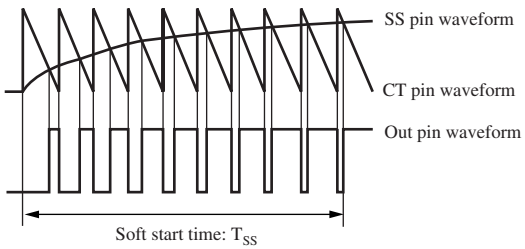


Figure 7. Soft start operation

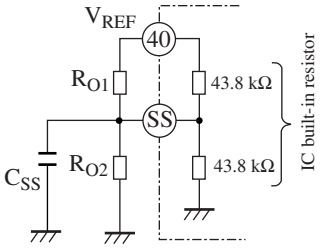


Figure 8. Output D_U and soft start setting

9. CH 1 output block

a) At startup

At start up time, a driving current is supplied by PNP transistor at output on, and output Tr. is turned off by the built-in resistor 15 kΩ at output off, as shown right figures. An output source current at the turn on is approx. 5 mA typ. and the sink current is determined by a base-emitter voltage (V_{BE}) of SWTr. and the built-in resistor 15 kΩ.

As mentioned above, both output sink and source currents are small. In this respect, you are required to use a bipolar transistor for an external SW element so that CH 1 output load current may be lower than the current found by the following equation.

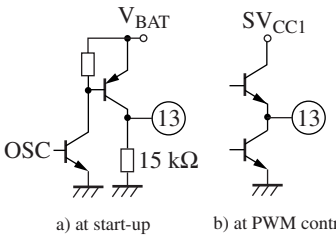


Figure 9. CH 1 output drive form

$I_O = h_{fe} \times I_{ST}$

I_O : CH 1 output load current at startup
h_{fe} : Current amplification ratio of an external SW element
I_{ST} : Output sink or source current at startup whichever langer.

■ Application Notes (continued)

[3] Function descriptions (continued)

9. CH 1 output block (continued)

b) At PWM control

At the time of PWM control, CH 1 output is switched to a totem pole type as shown in the figure 3. Output sink or source current is approximately 20 mA typ.

10. CH 2 to CH 6 output block

All the output circuits are of a totem pole type. A sink or source current is maximum ±100 mA and a peak current is maximum ±0.4 A, enabling you to operate directly MOSFET as an external SW element.

Further, for CH 3, you can select either N-channel or P-channel for an external SW element by setting UDSW (pin 36).

* CH 2, CH 5 and CH 6 are set to N-channel driving and CH 4 to P-channel driving.

Note) Output high voltage for CH 3 and CH 4 is V_{CC} - 1 V (max.).

Be careful of selecting a threshold voltage value of P-channel MOS when using CH 3 and CH 4 SW elements of the P-channel.

11. CTL block

This functions as on / off for each CH and enables you to run a sequence control as shown in the figure 10.

Note) 1. Since CH 1 output is used as a bias (SV_{CC}) of IC, you cannot operate on / off of other CHs as long as CH 1 (CTL 1) is not driven.

2. CH 3 and CH 4 are commonly controlled by CTL 34 (pin 44).
When you do not use either CH 3 or CH 4, use the IC in the state that there are no oscillations at output by short-circuiting SS or EO pin of the unused CH to GND.

3. Abrupt rise of CTL-1 pin voltage likely causes operation error. After connecting a resistor and a capacitor to CTL-1 pin, use the rise of CTL-1 pin according to the slope shown below:

CTL-1 rise-up slope is dv/dt < 5.5 mV/μs

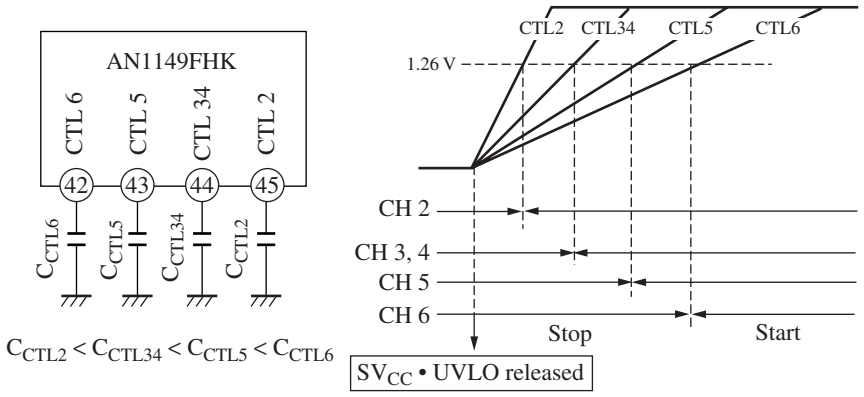


Figure 10. CTL sequence control

■ Application Notes (continued)

[3] Function descriptions (continued)

12. Regulator amplifier block

A regulator amplifier which forms a three-pin regulator by connecting an external PNP transistor to SRFB (pin 47) and SRDV (pin 48) is bult in.

CH 1 output is exclusively used for a step-up circuit and you can keep the output constant by using a regulator amplifier under the conditions on which input battery voltage (V_{BAT}) varies widely.

The sink current of a regulator amplifier is 10 mA typ. and a detection resistor of ±1% precision to set output voltage to 5 V is built in. Set an output voltage in the same way as for error amplifier if variable output is needed. (See the "Application Note - [3] 5.)

Note) When using a regulator amplifier, insert a resistor R1 between base and SRDV (pin 48) of an external PNP transistor to protect from a rush-in current, as shown in the figure below:

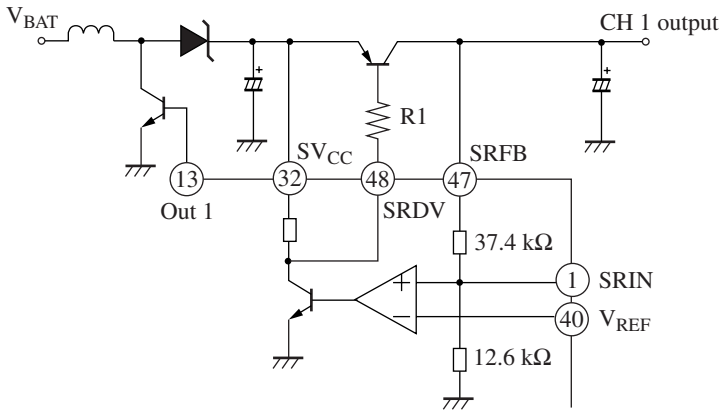
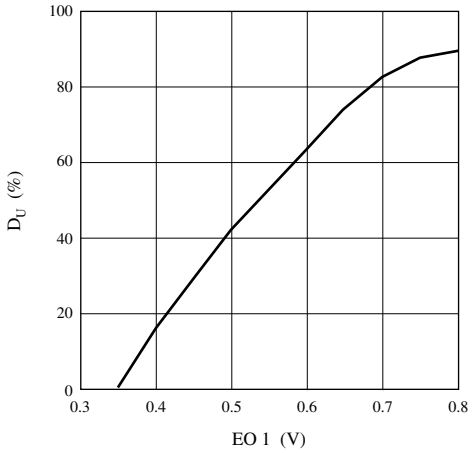


Figure 11. Connection of regulator amplifier

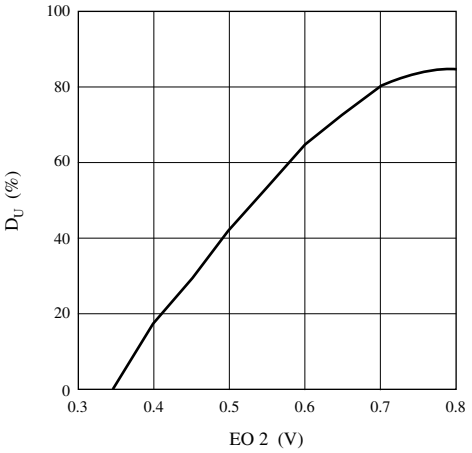
■ Application Notes (continued)

[4] Characteristic curves

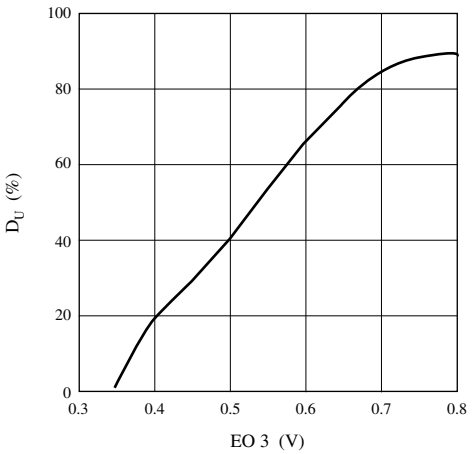
D_U linearity characteristics (CH 1)



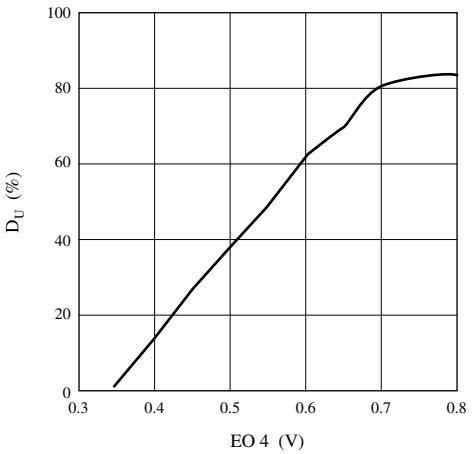
D_U linearity characteristics (CH 2)



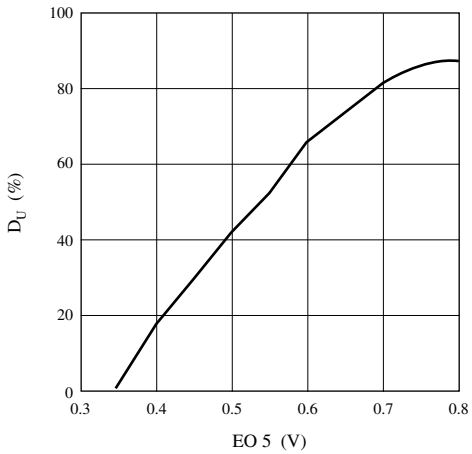
D_U linearity characteristics (CH 3)



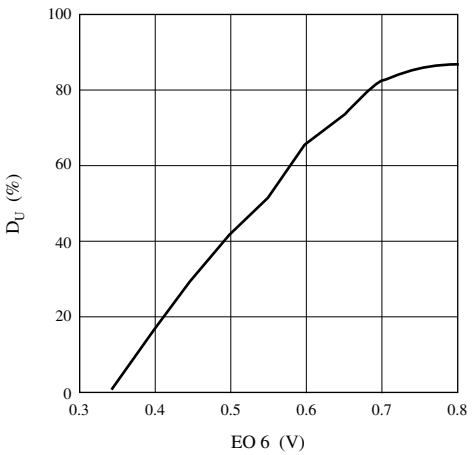
D_U linearity characteristics (CH 4)



D_U linearity characteristics (CH 5)



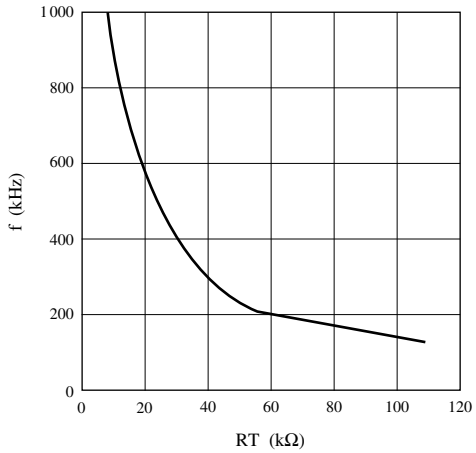
D_U linearity characteristics (CH 6)



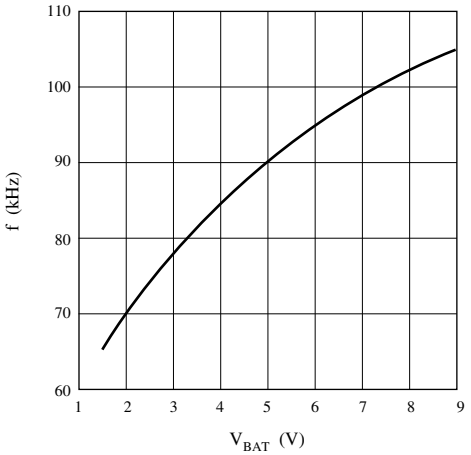
■ Application Notes (continued)

[4] Characteristic curves (continued)

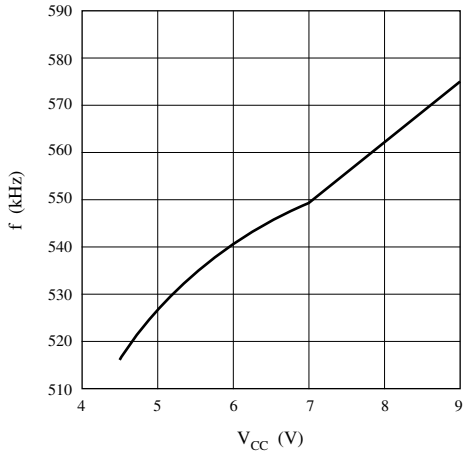
RT-CT (oscillation frequency) characteristics: CT = 560 (pF)



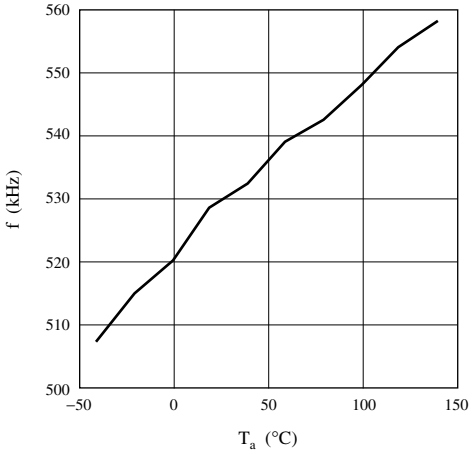
Startup oscillation frequency V_{BAT} fluctuation at start-up



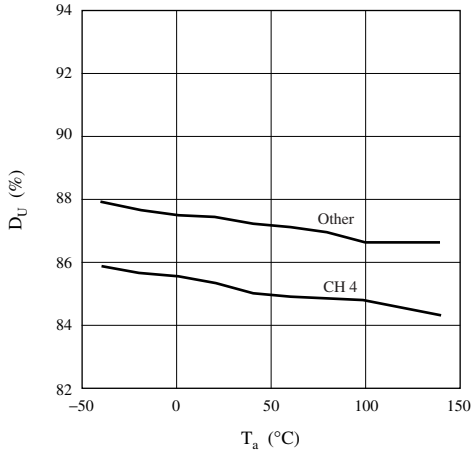
Normal oscillation frequency V_{CC} fluctuation



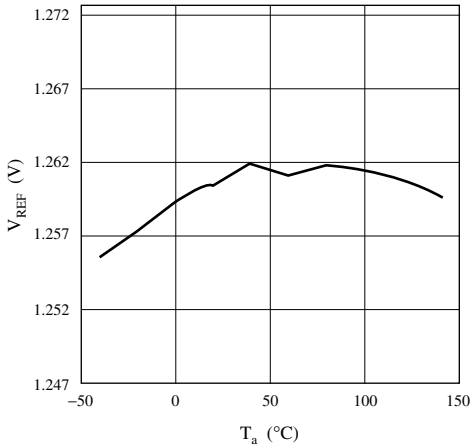
Oscillator frequency temperature characteristics



Duty ratio temperature characteristics

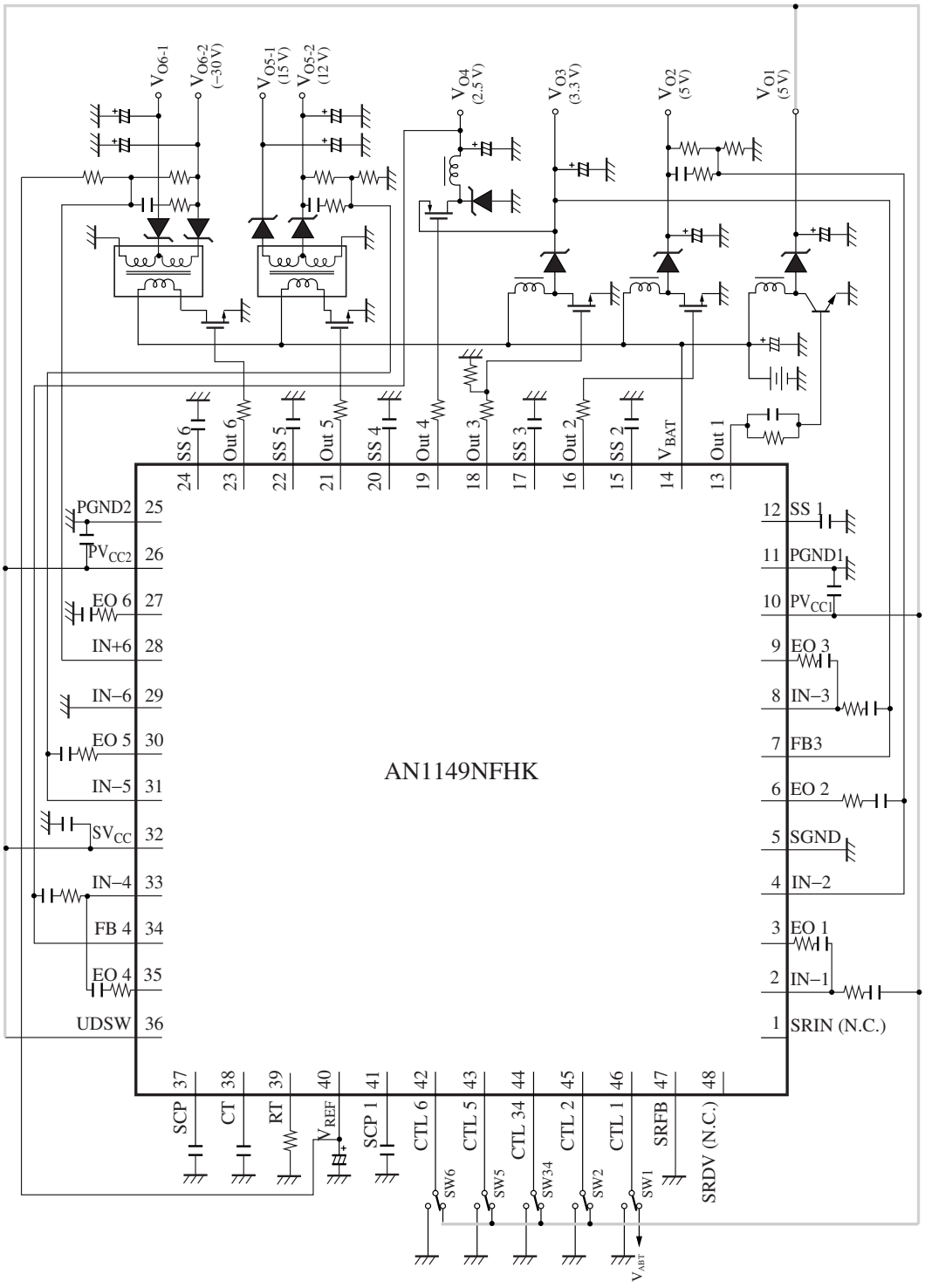


V_{REF} temperature characteristics



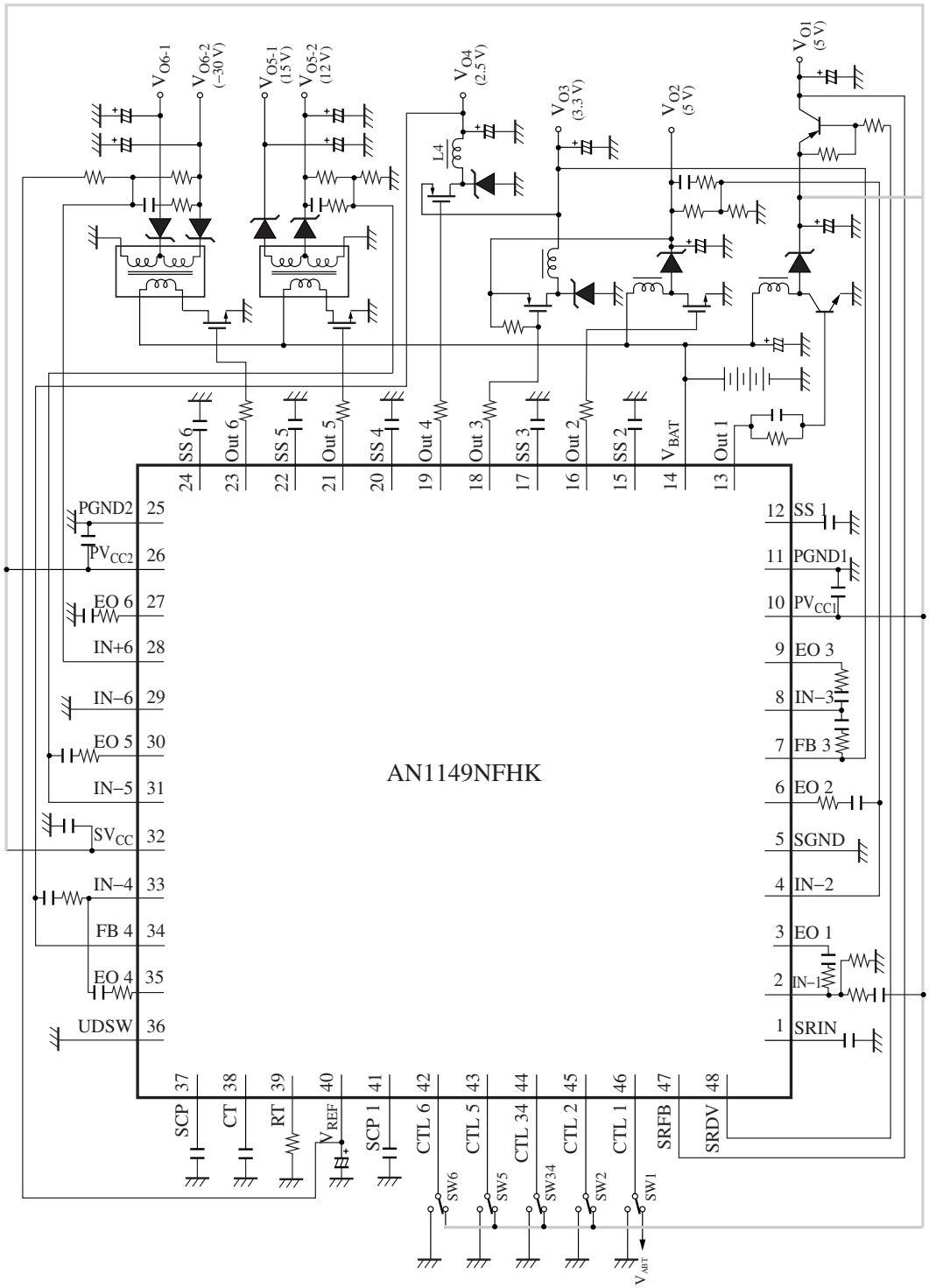
■ Application Circuit Examples

• Application circuit examples. V_{BAT} : JIS SUM-3 dry battery (2 units), 1.5 V to 3.6 V



■ Application Circuit Examples (continued)

• Application circuit examples. V_{BAT} : JIS SUM-3 dry battery (4 units), 3 V to 7.2 V



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