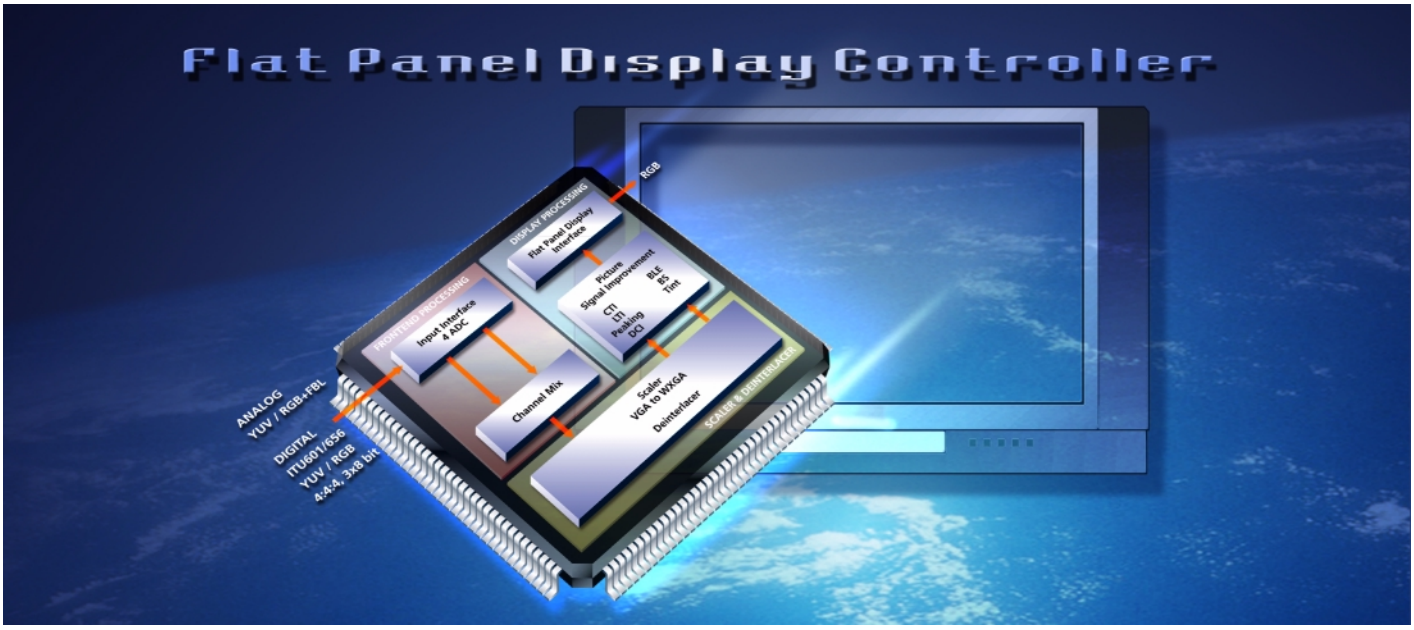
DPS 9450A

Feb/2002



DPS 9450A
Display Processor and Scaler

The DPS is a single-chip digital display processor and scaler specially designed for TV sets with matrix displays. The DPS 9450A is a new family member of the Micronas MEGAVISION® IC set implemented in deep submicron CMOS technology.

Video Inputs

- Digital input for 50/60 I or 50/60 P signals in ITU-656 (8 bit) or ITU-601 (16 bit)
- 3×8 bit YC_rC_b/RGB input
- 2 analog RGB/YC_rC_b inputs for Teletext, graphic, 480p (EIA-770.2, 1080i/720p reduced resolution):
  4 built-in ADCs (8-bit) for RGB + fast-blank with 40.5 MHz sampling rate
- Separate HS and VS (2×) inputs

Sync Processing

- HS and VS outputs to synchronize
  - the ext. analog RGB/YC_rC_b source in the soft mix mode (see display modes)
  - ext. OSD source

Display Modes

- Digital mode: video from the digital input
- Analog mode: video/graphic/teletext from the analog RGB/YC_rC_b input
- Softmix mode: soft mixing of the video and component input
- Additional OSD can be mixed

Video Processing

- Full 4:4:4 processing
- RGB-to-YC_rC_b conversion
- Brightness, Contrast, Saturation for analog component input
- Dynamic contrast improvement (DCI)
- Black level expander (BLE)
- Luma & chroma transition improvement
- Dynamic peaking
- Brightness, Contrast, Saturation, Tint
- Programmable YC_rC_b-to-RGB matrix
- Programmable characteristic on R,G,B, for γ-correction, Blue-stretch, White-drive
- Dithering for 8- to 6-bit digital outputs

Display Format Processing

- Prescaling of the input signal:
  horizontal scaling factor: 1.0 ... 1/64
- Upscaling of the output signal:
  horizontal scaling factor: 1 ... 4
  (5-zone panorama generator)
- Vertical scaling factor: 0.5 ... 4
- Deinterlacing with line-doubling/upscaling

OSD

- digital RGB input (6 or 12 bit / pixel)
- 64 entry CLUT with 12-bit colors
- Picture frame and testpattern generation
- Half-contrast switch (0, 25%, 50%, 100%)

Display Resolutions

- 640×480 (VGA; 4:3 panel)
- 852×480 (W-VGA; 16:9 panel)
- 800×600 (SVGA)
- 1024×768 (XGA)
- 1365×768 (W-XGA)

DPS 9450A

Feb/2002

Output Interface

- 2×18- or 24-bit RGB output: dual-pixel mode
- programmable panel control signals

Miscellaneous

- up to 2 PWM outputs
- up to 8 general purpose I/Os
- I^2C interface (400 kHz)
- JTAG boundary scan interface
- 1.8 V and 3.3 V supply
- PMQFP144 package

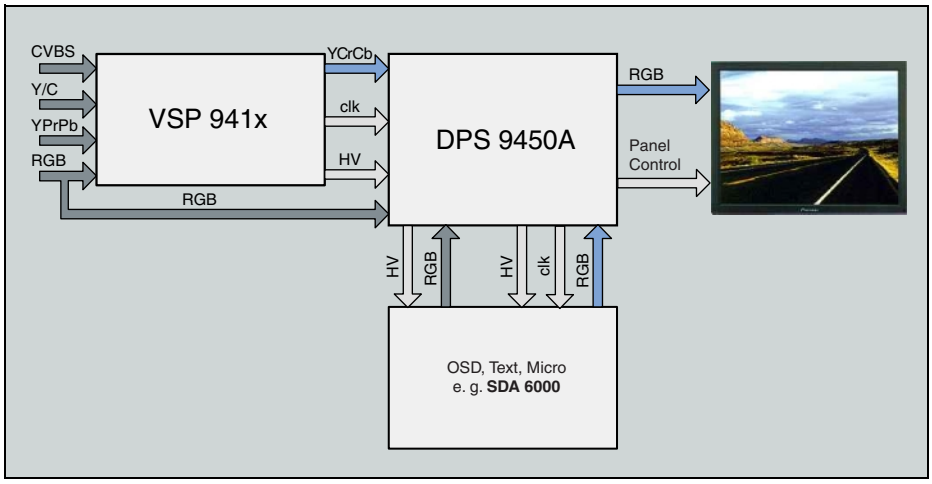


Fig. 1: Application example: TV/VGA source XGA panel

System Architecture

The figure shows the block diagram of the DPS 9450A. The device has digital outputs. In principle the device comprises three major functional and clock domains parts.

The functional parts are

- video input processing,
- scaling, and
- display processing.

The clock domains are

- ITU domain,
- input domain, and
- display domain (compare the block diagram and the different shaded areas).

The input and the output signals of the IC can be chosen in various configurations.

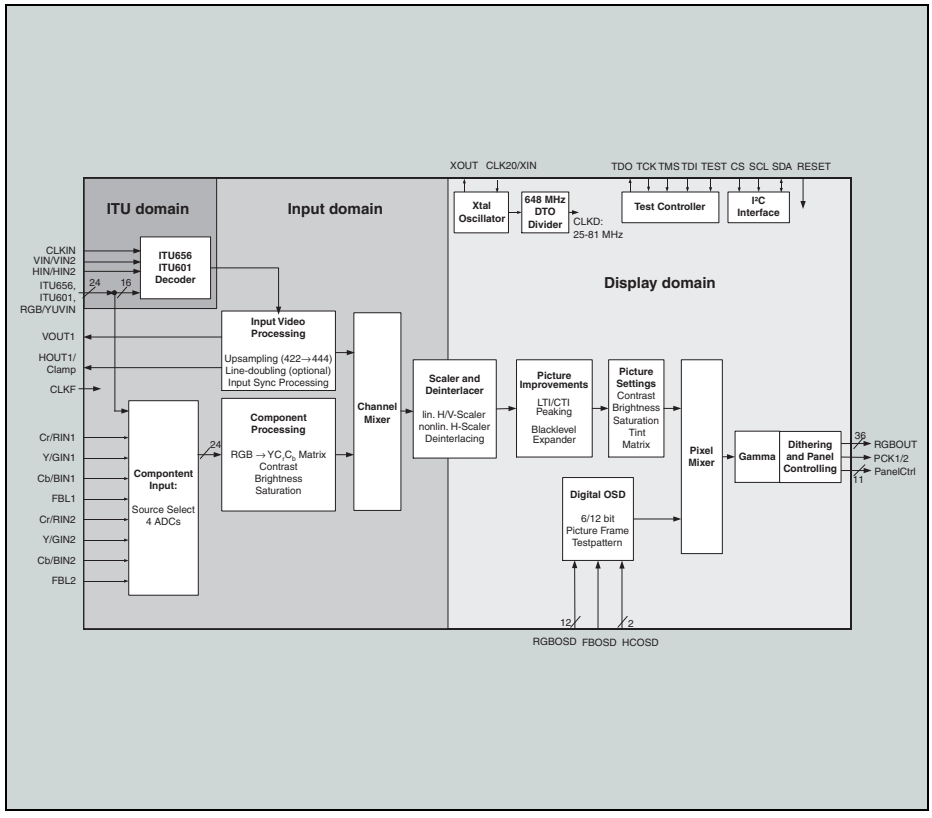


Fig. 2: Block diagram of the DPS 9450A

Edition Feb. 25, 2002; Order No. 6251-591-1PI

Micronas GmbH · Hans-Bunte-Strasse 19 · D-79108 Freiburg (Germany) · P.O. Box 840 · D-79008 Freiburg (Germany)
Tel. +49-761-517-0 · Fax +49-761-517-2174 · E-mail: docservice@micronas.com · www.micronas.com