SYNCHRONOUS ZBL SRAM PIPELINED OUTPUT

128K x 36 SRAM

+3.3V SUPPLY, FULLY REGISTERED
2-BIT BURST COUNTER

FEATURES

- Zero Bus Latency, no dead cycles between write and read cycles
- Fast clock speed: 143, 133, 117, and 100MHz
- Fast access time: 4.0, 4.2, 4.5, 5.0ns
- Internally synchronized registered outputs eliminate the need to control OE#
- Single 3.3V -5% and +5% power supply
- Single R/W# (READ/WRITE) control pin
- Positive clock-edge triggered, address, data, and control signal registers for fully pipelined applications
- Interleaved or linear 4-word burst capability
- Individual byte write (BWa# - BWd#) control (may be tied LOW)
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- SNOOZE MODE for low power standby
- Automatic power down
- Packaged in a JEDEC standard 100-pin TQFP package

OPTIONS MARKING

- Timing
  - 4.0ns access/7.0ns cycle -4
  - 4.2ns access/7.5ns cycle -5
  - 4.5ns access/8.5ns cycle -6
  - 5.0ns access/10.0 cycle -7
- Packages
  - 100-pin TQFP T

GENERAL DESCRIPTION

The GVT71128ZC36 SRAM is designed to eliminate dead cycles when transitions from READ to WRITE or vice versa. This SRAM is optimized for 100 percent bus utilization and achieves Zero Bus Latency (ZBL). It integrates 131,072x36 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. The Galvantech Synchronous Burst SRAM family employs high-speed, low power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, depth-expansion chip enables (CE#, CE2# and CE2), cycle start input (ADV/LD#), clock enable (CKE#), byte write enables (BWa#, BWb#, BWc# and BWd#), and read-write control (R/W#).

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later, its associated data occurs, either read or write.

A clock enable (CKE#) pin allows operation of the GVT71128ZC36 to be suspended as long as necessary. All synchronous inputs are ignored when (CKE#) is high and the internal device registers will hold their previous values.

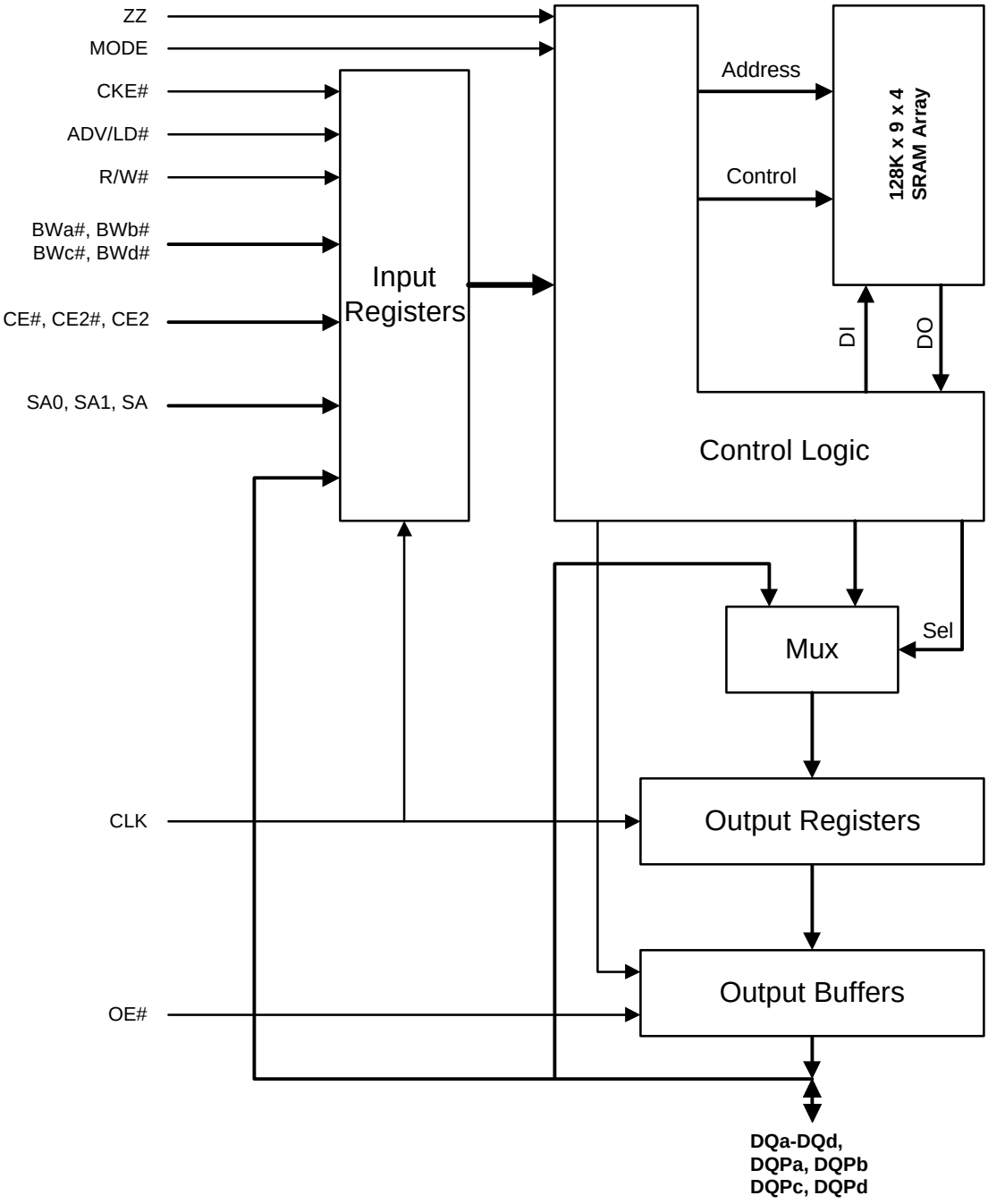
There are three chip enable pins (CE#, CE2, CE2#) that allow the user to deselect the device when desired. If any one of these three are not active when ADV/LD# is low, no new memory operation can be initiated and any burst cycle in progress is stopped. However, any pending data transfers (read or write) will be completed. The data bus will be in high impedance state two cycles after chip is deselected or a write cycle is initiated.

The GVT71128ZC36 has an on-chip 2-bit burst counter. In the burst mode, the GVT71128ZC36 provides four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the MODE input pin. The MODE pin selects between linear and interleaved burst sequence. The ADV/LD# signal is used to load a new external address (ADV/LD#=LOW) or increment the internal burst counter (ADV/LD#=HIGH)

Output enable (OE#), snooze enable (ZZ) and burst sequence select (MODE) are the asynchronous signals. OE# can be used to disable the outputs at any given time. ZZ may be tied to LOW if it is not used.

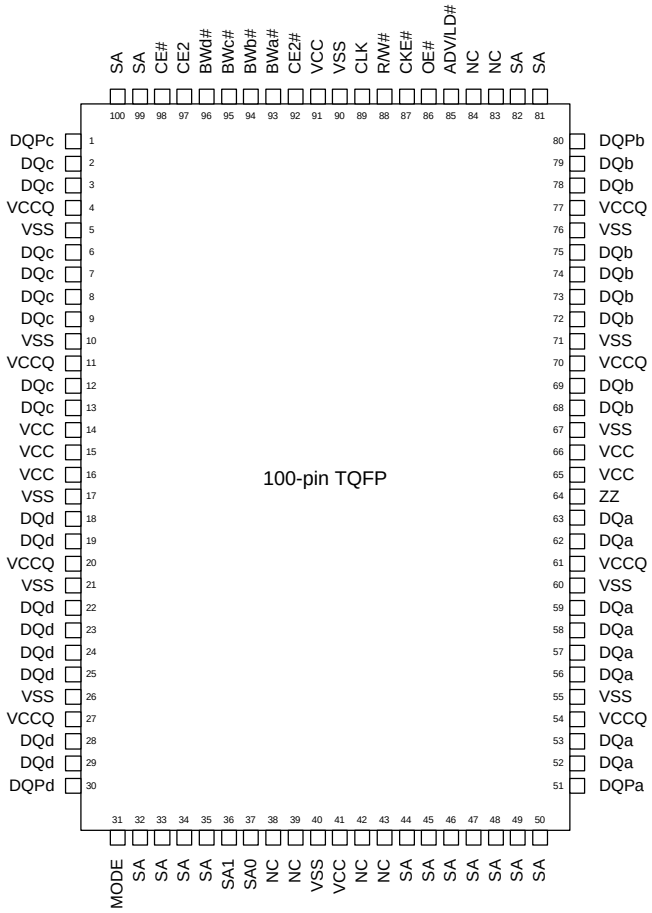
The GVT71128ZC36 utilizes high performance high volume 3.3V CMOS process, and is packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) for high board density.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN ASSIGNMENT (Top View)



PIN DESCRIPTIONS

TQFP PINS	SYMBOL	TYPE	DESCRIPTION
37, 36, 32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 99, 100	SA0, SA1, SA	Input-Synchronous	Synchronous Address Inputs: The address register is triggered by a combination of the rising edge of CLK, ADV/LD# LOW, CKE# LOW and true chip enables. SA0 and SA1 are the two least significant bits of the address field and set the internal burst counter if burst cycle is initiated.
93, 94, 95, 96	BWa#, BWb#, BWc#, BWd#	Input-Synchronous	Synchronous Byte Write Enables: Each 9-bit byte has its own active low byte write enable. On load write cycles (when R/W# and ADV/LD# are sampled LOW), the appropriate byte write signal (BWx#) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte write signals are ignored when R/W# is sampled high. The appropriate byte(s) of data are written into the device two cycles later. BWa# controls DQa and DQPa pins; BWb# controls DQb and DQPb pins; BWc# controls DQc and DQPc pins; BWd# controls DQd and DQPd pins. BWx# can all be tied LOW if always doing write to the entire 36-bit word.
87	CKE#	Input-Synchronous	Synchronous Clock Enable Input: When CKE# is sampled HIGH, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of CKE# sampled HIGH on the device outputs is as if the low to high clock transition did not occur. For normal operation, CKE# must be sampled LOW at rising edge of clock.
88	R/W#	Input-Synchronous	Read Write: R/W# signal is a synchronous input that identifies whether the current loaded cycle and the subsequent burst cycles initiated by ADV/LD# is a Read or Write operation. The data bus activity for the current cycle takes place two clock cycles later.

PIN DESCRIPTIONS (continued)

TQFP PINS	SYMBOL	TYPE	DESCRIPTION
89	CLK	Input-Synchronous	Clock: This is the clock input to GVT71128ZC36. Except for OE#, ZZ and MODE, all timing references for the device are made with respect to the rising edge of CLK.
98, 92	CE#, CE2#	Input-Synchronous	Synchronous Active Low Chip Enable: CE# and CE2# are used with CE2 to enable the GVT71128ZC36. CE# or CE2# sampled HIGH or CE2 sampled LOW, along with ADV/LD# LOW at the rising edge of clock, initiates a deselect cycle. The data bus will be HIGH-Z two clock cycles after chip deselect is initiated.
97	CE2	input-Synchronous	Synchronous Active High Chip enable: CE2 is used with CE# and CE2# to enable the chip. CE2 has inverted polarity but otherwise is identical to CE# and CE2#.
86	OE#	Input	Asynchronous Output Enable: OE# must be LOW to read data. When OE# is HIGH, the I/O pins are in high impedance state. OE# does not need to be actively controlled for read and write cycles. In normal operation, OE# can be tied LOW.
85	ADV/LD#	Input-Synchronous	Advance/Load: ADV/LD# is a synchronous input that is used to load the internal registers with new address and control signals when it is sampled LOW at the rising edge of clock with the chip is selected. When ADV/LD# is sampled HIGH, then the internal burst counter is advanced for any burst that was in progress. The external addresses and R/W# are ignored when ADV/LD# is sampled HIGH.
31	MODE	Input-Static	Burst Mode: When MODE is HIGH or NC, the interleaved burst sequence is selected. When MODE is LOW, the linear burst sequence is selected. MODE is a static DC input.
64	ZZ	Input-Asynchronous	Snooze Enable: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC.
52, 53, 56-59, 62, 63 68, 69, 72-75, 78, 79 2, 3, 6-9, 12, 13 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/Output	Data Inputs/Outputs: Both the data input path and data output path are registered and triggered by the rising edge of CLK. Byte “a” is DQa pins; Byte “b” is DQb pins; Byte “c” is DQc pins; Byte “d” is DQd pins.
51, 80, 1, 30	DQPa, DQPb, DQPc, DQPd	Input/Output	Parity Inputs/Outputs: Both the data input path and data output path are registered and triggered by the rising edge of CLK. DQPa is parity bit for Byte “a”; DQPb is parity bit for Byte “b”; DQPc is parity bit for Byte “c”; DQPd is parity bit for Byte “d”.
14, 15, 16, 41, 65, 66, 91	VCC	Supply	Power Supply: +3.3V -5% and +5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	VSS	Ground	Ground: GND.
4, 11, 20, 27, 54, 61, 70, 77	VCCQ	I/O Supply	Output Buffer Supply: +3.3V -5% and +5%.
38, 39, 42, 43, 83, 84	NC	-	No Connect: These signals are not internally connected.

INTERLEAVED BURST ADDRESS TABLE (MODE = VCC or NC)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)[1]
A...A_{00}	A...A_{01}	A...A_{10}	A...A_{11}
A...A_{01}	A...A_{00}	A...A_{11}	A...A_{10}
A...A_{10}	A...A_{11}	A...A_{00}	A...A_{01}
A...A_{11}	A...A_{10}	A...A_{01}	A...A_{00}

LINEAR BURST ADDRESS TABLE (MODE = VSS)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)[1]
A...A_{00}	A...A_{01}	A...A_{10}	A...A_{11}
A...A_{01}	A...A_{10}	A...A_{11}	A...A_{00}
A...A_{10}	A...A_{11}	A...A_{00}	A...A_{01}
A...A_{11}	A...A_{00}	A...A_{01}	A...A_{10}

Note:

1. Upon completion of the Burst sequence, the counter wraps around to its initial state and continues counting.

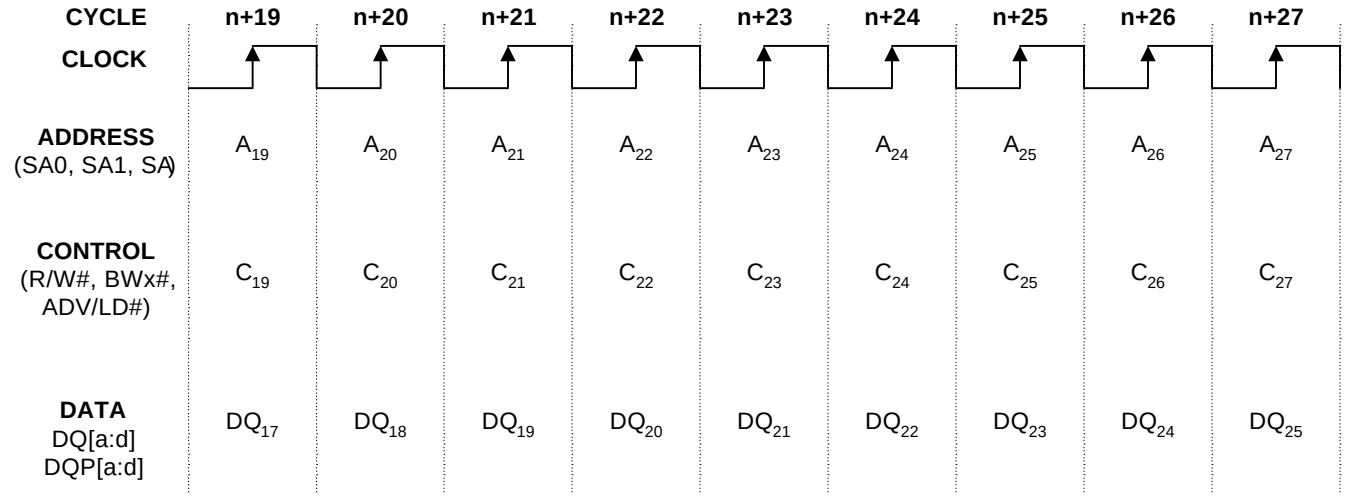
PARTIAL TRUTH TABLE FOR READ/WRITE[1]

FUNCTION	R/W#	BWa#	BWb#	BWc#	BWd#
Read	H	X	X	X	X
No Write	L	H	H	H	H
Write Byte a (DQa, DQPa)[2]	L	L	H	H	H
Write Byte b (DQb, DQPb)[2]	L	H	L	H	H
Write Byte c (DQc, DQPc)[2]	L	H	H	L	H
Write Byte d (DQd, DQPd}[2]	L	H	H	H	L
Write all bytes	L	L	L	L	L

Note:1

1. L means logic LOW. H means logic HIGH. X means "Don't Care."
2. Multiple bytes may be selected during the same cycle.

FUNCTIONAL TIMING DIAGRAM



Note:

1. This assumes that CKE#, CE#, CE2 and CE2# are all True.
2. All addresses, control and data-in are only required to meet set-up and hold time with respect to the rising edge of clock. Data out is valid after a clock-to-data delay from the rising edge of clock.

TRUTH TABLE(1-9)

OPERATION	PREVIOUS CYCLE	ADDRESS USED	R/W#	ADV/LD#	CE#	CKE#	BWx#	OE#	DQ (2 cycles later)	NOTES
DESELECT CYCLE	X	X	X	L	H	L	X	X	High-Z	
CONTINUE DESELECT/NOP	DESELECT	X	X	H	X	L	X	X	High-Z	10
READ CYCLE (BEGIN BURST)	X	External	H	L	L	L	X	X	Q	
READ CYCLE (CONTINUE BURST)	READ	Next	X	H	X	L	X	X	Q	10
DUMMY READ (BEGIN BURST)	X	External	H	L	L	L	X	H	High-Z	11
DUMMY READ (CONTINUE BURST)	READ	Next	X	H	X	L	X	H	High-Z	10, 11
WRITE CYCLE (BEGIN BURST)	X	External	L	L	L	L	L	X	D	
WRITE CYCLE (CONTINUE BURST)	WRITE	Next	X	H	X	L	L	X	D	10
ABORT WRITE (BEGIN BURST)	X	External	L	L	L	L	H	X	High-Z	11
ABORT WRITE (CONTINUE BURST)	WRITE	Next	X	H	X	L	H	X	High-Z	10, 11
IGNORE CLOCK EDGE /NOP	X	X	X	H	X	H	X	X	-	12

Note:

1. L means logic LOW. H means logic HIGH. X means "Don't Care." High-Z means HIGH IMPEDANCE. BWx# = L means [BWa#*BWb#*BWc#*BWd#] equals LOW. BWx# = H means [BWa#*BWb#*BWc#*BWd#] equals HIGH.
2. CE# equals H means CE# and CE2# are LOW along with CE2 being HIGH. CE# equals L means CE# or CE2# is HIGH or CE2 is LOW. CE# equals X means CE#, CE2# and CE2 are "Don't Care."
3. BWa# enables WRITE to byte "a" (DQa and DQPa pins). BWb# enables WRITE to byte "b" (DQb and DQPb pins). BWc# enables WRITE to byte "c" (DQc and DQPc pins). BWd# enables WRITE to byte "d" (DQd and DQPd pins).
4. The device is not in SNOOZE MODE, i.e. the ZZ pin is LOW.
5. During SNOOZE MODE, the ZZ pin is HIGH and all the address pins and control pins are "Don't Care." The SNOOZE MODE can only be entered 2 cycles after the WRITE cycle, otherwise the WRITE cycle may not be completed.
6. All inputs, except OE#, ZZ and MODE pins, must meet setup time and hold time specification against the clock (CLK) LOW-to-HIGH transition edge.
7. OE# may be tied to LOW for all the operation. This device automatically turns off the output driver during WRITE cycle.
8. Device outputs are ensured to be in High-Z during device power-up.
9. This device contains a 2-bit burst counter. The address counter is incremented for all CONTINUE BURST cycles. Address wraps to the initial address every fourth burst cycle.
10. CONTINUE BURST cycles, whether READ or WRITE, use the same control signals. The type of cycle performed, READ or WRITE, depends upon the R/W# control signal at the BEGIN BURST cycle. A CONTINUE DESELECT cycle can only be entered if a DESELECT cycle is executed first.
11. DUMMY READ and ABORT WRITE cycles can be entered to setup subsequent READ or WRITE cycles or to increment the burst counter.
12. When an IGNORE CLOCK EDGE cycle enters, the output data (Q) will remain the same if the previous cycle is READ cycle or remain High-Z if the previous cycle is WRITE or DESELECT cycle.

ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS.....-0.5V to +4.6V
V_{IN} .....-0.5V to VCC+0.5V
Storage Temperature (plastic) .....-55°C to +125°
Junction Temperature .....+125°
Power Dissipation 2.0W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(0°C ≤ T_a ≤ 70°C; VCC = 3.3V -5% and +5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data Inputs (DQxx)	V_{IHD}	2.0	VCC+0.3	V	1,2
	All Other Inputs	V_{IH}	2.0	4.6	V	1,2
Input Low (Logic 0) Voltage		V_{II}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-	5	uA	
MODE and ZZ Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-	30	uA	6
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ VCC	IL_O	-	5	uA	
Output High Voltage	I_{OH} = -5.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		VCC	3.135	3.465	V	1
I/O Supply Voltage		VCCQ	3.135	VCC	V	1

DESCRIPTION	CONDITIONS	SYM	TYP	-4	-5	-6	-7	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH};cycle time ≥ ^tKC MIN; VCC =MAX; outputs open, ADV/LD# = X, f = f_{MAX} [2]	Icc	150	400	380	350	300	mA	3, 4, 5, 7
CMOS Standby	Device deselected; VCC = MAX; all inputs ≤ VSS +0.2 or ≥VCC -0.2; all inputs static; CLK frequency = 0	I_{SB2}	5	10	10	10	10	mA	4, 5, 7
TTL Standby	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; VCC = MAX; CLK frequency = 0	I_{SB3}	20	40	40	40	40	mA	4, 5, 7
Clock Running	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; VCC = MAX; CLK cycle time ≥ ^tKC MIN	I_{SB4}	50	95	85	80	70	mA	4, 5, 7

Note:

1. All voltages referenced to VSS (GND).
2. Overshoot: V_{IH} ≤ +6.0V for t ≤ ^tKC /2
   Undershoot: V_{IL} ≤ -2.0V for t ≤ ^tKC /2.
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. "Device Deselected" means the device is in POWER -DOWN mode as defined in the truth table. "Device Selected" means the device is active.
5. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
6. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±30 µA.
7. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of $1/t_{CYC}$; f = 0 means no input lines are changing.

AC ELECTRICAL CHARACTERISTICS

(Note 2) ($0^oC \leq T_A \leq 70^oC$; VCC = 3.3V -5% and +5%)

DESCRIPTION		- 4 143MHz		- 5 133MHz		-6 117MHz		- 7 100MHz			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock											
Clock cycle time	^tKC	7.0		7.5		8.5		10		ns	
Clock HIGH time	^tKH	2.0		2.2		3.4		3.5		ns	
Clock LOW time	^tKL	2.0		2.2		3.4		3.5		ns	
Output Times											
Clock to output valid	^tKQ		4.0		4.2		4.5		5.0	ns	
Clock to output invalid	^tKQX	1.5		1.5		1.5		1.5		ns	
Clock to output in Low-Z	^tKQLZ	1.5		1.5		1.5		1.5		ns	1, 3, 4
Clock to output in High-Z	^tKQHZ	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	ns	1, 3, 4
OE to output valid	^tOEQ		4.0		4.2		4.5		5.0	ns	
OE to output in Low-Z	^tOELZ	0		0		0		0		ns	1, 3, 4
OE to output in High-Z	^tOEHZ		4		5		6		6	ns	1, 3, 4
Setup Times											
Address and Controls	^tS	2.0		2.0		2.0		2.2		ns	5
Data In	^tSD	1.7		1.7		1.7		2.0		ns	5
Hold Times											
Address and Controls	^tH	0.5		0.5		0.5		0.5		ns	5
Data In	^tHD	0.5		0.5		0.5		0.5		ns	5

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25^oC$; f = 1 MHz VCC = 3.3V	C_I	4	4	pF	1
Input/Output Capacitance (DQ)		C_O	7	6.5	pF	1

THERMAL CONSIDERATION

DESCRIPTION	CONDITIONS	SYMBOL	TQFP TYP	UNITS	NOTES
Thermal Resistance - Junction to Ambient	Still air, soldered on 4.25 x 1.125 inch 4-layer PCB	Θ_{JA}	25	^{o}C/W	
Thermal Resistance - Junction to Case		Θ_{JC}	9	^{o}C/W	

Note:

1. This parameter is sampled.
2. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
3. Output loading is specified with CL=5pF as in Fig. 2.
4. At any given temperature and voltage condition, ^tKQHZ is less than ^tKQLZ and ^tOEHZ is less than ^tOELZ.
5. This is a synchronous device. All synchronous inputs must meet specified setup and hold time, except for “don’t care” as defined in the truth table.
6. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.

AC TEST CONDITIONS

Input pulse levels	0V to 3V
Input slew rate	1.0V/ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

OUTPUT LOADS

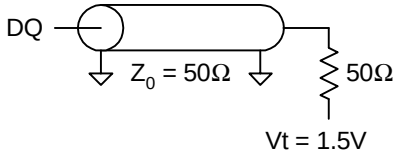


Fig. 1 OUTPUT LOAD EQUIVALENT

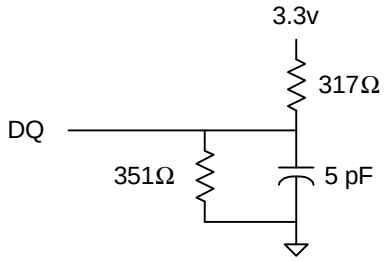
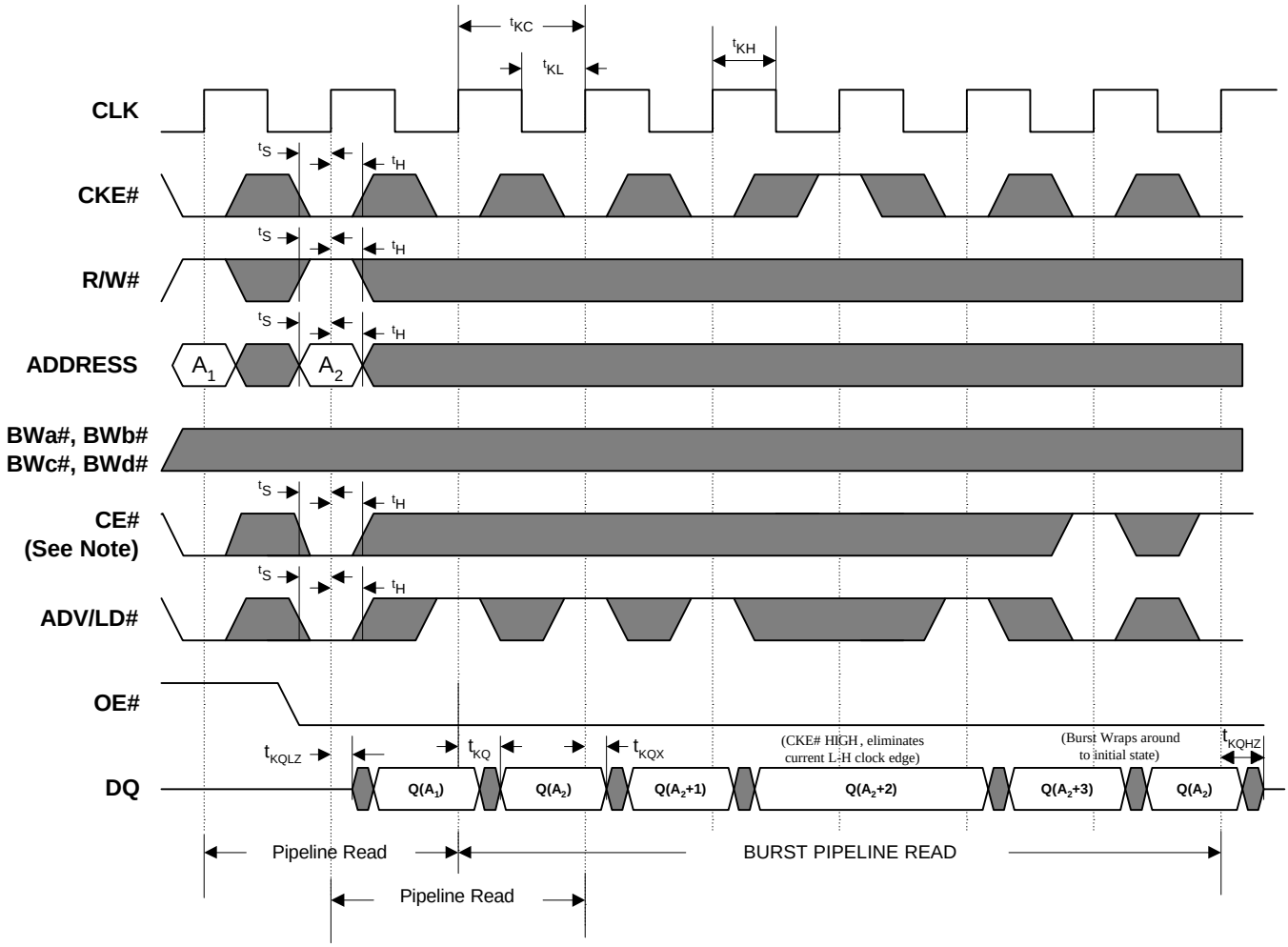


Fig. 2 OUTPUT LOAD EQUIVALENT

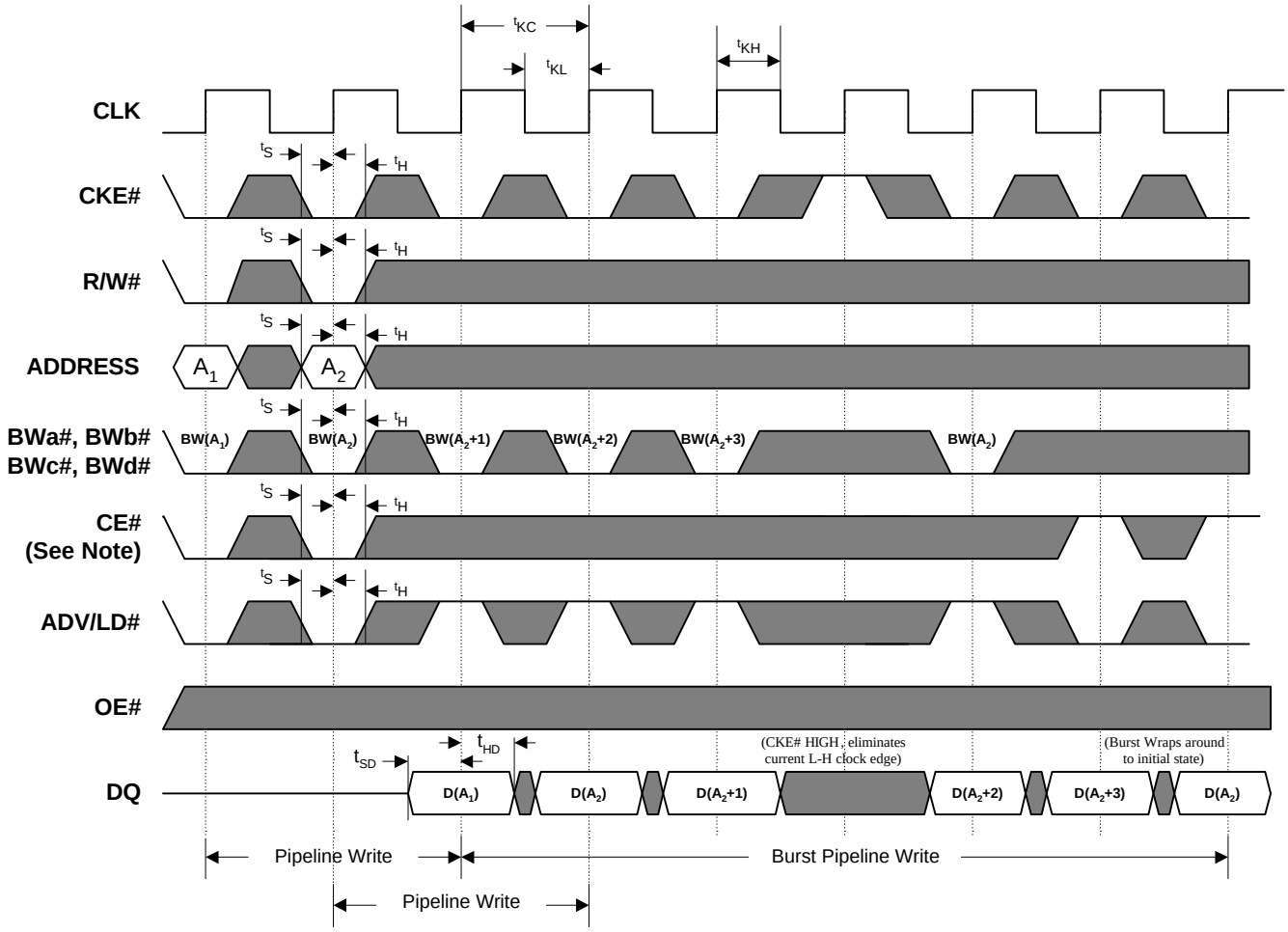
READ TIMING



Note:

1. $Q(A_1)$ represents the first output from the external address A_1. $Q(A_2)$ represents the first output from the external address A_2; $Q(A_2+1)$ represents the next output data in the burst sequence of the base address A_2, etc. where address bits SA0 and SA1 are advancing for the four word burst in the sequence defined by the state of the MODE input.
2. CE2# timing transitions are identical to the CE# signal. For example, when CE# is LOW on this waveform, CE2# is LOW. CE2 timing transitions are identical but inverted to the CE# signal. For example, when CE# is LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD# LOW.
4. R/W# is “Don’t Care” when the SRAM is bursting (ADV/LD# sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM.

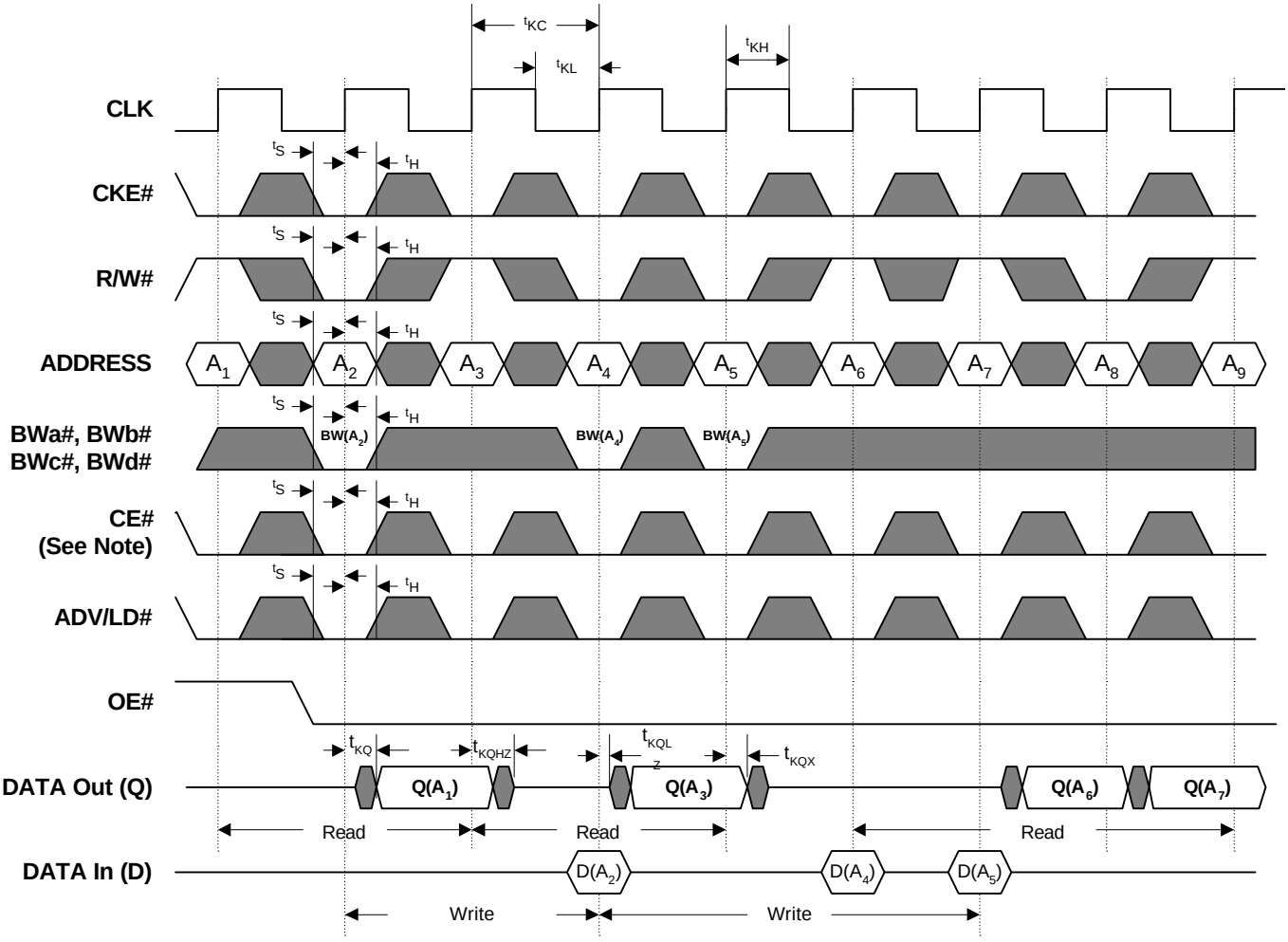
WRITE TIMING



Note:

1. D(A_1) represents the first input to the external address A1. D(A_2) represents the first input to the external address A_2; D(A_2+1) represents the next input data in the burst sequence of the base address A_2, etc. where address bits SA0 and SA1 are advancing for the four word burst in the sequence defined by the state of the MODE input.
2. CE2# timing transitions are identical to the CE# signal. For example, when CE# is LOW on this waveform, CE2# is LOW. CE2 timing transitions are identical but inverted to the CE# signal. For example, when CE# is LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD# LOW.
4. R/W# is “Don’t Care” when the SRAM is bursting (ADV/LD# sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals (BWx#) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W# signal is sampled LOW when ADV/LD# is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

READ/WRITE TIMING



Note:

1. $Q(A_1)$ represents the first output from the external address A_1. $D(A_2)$ represents the input data to the SRAM corresponding to address A_2.
2. CE2# timing transitions are identical to the CE# signal. For example, when CE# is LOW on this waveform, CE2# is LOW. CE2 timing transitions are identical but inverted to the CE# signal. For example, when CE# is LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals (BWx#) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W# signal is sampled LOW when ADV/LD# is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

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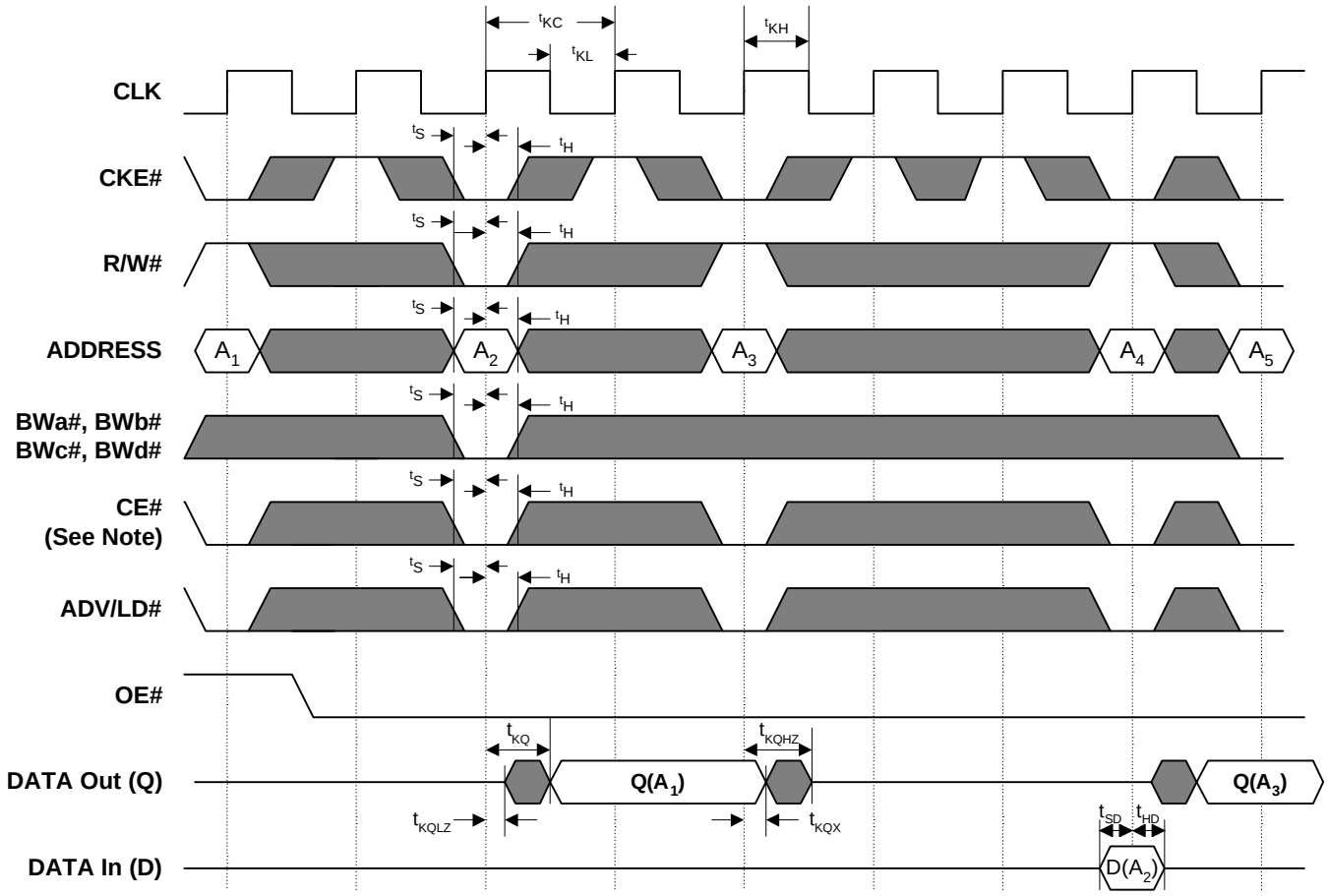
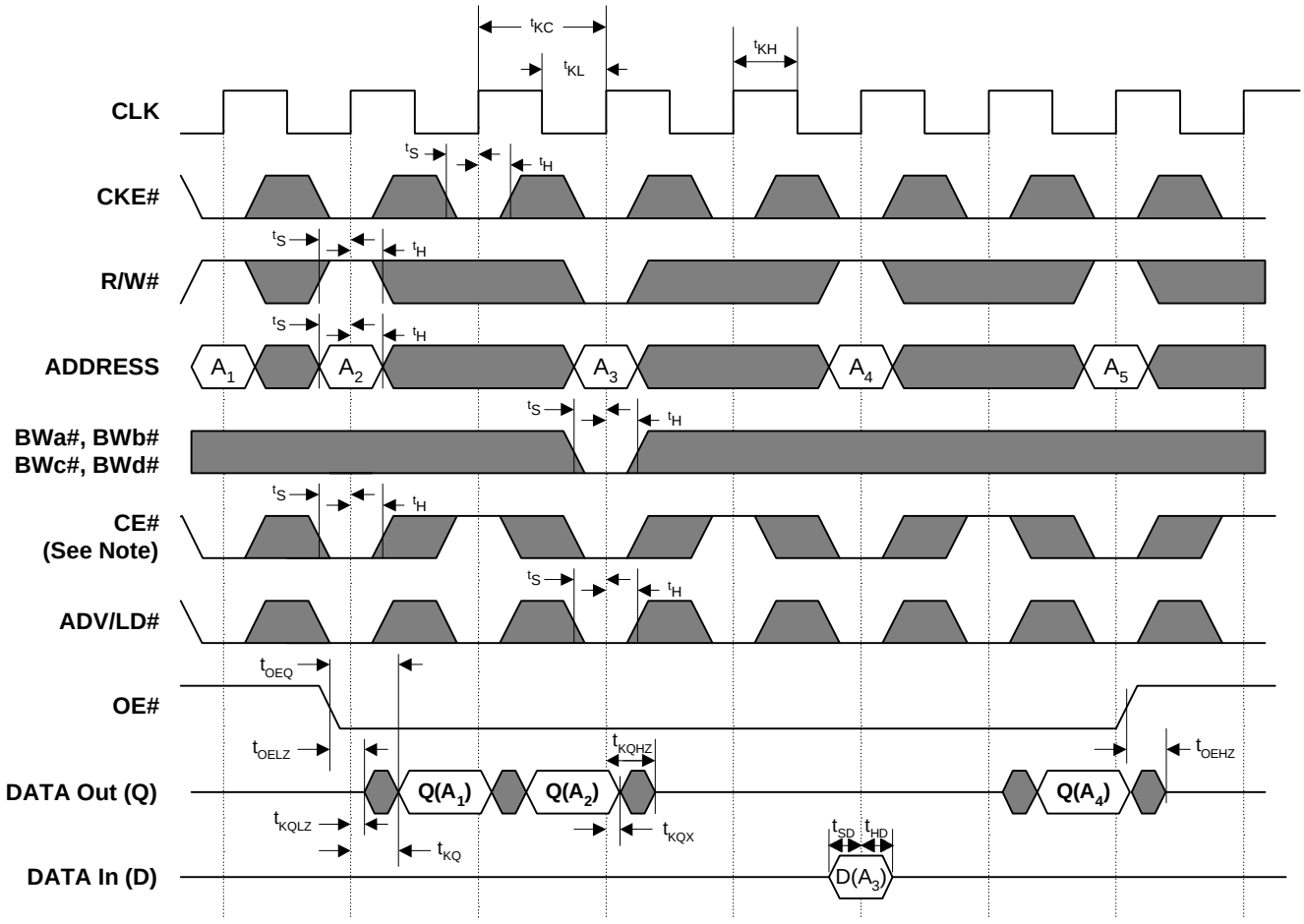
CKE# TIMING



Note:

1. $Q(A_1)$ represents the first output from the external address A_1. $D(A_2)$ represents the input data to the SRAM corresponding to address A_2.
2. CE2# timing transitions are identical to the CE# signal. For example, when CE# is LOW on this waveform, CE2# is LOW. CE2 timing transitions are identical but inverted to the CE# signal. For example, when CE# is LOW on this waveform, CE2 is HIGH.
3. CKE# when sampled HIGH on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal register in the SRAM will retain their previous state.
4. Individual Byte Write signals (BWx#) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W# signal is sampled LOW when ADV/LD# is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

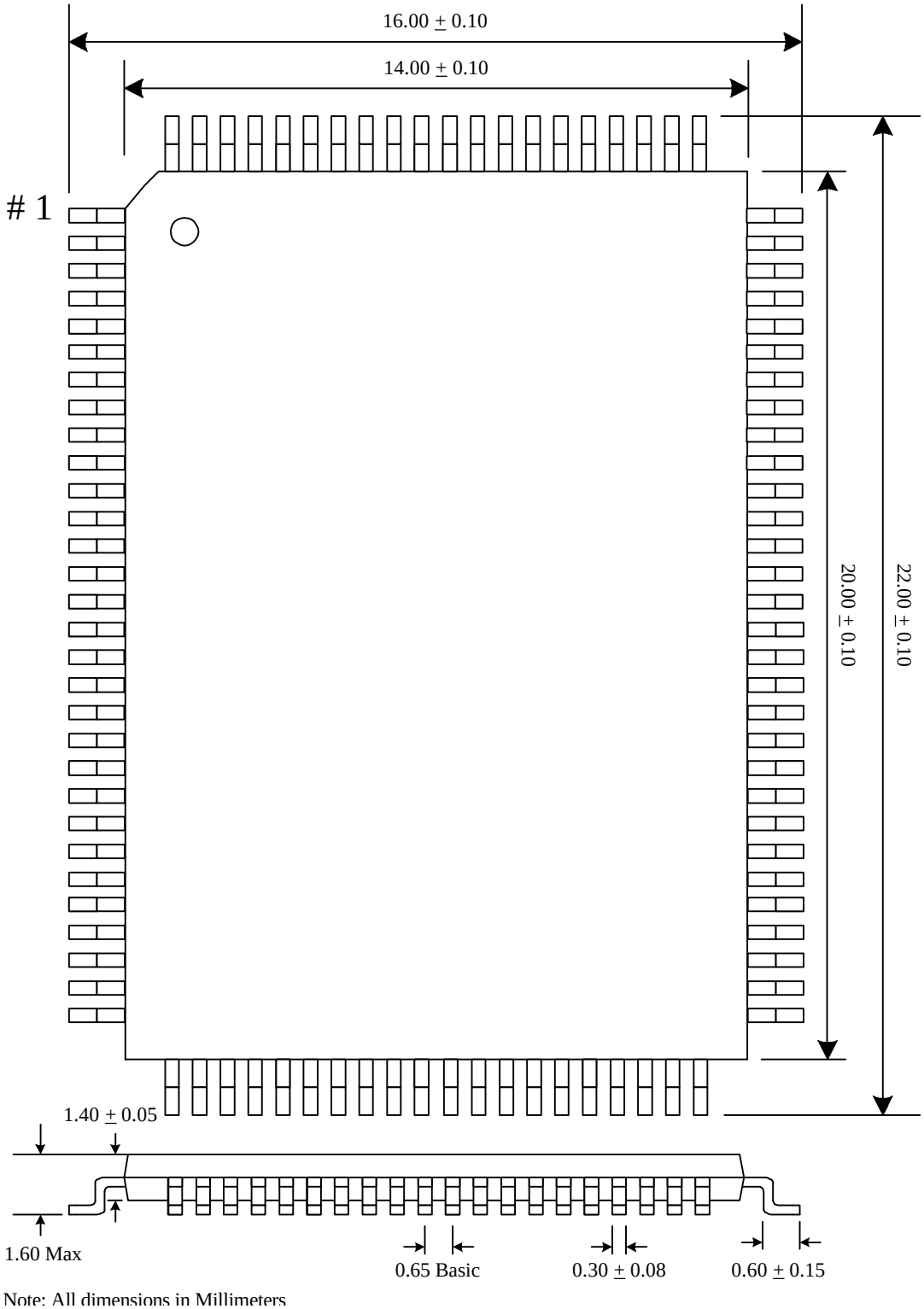
CE# TIMING



Note:

1. $Q(A_1)$ represents the first output from the external address A_1. $D(A_3)$ represents the input data to the SRAM corresponding to address A_3, etc.
2. CE2# timing transitions are identical to the CE# signal. For example, when CE# is LOW on this waveform, CE2# is LOW. CE2 timing transitions are identical but inverted to the CE# signal. For example, when CE# is LOW on this waveform, CE2 is HIGH.
3. When either one of the Chip enables (CE#, CE2 or CE2#) is sampled inactive at the rising clock edge, a chip deselect cycle is initiated. The data-bus High-Z two cycles after the initiation of the deselect cycle. This allows for any pending data transfers (reads or writes) to be completed.
4. Individual Byte Write signals (BWx#) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W# signal is sampled LOW when ADV/LD# is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

100 Pin TQFP Package Dimensions



Note: All dimensions in Millimeters

Ordering Information