HM6289 Series

16384-word × 4-bit High Speed CMOS Static RAM (with $\overline{OE}$)

HITACHI

Description

The Hitachi HM6289 is a high speed 64 k static RAM organized as 16-kword × 4-bit. It realizes high speed access time (25/35 ns) and low power consumption, employing CMOS process technology. It is most advantageous for high speed and high density memory, such as in cache memory for mainframes or 32-bit MPUs. The HM6289, packaged in a 300-mil SOJ, is available for high density mounting. The low power version retains the data with battery backup.

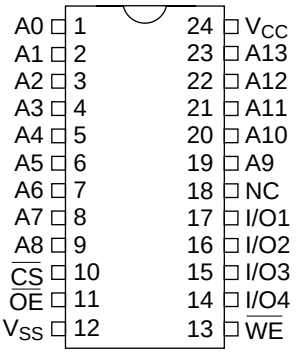
Features

- High speed access time:
  - — t_{AA}: 25/35 ns (max)
  - — t_{OE}: 12/15 ns (max)
- High density 24-pin S0J package
- Low power
  - — Active mode: 300 mW (typ)
  - — Standby mode: 100 μW (typ)
- Single 5 V supply
- Completely static memory: No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

Ordering Information

Type No.	Access Time	Package
HM6289JP-25	25 ns	300-mill, 24-pin SOJ (CP-24D)
HM6289JP-35	35 ns	
HM6289LJP-25	25 ns	
HM6289LJP-35	35 ns	

Pin Arrangement

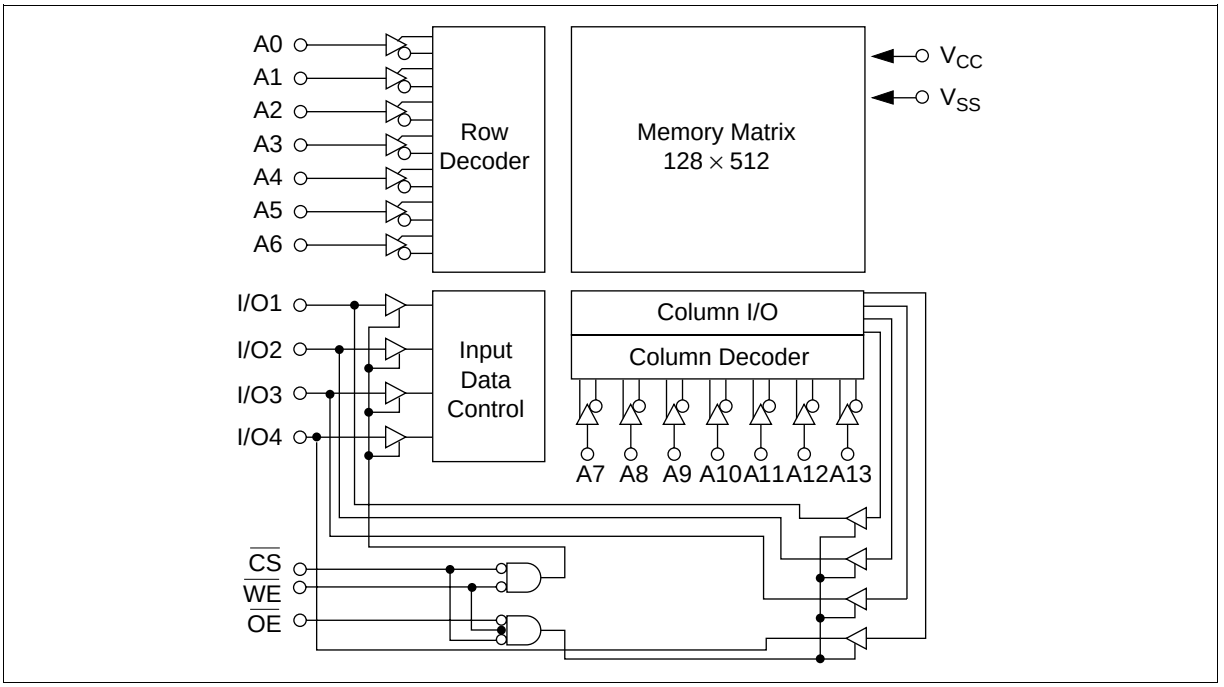


(Top view)

Pin Description

Pin Name	Function
A0 – A13	Address
I/O1 – I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{cc}	Power supply
V_{ss}	Ground

Block Diagram



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	Dout	Read cycle (1) – (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1) – (2)
L	L	L	Write	I_{CC}	Din	Write cycle (3) – (6)

Note: ×: Don't care (H or L).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Vin	–0.5 [*1] to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Note: 1. Vin min = –2.0 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5 [*1]	—	0.8	V

Note: 1. V_{IL} min = –2.0 V for pulse widths ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ[*1]	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max Vin = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}
Operating V_{CC} current	I_{CC}	—	60	120	mA	$\overline{CS}$ = V_{IL}, Iout = 0 mA, min cycle
Standby V_{CC} current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby V_{CC} current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, 0 V ≤ Vin ≤ 0.2 V or V_{CC} – 0.2 V ≤ V_{in}
	I_{SB1} [*2]	—	—	0.1	µA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.
2. L-version

Capacitance (Ta = 25°C, f = 1 MHz)[*1]

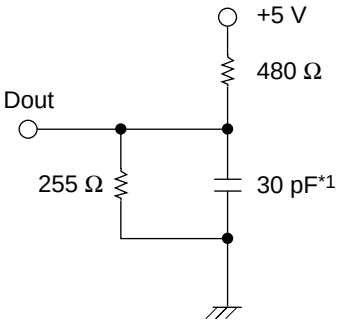
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. These parameters are sampled and not 100% tested.

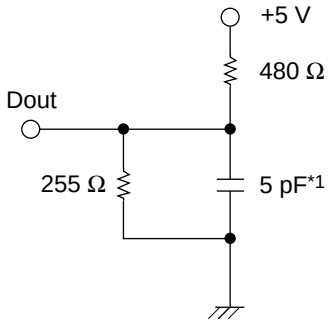
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)



Output load (B)
(for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, and t_{OW})

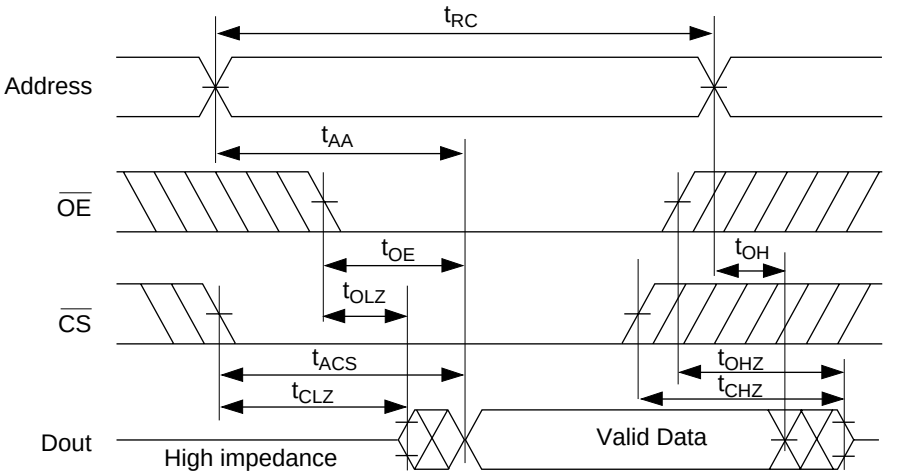
Note: 1. Including scope and jig.

Read Cycle

		HM6289-25		HM6289-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Chip selection to output in low-Z	t_{CLZ} *1	5	—	5	—	ns
Output enable to output valid	t_{OE}	—	12	—	15	ns
Output enable to output in low-Z	t_{OLZ} *1	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ} *1	0	12	0	20	ns
Chip disable to output high-Z	t_{OHZ} *1	0	10	0	10	ns
Output hold from address change	t_{OH}	3	—	5	—	ns

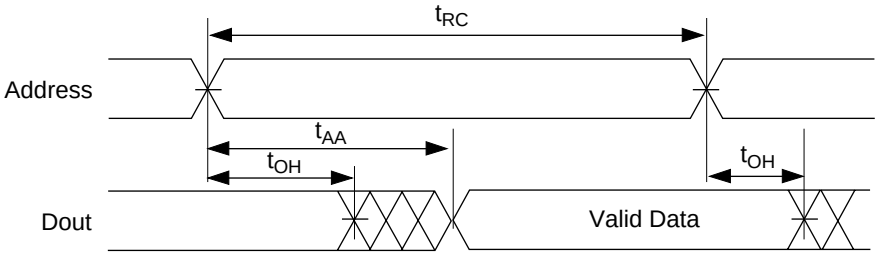
Note: 1. Output transition is measured ±200 mV from steady state voltage with load (B). These parameters are sampled and not 100% tested.

Read Timing Waveform (1)



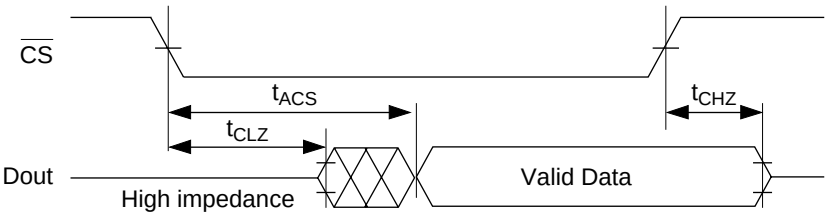
Note: $\overline{WE}$ is high for read cycle.

Read Timing Waveform (2)



Notes: 1. $\overline{WE}$ is high for read cycle.
2. Device is continously selected, $\overline{CS}$ = V_{IL}.
3. $\overline{OE}$ = V_{IL}

Read Timing Waveform (3)



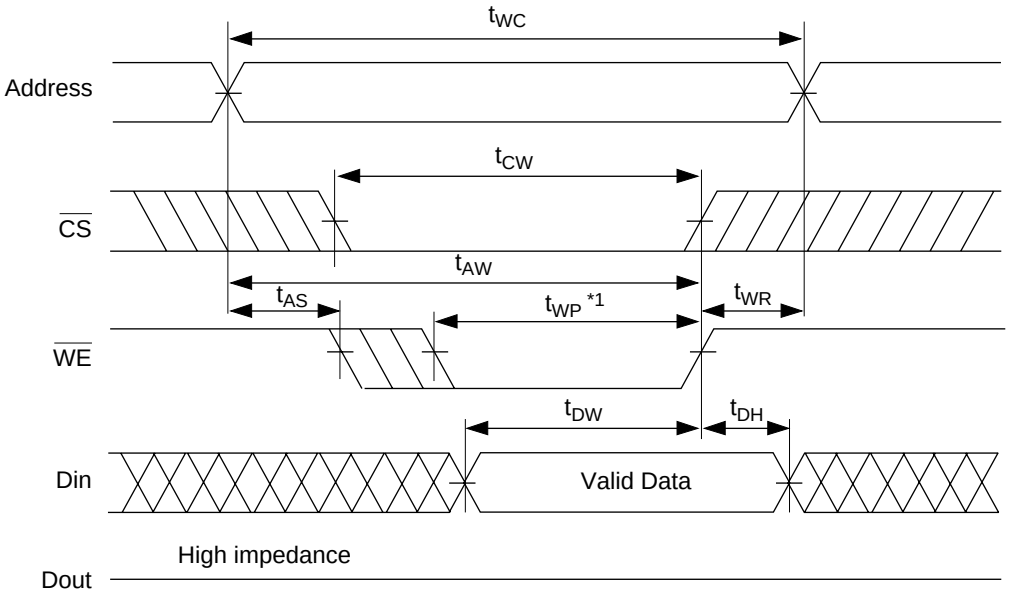
Notes: 1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE} = V_{IL}$

Write Cycle

		HM6289-25		HM6289-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Output disable to output in high-Z[*1]	t_{OHZ}	0	10	0	10	ns
Write to output in high-Z[*1]	t_{WHZ}	0	8	0	10	ns
Data to write time overlap	t_{DW}	12	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Output active from end of write [*1]	t_{OW}	5	—	5	—	ns

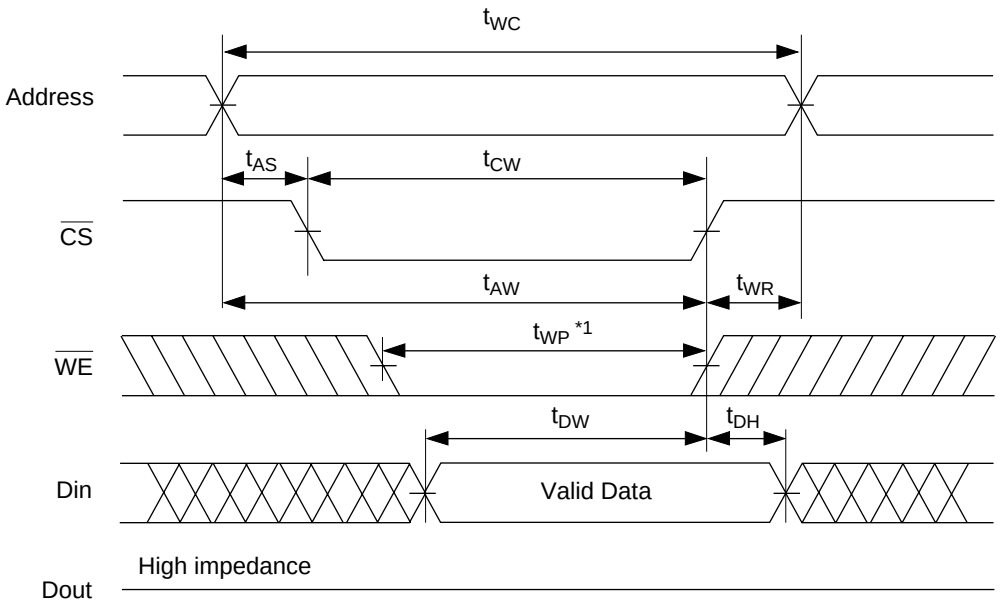
Note: 1. Output transition is measured ±200 mV from steady state voltage with load (B). These parameters are sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{OE}$ = High, $\overline{WE}$ = Controlled)



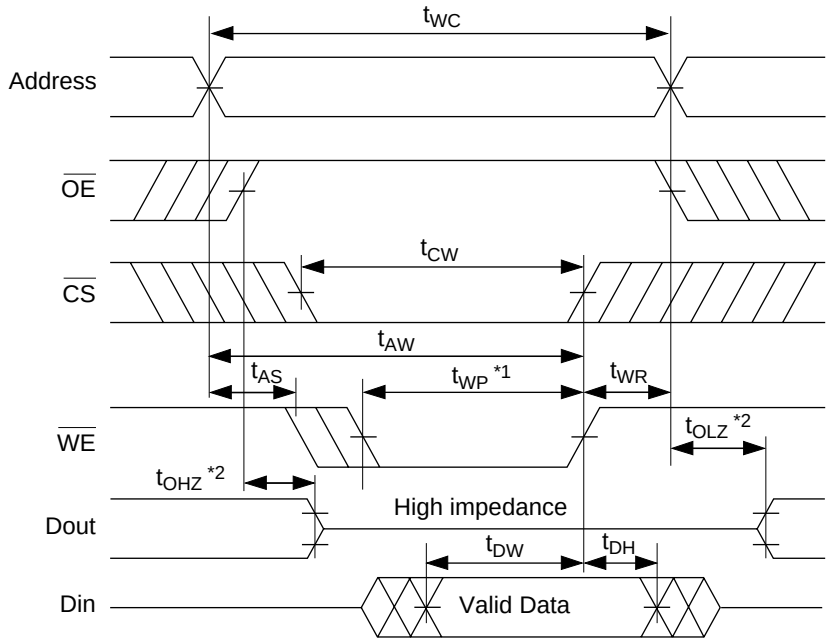
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Timing Waveform (2) ($\overline{OE}$ = High, $\overline{CS}$ = Controlled)



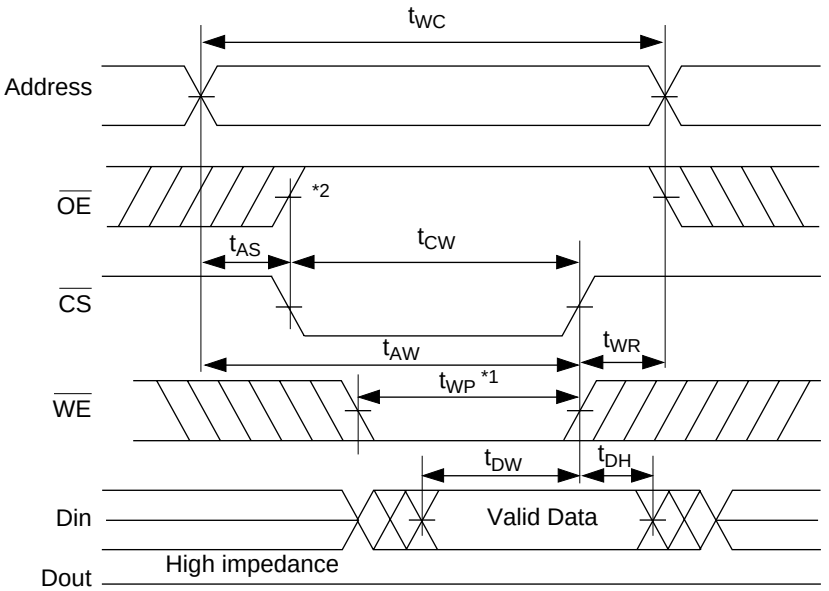
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Timing Waveform (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ = Controlled)



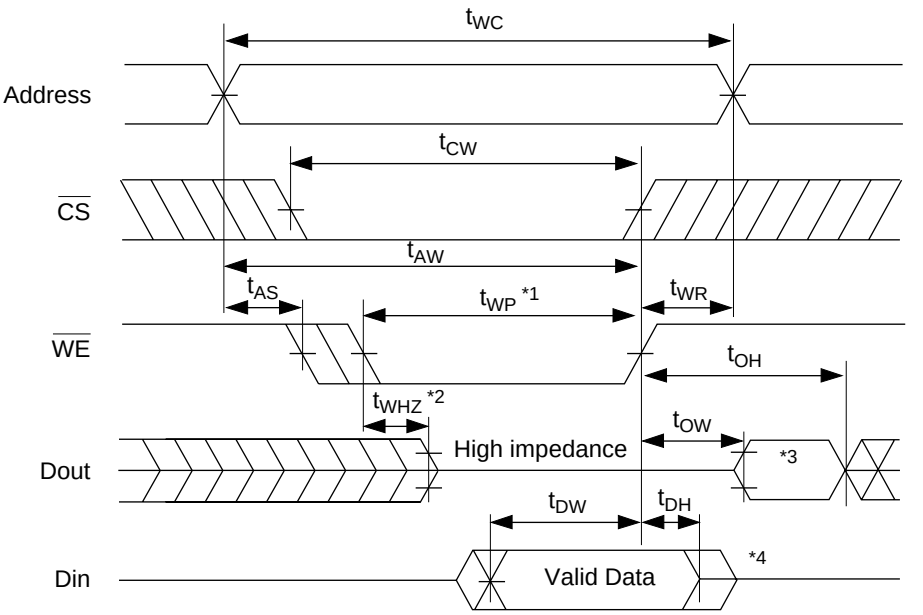
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

Write Timing Waveform (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ = Controlled)



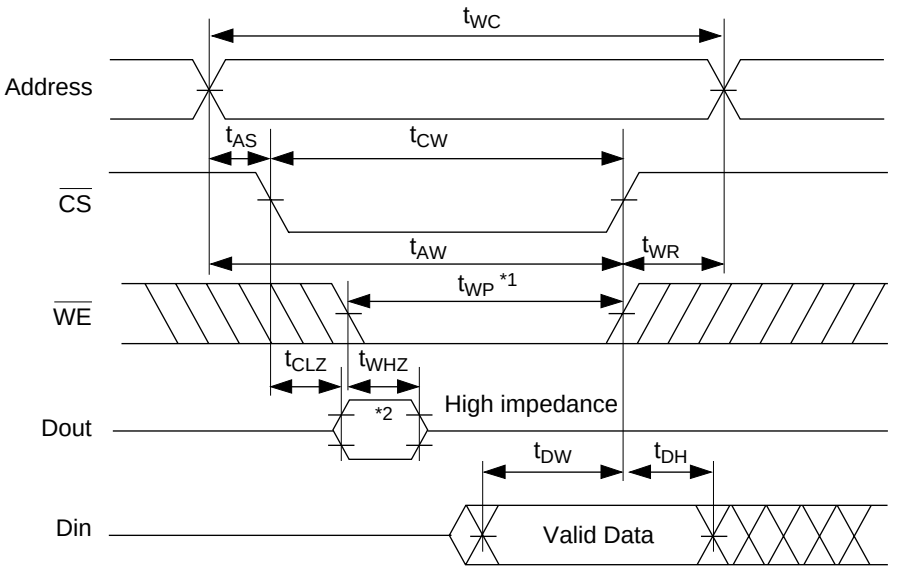
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

Write Timing Waveform (5) ($\overline{OE}$ = Low, $\overline{WE}$ = Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state after t_{OW}. Then the data input signals of opposite phase to the outputs must not be applied to them.

Write Timing Waveform (6) ($\overline{OE}$ = Low, $\overline{CS}$ = Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

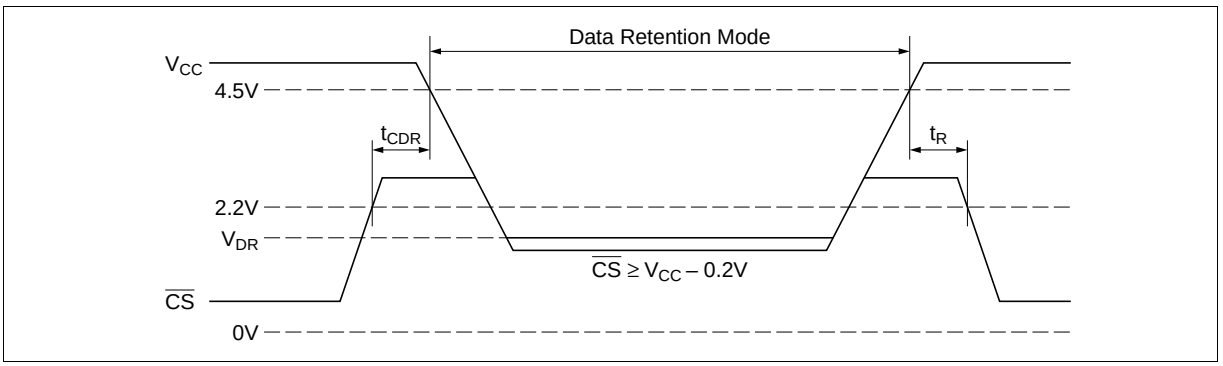
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

These characteristics are guaranteed for the L-version only.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq V_{CC} - 0.2$ V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	—	50*2	µA	
		—	—	35*3	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Notes: 1. t_{RC} = Read cycle time
2. V_{CC} = 3.0 V
3. V_{CC} = 2.0 V

Low V_{CC} Data Retention Waveform



Package Dimension

HM6289JP/LJP Series (CP-24D) Unit: mm