

Advanced Information

- 4 194 304 words by 32-bit organization (alternative 8 388 608 words by 16-bit)
- Fast access and cycle time
 - 50 ns access time
 - 90 ns cycle time (-50 version)
 - 60 ns access time
 - 110 ns cycle time (-60 version)
- Fast page mode capability
 - 35 ns cycle time (-50 version)
 - 40 ns cycle time (-60 version)
- Single + 5 V ($\pm 10\%$) supply
- Low power dissipation
 - max. 5280 mW active (HYM 324020S/GS-50)
 - max. 4840 mW active (HYM 324020S/GS-60)
 - CMOS – 44 mW standby
 - TTL – 88 mW standby
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - $\overline{\text{RAS}}$ -only-refresh
 - Hidden-refresh
- 8 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module with 22.86 mm (900 mil) height
- Utilizes eight 4Mx4-DRAMs in 300mil wide SOJ packages
- 2048 refresh cycles / 32 ms
- Optimized for use in byte-write non-parity applications
- Tin-Lead contact pads (S - version)
- Gold contact pads (GS - version)

The HYM 324020S/GS-50/-60 is a 16 MByte DRAM module organized as 4 194 304 words by 32-bit in a 72-pin single-in-line package comprising eight HYB 5117400BJ 4M x 4 DRAMs in 300 mil wide SOJ-packages mounted together with eight 0.2 μ F ceramic decoupling capacitors on a PC board.

The HYM 324020S/GS-50/-60 can also be used as a 8 388 608 words by 16-bits dynamic RAM module by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ..., DQ15 and DQ31, respectively.

Each HYB 5117400BJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

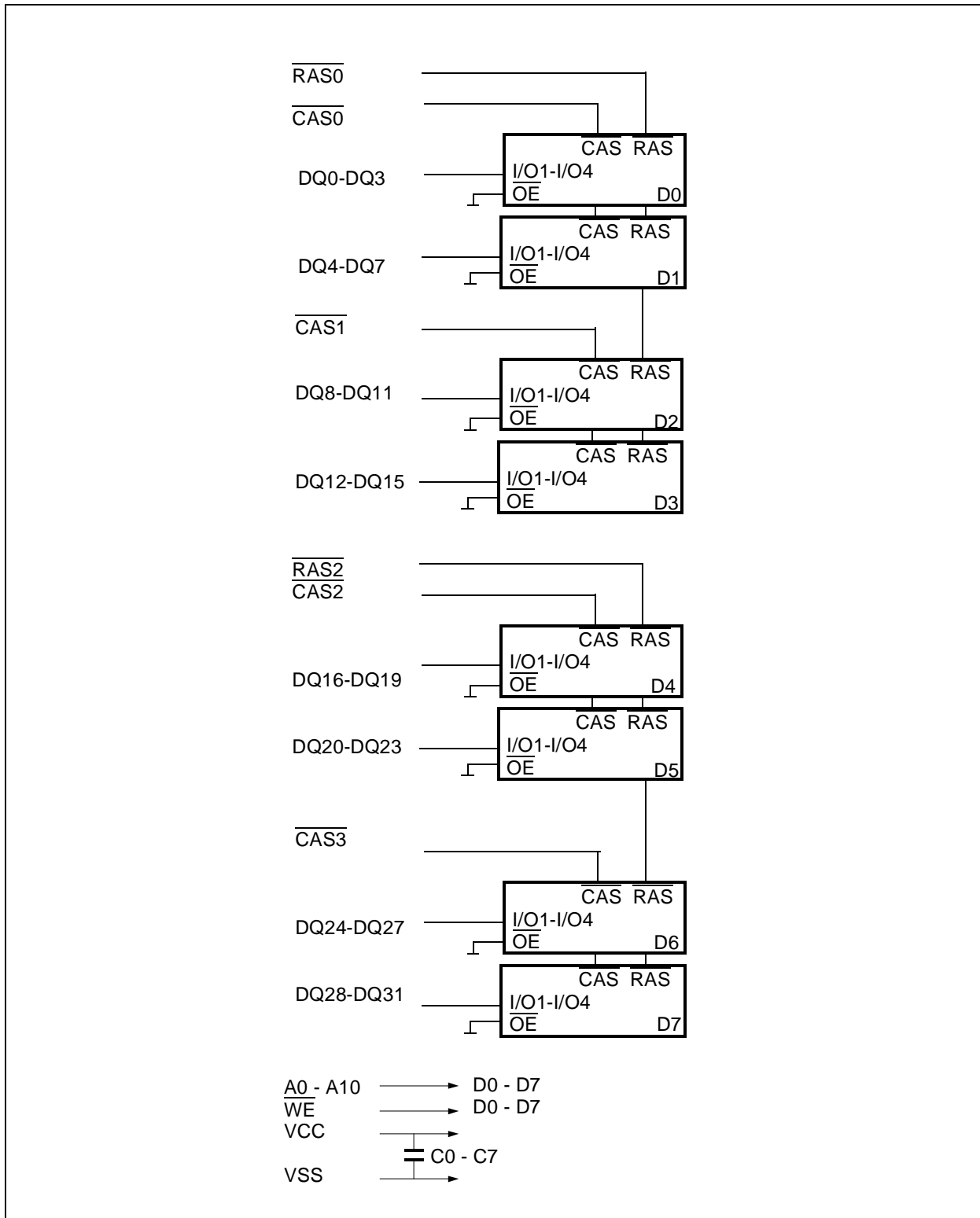
The common I/O feature on the HYM 324020S/GS-50/-60 dictates the use of early write cycles.

Ordering Information

Type	Ordering Code	Package	Description
HYM 324020S-50	on request	L-SIM-72-12	DRAM Module (access time 50 ns)
HYM 324020S-60	Q67100-Q979	L-SIM-72-12	DRAM Module (access time 60 ns)
HYM 324020GS-50	on request	L-SIM-72-12	DRAM Module (access time 50 ns)
HYM 324020GS-60	Q67100-Q2005	L-SIM-72-12	DRAM Module (access time 60 ns)

Pin Configuration

<table border="0" style="width: 100%;"> <tr><td>VSS</td><td>1</td><td>DQ0</td><td>2</td></tr> <tr><td>DQ16</td><td>3</td><td>DQ1</td><td>4</td></tr> <tr><td>DQ17</td><td>5</td><td>DQ2</td><td>6</td></tr> <tr><td>DQ18</td><td>7</td><td>DQ3</td><td>8</td></tr> <tr><td>DQ19</td><td>9</td><td>VCC</td><td>10</td></tr> <tr><td>N.C.</td><td>11</td><td>A0</td><td>12</td></tr> <tr><td>A1</td><td>13</td><td>A2</td><td>14</td></tr> <tr><td>A3</td><td>15</td><td>A4</td><td>16</td></tr> <tr><td>A5</td><td>17</td><td>A6</td><td>18</td></tr> <tr><td>A10</td><td>19</td><td>DQ4</td><td>20</td></tr> <tr><td>DQ20</td><td>21</td><td>DQ5</td><td>22</td></tr> <tr><td>DQ21</td><td>23</td><td>DQ6</td><td>24</td></tr> <tr><td>DQ22</td><td>25</td><td>DQ7</td><td>26</td></tr> <tr><td>DQ23</td><td>27</td><td>A7</td><td>28</td></tr> <tr><td>N.C.</td><td>29</td><td>VCC</td><td>30</td></tr> <tr><td>A8</td><td>31</td><td>A9</td><td>32</td></tr> <tr><td>N.C.</td><td>33</td><td>$\overline{\text{RAS2}}$</td><td>34</td></tr> <tr><td>N.C.</td><td>35</td><td>N.C.</td><td>36</td></tr> <tr><td colspan="4"> </td></tr> <tr><td>N.C.</td><td>37</td><td>N.C.</td><td>38</td></tr> <tr><td>VSS</td><td>39</td><td>$\overline{\text{CAS0}}$</td><td>40</td></tr> <tr><td>$\overline{\text{CAS2}}$</td><td>41</td><td>$\overline{\text{CAS3}}$</td><td>42</td></tr> <tr><td>$\overline{\text{CAS1}}$</td><td>43</td><td>RAS0</td><td>44</td></tr> <tr><td>N.C.</td><td>45</td><td>N.C.</td><td>46</td></tr> <tr><td>WE</td><td>47</td><td>N.C.</td><td>48</td></tr> <tr><td>DQ8</td><td>49</td><td>DQ24</td><td>50</td></tr> <tr><td>DQ9</td><td>51</td><td>DQ25</td><td>52</td></tr> <tr><td>DQ10</td><td>53</td><td>DQ26</td><td>54</td></tr> <tr><td>DQ11</td><td>55</td><td>DQ27</td><td>56</td></tr> <tr><td>DQ12</td><td>57</td><td>DQ28</td><td>58</td></tr> <tr><td>VCC</td><td>59</td><td>DQ29</td><td>60</td></tr> <tr><td>DQ13</td><td>61</td><td>DQ30</td><td>62</td></tr> <tr><td>DQ14</td><td>63</td><td>DQ31</td><td>64</td></tr> <tr><td>DQ15</td><td>65</td><td>N.C.</td><td>66</td></tr> <tr><td>PD0</td><td>67</td><td>PD1</td><td>68</td></tr> <tr><td>PD2</td><td>69</td><td>PD3</td><td>70</td></tr> <tr><td>N.C.</td><td>71</td><td>VSS</td><td>72</td></tr> </table>	VSS	1	DQ0	2	DQ16	3	DQ1	4	DQ17	5	DQ2	6	DQ18	7	DQ3	8	DQ19	9	VCC	10	N.C.	11	A0	12	A1	13	A2	14	A3	15	A4	16	A5	17	A6	18	A10	19	DQ4	20	DQ20	21	DQ5	22	DQ21	23	DQ6	24	DQ22	25	DQ7	26	DQ23	27	A7	28	N.C.	29	VCC	30	A8	31	A9	32	N.C.	33	$\overline{\text{RAS2}}$	34	N.C.	35	N.C.	36					N.C.	37	N.C.	38	VSS	39	$\overline{\text{CAS0}}$	40	$\overline{\text{CAS2}}$	41	$\overline{\text{CAS3}}$	42	$\overline{\text{CAS1}}$	43	RAS0	44	N.C.	45	N.C.	46	WE	47	N.C.	48	DQ8	49	DQ24	50	DQ9	51	DQ25	52	DQ10	53	DQ26	54	DQ11	55	DQ27	56	DQ12	57	DQ28	58	VCC	59	DQ29	60	DQ13	61	DQ30	62	DQ14	63	DQ31	64	DQ15	65	N.C.	66	PD0	67	PD1	68	PD2	69	PD3	70	N.C.	71	VSS	72		<p>Pin Names</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td>A0-A10</td><td>Address Inputs for HYM 324020S/GS</td></tr> <tr><td>DQ0-DQ31</td><td>Data Input/Output</td></tr> <tr><td>$\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$</td><td>Column Address Strobe</td></tr> <tr><td>$\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$</td><td>Row Address Strobe</td></tr> <tr><td>$\overline{\text{WE}}$</td><td>Read/Write Input</td></tr> <tr><td>V_{CC}</td><td>Power (+ 5 V)</td></tr> <tr><td>V_{SS}</td><td>Ground</td></tr> <tr><td>PD</td><td>Presence Detect Pin</td></tr> <tr><td>N.C.</td><td>No Connection</td></tr> </table> <p>Presence Detect Pins</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr><th></th><th>-50</th><th>-60</th></tr> </thead> <tbody> <tr><td>PD0</td><td>V_{SS}</td><td>V_{SS}</td></tr> <tr><td>PD1</td><td>N.C.</td><td>N.C.</td></tr> <tr><td>PD2</td><td>V_{SS}</td><td>N.C.</td></tr> <tr><td>PD3</td><td>V_{SS}</td><td>N.C.</td></tr> </tbody> </table>	A0-A10	Address Inputs for HYM 324020S/GS	DQ0-DQ31	Data Input/Output	$\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$	Column Address Strobe	$\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$	Row Address Strobe	$\overline{\text{WE}}$	Read/Write Input	V_{CC}	Power (+ 5 V)	V_{SS}	Ground	PD	Presence Detect Pin	N.C.	No Connection		-50	-60	PD0	V_{SS}	V_{SS}	PD1	N.C.	N.C.	PD2	V_{SS}	N.C.	PD3	V_{SS}	N.C.
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Block Diagram

Absolute Maximum Ratings

Operation temperature range	0 to + 70 °C
Storage temperature range.....	- 55 to 125 °C
Input/output voltage	-0.5V to min (V _{CC} +0.5, 7.0) V
Power supply voltage.....	- 1 to + 7 V
Power dissipation.....	6.72 W
Data out current (short circuit)	50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to 70 °C, $V_{SS} = 0$ V, $V_{CC} = 5$ V \pm 10 %; $t_T = 5$ ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	$V_{CC}+0.5$	V	1)
Input low voltage	V_{IL}	- 0.5	0.8	V	1)
Output high voltage ($I_{OUT} = - 5$ mA)	V_{OH}	2.4	-	V	1)
Output low voltage ($I_{OUT} = 4.2$ mA)	V_{OL}	-	0.4	V	1)
Input leakage current (0 V $\leq V_{IH} \leq V_{CC} + 0.3$ V, all other pins = 0 V)	$I_{(L)}$	- 20	20	μ A	1)
Output leakage current (DO is disabled, 0 V $\leq V_{OUT} \leq V_{CC} + 0.3$ V)	$I_{O(L)}$	- 10	10	μ A	1)
Average V_{CC} supply current: -50 ns version -60 ns version (RAS, CAS, address cycling: $t_{RC} = t_{RC}$ min.)	I_{CC1}	-	960 880	mA mA	2) 3) 4) 2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	-	16	mA	-
Average V_{CC} supply current, during \overline{RAS} -only refresh cycles: -50 ns version -60 ns version (\overline{RAS} cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min.)	I_{CC3}	-	960 880	mA mA	2) 4) 2) 4)
Average V_{CC} supply current, during fast page mode: -50 ns version -60 ns version ($\overline{RAS} = V_{IL}$, \overline{CAS} , address cycling: $t_{PC} = t_{PC}$ min.)	I_{CC4}	-	320 280	mA mA	2) 3) 4) 2) 3) 4)

DC Characteristics (cont'd)

$T_A = 0$ to 70 °C, $V_{SS} = 0$ V, $V_{CC} = 5$ V \pm 10 %; $t_T = 5$ ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V)	I_{CC5}	–	8	mA	1)
Average V_{CC} supply current, during \overline{CAS} - before-RAS refresh mode: -50 ns version -60 ns version (\overline{RAS} , \overline{CAS} cycling: $t_{RC} = t_{RC}$ min.)	I_{CC6}	– –	960 880	mA mA	2) 4) 2) 4)

Capacitance

$T_A = 0$ to 70 °C, $V_{CC} = 5$ V \pm 10 %, $f = 1$ MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance ($A0$ to $A10$, \overline{WE})	C_{11}	–	75	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{12}	–	45	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{13}	–	25	pF
I/O capacitance (DQ0-DQ31)	C_{10}	–	15	pF

AC Characteristics ⁵⁾⁶⁾

$T_A = 0$ to 70 °C, $V_{CC} = 5$ V \pm 10 %, $t_T = 5$ ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

common parameters

Random read or write cycle time	t_{RC}	90	–	110	–	ns	
\overline{RAS} precharge time	t_{RP}	30	–	40	–	ns	
\overline{RAS} pulse width	t_{RAS}	50	10k	60	10k	ns	
\overline{CAS} pulse width	t_{CAS}	13	10k	15	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	15	–	ns	
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	18	37	20	45		
\overline{RAS} to column address delay time	t_{RAD}	13	25	15	30	ns	
\overline{RAS} hold time	t_{RSH}	13		15	–	ns	
\overline{CAS} hold time	t_{CSH}	50		60	–	ns	
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	5	–	5	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period	t_{REF}	–	32	–	32	ms	

Read Cycle

Access time from \overline{RAS}	t_{RAC}	–	50	–	60	ns	8, 9
Access time from \overline{CAS}	t_{CAC}	–	13	–	15	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	ns	8,10
Column address to \overline{RAS} lead time	t_{RAL}	25	–	30	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	11
Read command hold time referenced to \overline{RAS}	t_{RRH}	0	–	0	–	ns	11
\overline{CAS} to output in low-Z	t_{CLZ}	0	–	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	12

AC Characteristics (cont'd) ⁵⁾⁶⁾

$T_A = 0$ to 70 °C, $V_{CC} = 5$ V \pm 10 %, $t_T = 5$ ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

Early Write Cycle

Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	ns	13
Write command to \overline{RAS} lead time	t_{RWL}	13	–	15	–	ns	
Write command to \overline{CAS} lead time	t_{CWL}	13	–	15	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	14
Data hold time	t_{DH}	10	–	10	–	ns	14

Fast Page Mode Cycle

Fast page mode cycle time	t_{PC}	35	–	40	–	ns	
\overline{CAS} precharge time	t_{CP}	10	–	10	–	ns	
Access time from \overline{CAS} precharge	t_{CPA}	–	30	–	35	ns	7
\overline{RAS} pulse width	t_{RAS}	50	200k	60	200k	ns	
\overline{CAS} precharge to \overline{RAS} Delay	t_{RHCP}	30	–	35	–	ns	

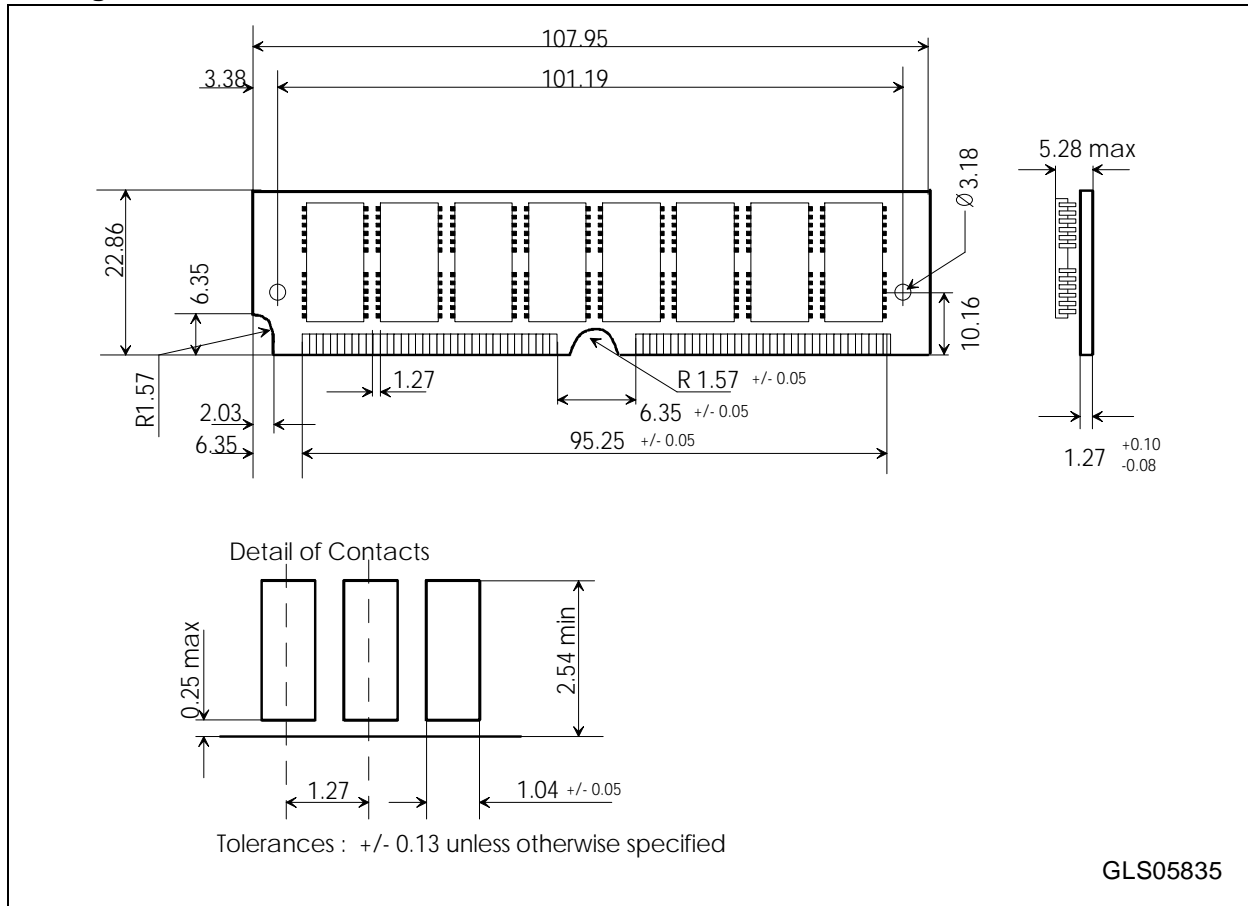
\overline{CAS} -before- \overline{RAS} Refresh Cycle

\overline{CAS} setup time	t_{CSR}	10	–	10	–	ns	
\overline{CAS} hold time	t_{CHR}	10	–	10	–	ns	
\overline{RAS} to \overline{CAS} precharge time	t_{RPC}	5	–	5	–	ns	
Write to \overline{RAS} precharge time	t_{WRP}	10	–	10	–	ns	
Write hold time referenced to \overline{RAS}	t_{WRH}	10	–	10	–	ns	

Notes:

- 1) All voltages are referenced to VSS.
- 2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
- 3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while $\overline{\text{RAS}} = \text{VIL}$. In the case of ICC4 it can be changed once or less during a fast page mode cycle (tPC).
- 5) An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before-RAS initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
- 6) AC measurements assume $t_T = 5 \text{ ns}$.
- 7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Transition times are also measured between VIH and VIL .
- 8) Measured with a load equivalent to 2 TTL loads and 100 pF.
- 9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.
- 10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.
- 11) Either tRCH or tRRH must be satisfied for a read cycle.
- 12) tOFF (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
- 13) tWCS is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If $t\text{WCS} > t\text{WCS}(\text{min.})$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle.
- 14) These parameters are referenced to the $\overline{\text{CAS}}$ leading edge.

Package Outline



**Module Package, L-SIM-72-12
(Single in-Line Memory Module)**