LT1533

Ultralow Noise 1A Switching Regulator

September 1997

FEATURES

- **Greatly Reduced Conducted and Radiated EMI (<60μV_{P-P} in Typical Application)**
- **Low Switching Harmonic Content**
- **Independent Control of Switch Voltage and Current Slew Rates**
- Two 1A Current Limited Power Switches
- Regulates Positive and Negative Voltages
- 20kHz to 250kHz Oscillator Frequency
- Easily Synchronized to External Clock
- Wide Input Voltage Range: 2.7V to 23V
- Low Shutdown Current: 12μA Typical
- Easier Layout than with Conventional Switchers
- Outputs Can Be Forced to 50% Duty Cycle for Unregulated Applications

APPLICATIONS

- Precision Instrumentation Systems
- Isolated Supplies for Industrial Automation
- Medical Instruments
- Wireless Communications
- Single Board Data Acquisition Systems

DESCRIPTION

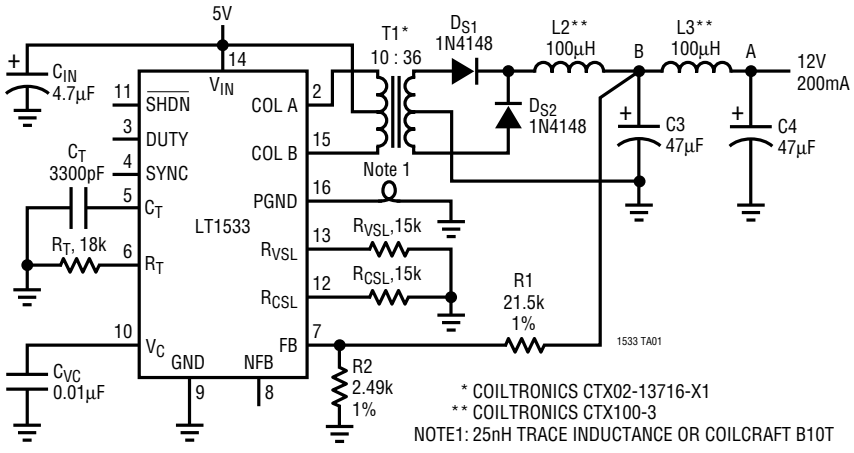
The LT®1533 is a new class of switching regulator designed to reduce conducted and radiated electromagnetic interference (EMI). Ultralow noise and EMI are achieved by providing user control of the output switch slew rates. Voltage and current slew rates can be independently programmed to optimize switcher harmonic content versus efficiency. The LT1533 can reduce high frequency harmonic power by as much as 40dB with only minor losses in efficiency.

The LT1533 utilizes a dual output switch current mode architecture optimized for low noise topologies. The IC includes two 1A power switches along with all necessary oscillator, control and protection circuitry. Unique error amp circuitry can regulate both positive and negative voltages. The internal oscillator may be synchronized to an external clock for more accurate placement of switching harmonics. Protection features include cycle by cycle short-circuit protection, undervoltage lockout and thermal shutdown.

Low minimum supply voltage and low supply current during shutdown make the LT1533 well suited for portable applications. The part may also be forced into a 50% duty cycle mode for unregulated applications. The LT1533 is available in the 16-pin narrow SO package.

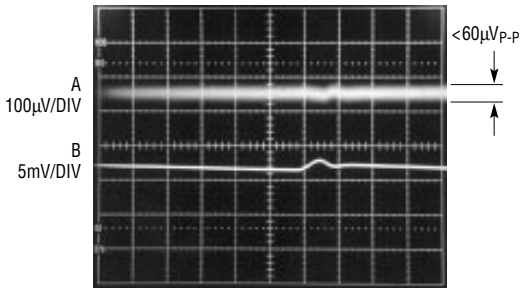
TYPICAL APPLICATION

Low Noise 5V to 12V Forward Push-Pull DC/DC Converter



* COILTRONICS CTX02-13716-X1
** COILTRONICS CTX100-3
NOTE1: 25nH TRACE INDUCTANCE OR COILCRAFT B10T

12V Output Noise (BW = 100MHz)

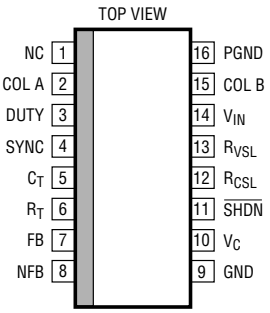


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage (V_{IN}) 30V
Switch Voltage (COL A, COL B) 30V
SHDN Pin Voltage 30V
Feedback Pin Current 10mA
Negative Feedback Pin Current ..... ±10mA
Storage Temperature Range ..... –65°C to 150°C
Operating Ambient Temperature Range ..... 0°C to 70°C
Operating Junction Temperature Range
(Note 2) ..... 0°C to 125°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD NARROW PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1533CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_C = 0.9V, V_{FB} = V_{REF}. COL A, COL B, $\overline{SHDN}$, NFB, DUTY pins open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifiers							
V_{REF}	Reference Voltage	Measured at Feedback Pin	 ●	1.235 1.215	1.250 1.250	1.265 1.275	V V
I_{FB}	Feedback Input Current	V_{FB} = V_{REF}	●		250	900	nA
FB_{REG}	Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 23V	●		0.003	0.03	%/V
V_{NFR}	Negative Feedback Reference Voltage	Measured at Negative Feedback Pin with Feedback Pin Open	●	–2.550	–2.500	–2.420	V
I_{NFR}	Negative Feedback Input Current	V_{NFB} = V_{NFR}	●	–37	–25		µA
NFB_{REG}	Negative Feedback Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 23V	●		0.002	0.05	%/V
g_m	Error Amplifier Transconductance	ΔI_C = ±50µA	 ●	1100 700	1500	1900 2300	µmho µmho
I_{ESK}	Error Amplifier Sink Current	V_{FB} = V_{REF} + 150mV, V_C = 0.9V, $V_{\overline{SHDN}}$ = 1V	●	120	200	350	µA
I_{ESRC}	Error Amplifier Source Current	V_{FB} = V_{REF} – 150mV, V_C = 0.9V, $V_{\overline{SHDN}}$ = 1V	●	120	200	350	µA
V_{CLH}	Error Amplifier Clamp Voltage	High Clamp, V_{FB} = 1V			1.33		V
V_{CLL}	Error Amplifier Clamp Voltage	Low Clamp, V_{FB} = 1.5V			0.1		V
A_V	Error Amplifier Voltage Gain			180	250		V/V

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_C = 0.9V, V_{FB} = V_{REF}. COL A, COL B, $\overline{SHDN}$, NFB, DUTY pins open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Sync							
f_{MAX}	Maximum Switch Frequency				250		kHz
f_{SYNC}	Synchronization Frequency Range	f_{OSC} = 250kHz				375	kHz
R_{SYNC}	SYNC Pin Input Resistance				40		kΩ
V_{FBfs}	FB Pin Threshold for Frequency Shift	5% Reduction from Nominal			0.4		V
Output Switches							
DC_{MAX}	Maximum Switch Duty Cycle	DUTY Pin Open, R_{VSL} = R_{CSL} = 4.9k, f_{OSC} = 25kHz DUTY Pin Grounded, Forced 50% Duty Cycle	●	44	45.5 50.0		% %
t_{IBL}	Switch Current Limit Blanking Time				200		ns
BV	Output Switch Breakdown Voltage	2.7V ≤ V_{IN} ≤ 23V	●	25	30		V
R_{ON}	Output Switch-On Resistance	$I_{COL\ A}$ or $I_{COL\ B}$ = 0.75A	●		0.5	0.85	Ω
$I_{LIM(MAX)}$	Switch Current Limit Duty Cycle = 30%			1			A
I_{LIMSC}	Switch Current Limit Duty Cycle = 80%			0.8			A
$\Delta I_{IN}/\Delta I_{SW}$	Supply Current Increase During Switch-On Time				16		mA/A
V_{DUTYTH}	DUTY Pin Threshold				0.35		
Slew Control							
V_{SLEWR}	Output Voltage Slew Rising Edge	Either A or B, R_{VSL}, R_{CSL} = 17k			11		V/µs
V_{SLEWF}	Output Voltage Slew Falling Edge	Either A or B, R_{VSL}, R_{CSL} = 17k			14.5		V/µs
I_{SLEWR}	Output Current Slew Rising Edge	Either A or B, R_{VSL}, R_{CSL} = 17k			1.3		A/µs
I_{SLEWF}	Output Current Slew Falling Edge	Either A or B, R_{VSL}, R_{CSL} = 17k			1.3		A/µs
Supply and Protection							
V_{IN}	Recommended Operating Range		●	2.7		23	V
$V_{IN(MIN)}$	Minimum Input Voltage		●		2.55	2.7	V
I_{VIN}	Supply Current	2.7V ≤ V_{IN} ≤ 23V, R_{VSL}, R_{CSL}, R_T = 17k	●		12	18	mA
$I_{VIN(OFF)}$	Shutdown Supply Current	2.7V ≤ V_{IN} ≤ 23V, $V_{\overline{SHDN}}$ = 0V	●		12	30	µA
$V_{\overline{SHDNL}}$	Shutdown Threshold	2.7V ≤ V_{IN} ≤ 23V	●	0.4	0.8	1.2	V
I_{SHDN}	Shutdown Input Current				–2		µA

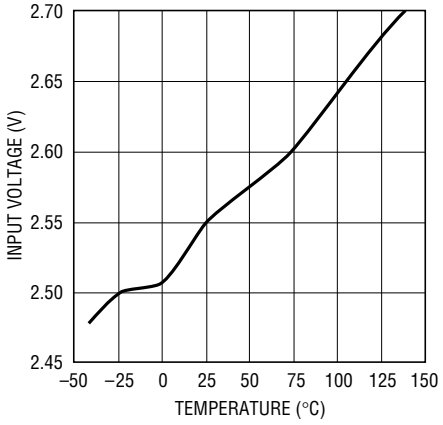
The ● denotes specifications that apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

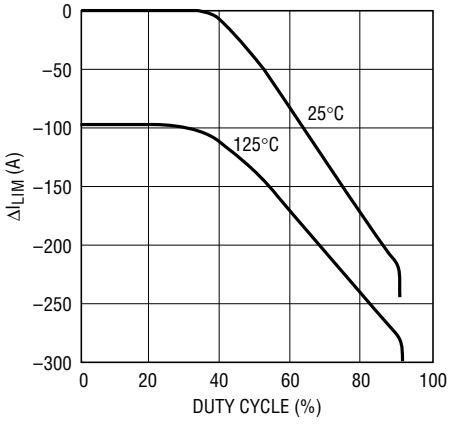
Note 2: The LT1533 is designed to operate over the junction temperature range of –40°C to 125°C, but is neither tested nor guaranteed beyond 0°C to 100°C.

TYPICAL PERFORMANCE CHARACTERISTICS

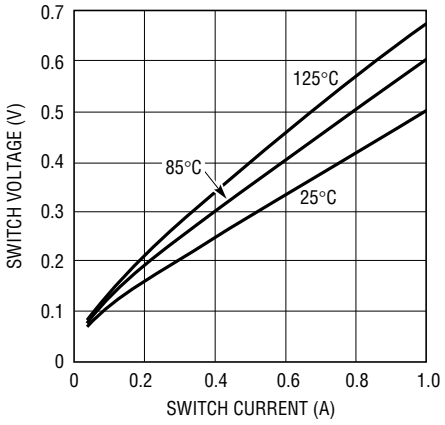
Minimum Input Voltage vs Temperature



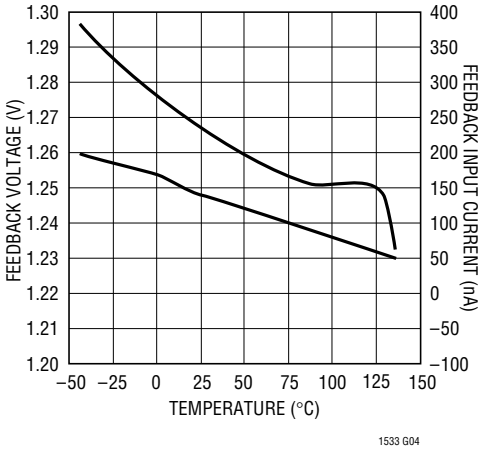
Change in I_{LIM} vs DC



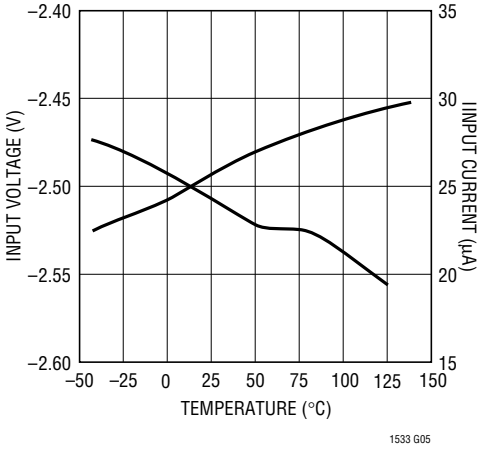
Switch Voltage Drop



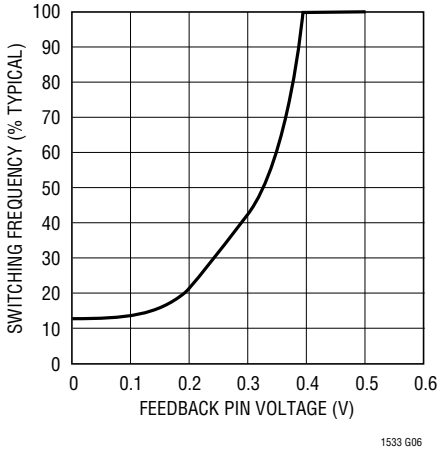
Feedback Voltage and Input Current



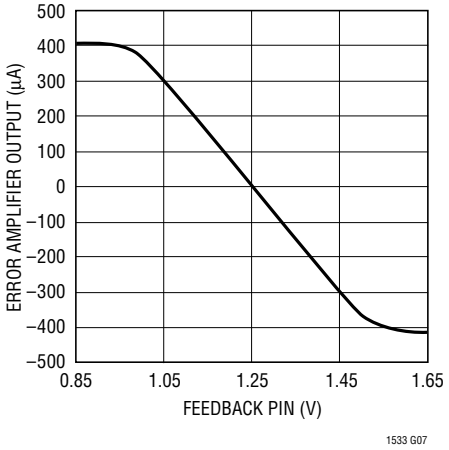
Negative Feedback Voltage and Input Current



Switching Frequency vs Feedback Pin Voltage



Error Amplifier Output Current



PIN FUNCTIONS

COL A, COL B (Pins 2, 15): These are the output collectors of the power switches. Their emitters return to PGND through a common sense resistor. COL A and COL B are alternately turned on out of phase. Large currents flow into these pins so it is desirable to keep external trace lengths short to minimize radiation. The collectors can be tied together for simple boost applications.

DUTY (Pin 3): Tying the DUTY pin to ground will force the outputs to switch with a 50% duty cycle. The DUTY pin must float if not used.

SYNC (Pin 4): The SYNC pin can be used to synchronize the oscillator to an external clock (see Oscillator Sync in Applications Information section for more details). The SYNC pin may either be floated or tied to ground if not used.

C_T (Pin 5): The oscillator capacitor pin is used in conjunction with R_T to set the oscillator frequency. For R_T = 16.9k,

$$C_{T(NF)} = 129/f_{OSC(kHz)}$$

R_T (Pin 6): The oscillator resistor pin is used to set the charge and discharge currents of the oscillator capacitor. The nominal value is 16.9k. It is possible to adjust this resistance ±25% to get a more accurate oscillator frequency.

FB (Pin 7): The feedback pin is used for positive voltage sensing and oscillator frequency shifting during start-up and short-circuit conditions. It is the inverting input to the error amplifier. The noninverting input of this amplifier connects internally to a 1.25V reference. This pin should be left open if not used.

NFB (Pin 8): The negative feedback pin is used for sensing a negative output voltage. The pin is connected to the inverting input of the negative feedback amplifier through a 100k source resistor. The negative feedback amplifier provides a gain of –0.5 to the feedback amplifier. This pin should be left open if not used.

GND (Pin 9): Signal Ground. The internal error amplifier, negative feedback amplifier, oscillator, slew control circuitry and the bandgap reference are referred to this ground. Keep the connection to the feedback divider and V_C compensation network free of large ground currents.

V_C (Pin 10): The compensation pin is used for frequency compensation and current limiting. It is the output of the error amplifier and the input of the current comparator. Loop frequency compensation can be performed with an RC network connected from the V_C pin to ground.

$\overline{SHDN}$ (Pin 11): The shutdown pin is used for disabling the switcher. Grounding this pin will disable all internal circuitry. Normally this output can be tied high (to V_{IN}) or may be left floating.

R_{CSL} (Pin 12): A resistor to ground sets the current slew rate for the collectors A and B. The minimum resistor value is 3.9k and the maximum value is 68k. Current slew will be approximately:

$$I_{SLEW(A/\mu s)} = 33/R_{CSL(k\Omega)}$$

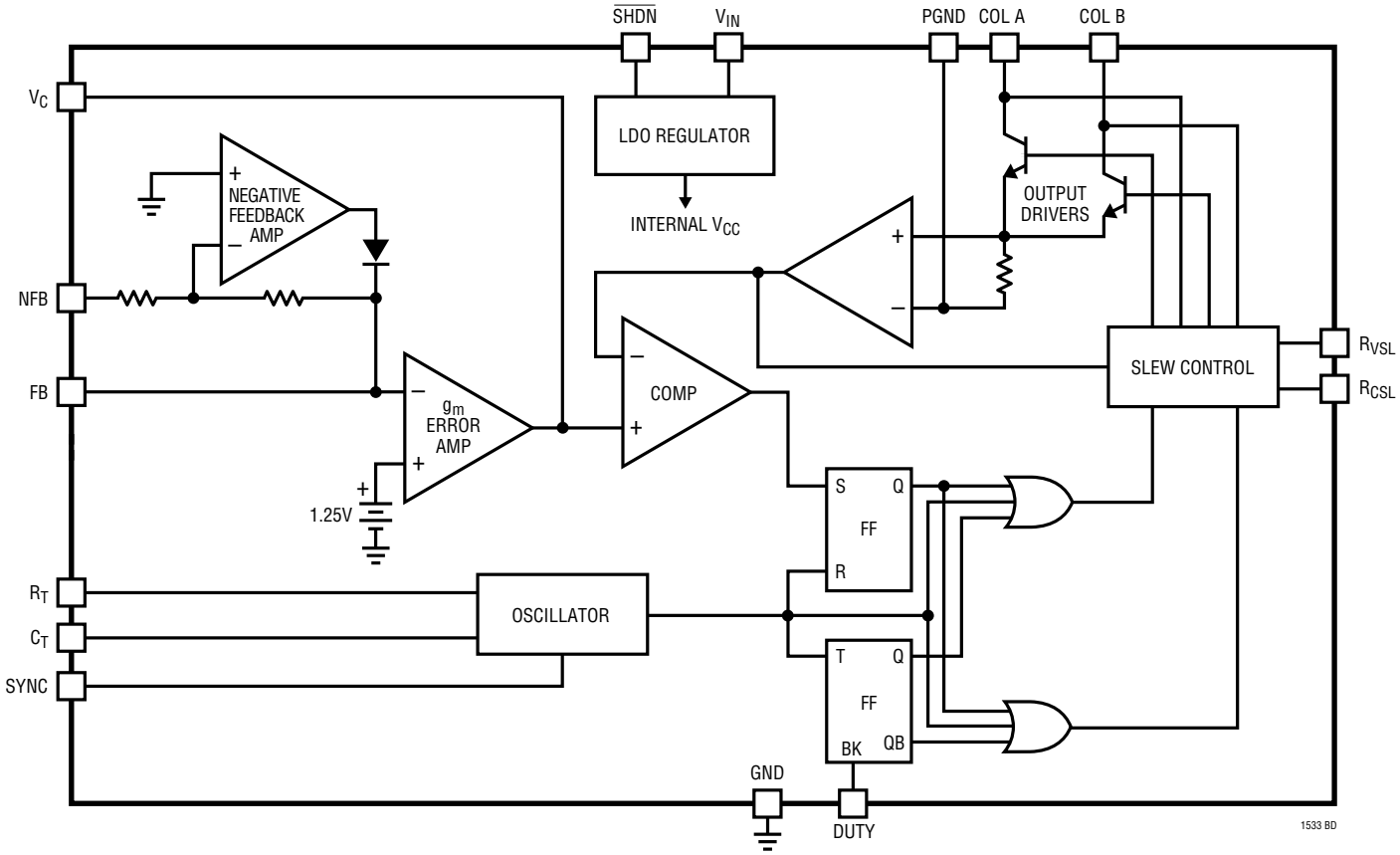
R_{VSL} (Pin 13): A resistor to ground sets the voltage slew rate for the collectors A and B. The minimum resistor value is 3.9k and the maximum value is 68k. Voltage slew will be approximately:

$$V_{SLEW(V/\mu s)} = 220/R_{VSL(k\Omega)}$$

V_{IN} (Pin 14): Input Supply Pin. Bypass this pin with a ≥ 4.7µF low ESR capacitor. When V_{IN} is below 2.55V the part will go into undervoltage lockout where it will stop output switching and pull the V_C pin low.

PGND (Pin 16): Power Switch Ground. This ground comes from the emitters of the power switches. In normal operation this pin should have approximately 25nH inductance to ground. This can be done by trace inductance (approximately 1") or with wire or a specific inductive component (e.g., small ferrite bead). This inductance ensures stability in the current slew control loop during turn-off. Too much inductance (>50nH) may produce oscillation on the output voltage slew edges.

BLOCK DIAGRAM



OPERATION

In noise sensitive applications, switching regulators tend to be ruled out as a power supply option due to their propensity for generating unwanted noise. When switching supplies are required due to efficiency or input/output voltage constraints, great pains must be taken to work around the noise generated by a typical supply. These steps may include precise synchronization of the power supply oscillator to an external clock, synchronizing the rest of the circuit to the power supply oscillator, or halting power supply switching during noise sensitive operations. The LT1533 greatly simplifies the task of eliminating supply noise by enabling the design of an inherently low noise switching regulator power supply.

The LT1533 is a fixed frequency, current mode switching regulator with unique circuitry to control the voltage and current slew rates of the output switches. Slew control capability provides much greater control over power supply components that can create conducted and radiated electromagnetic interference. The current mode control provides excellent AC and DC line regulation and simplifies loop compensation.

Current Mode Control

A switching cycle begins with an oscillator discharge pulse which resets the RS flip-flop, turning on one of the output drivers (refer to Block Diagram). The switch current is sensed across an internal resistor and the resulting voltage is amplified and compared to the output of the error amplifier (V_C pin). The driver is turned off once the output of the current sense amplifier exceeds the voltage on the V_C pin. The toggle flip-flop ensures that the two output drivers are enabled on alternate clock cycles. Internal slope compensation is provided to ensure stability under high duty cycle conditions.

OPERATION

Output regulation is obtained using the error amp to set the switch current trip point. The error amp is a transconductance amplifier that integrates the difference between the feedback output voltage and an internal 1.25V reference. The output of the error amp adjusts the switch current trip point to provide the required load current at the desired regulated output voltage. This method of controlling current rather than voltage provides faster input transient response, cycle by cycle current limiting for better output switch protection and greater ease in compensating the feedback loop.

The V_C pin serves three different purposes. It is used for loop compensation, current limit adjustment and soft starting. During normal operation the V_C voltage will be between 0.2V and 1.33V. An external clamp may be used for lowering the current limit. A capacitor coupled to an external clamp can be used for soft starting.

The negative feedback amplifier allows for direct regulation of negative output voltages. The voltage on the NFB pin gets amplified by a gain of –0.5 and driven onto the FB input, i.e., the NFB pin regulates to –2.5V while the amplifier output internally drives the FB pin to 1.25V as in normal operation. The negative feedback amplifier input impedance is 100k (typ) referred to ground.

Slew Control

Control of output voltage and current slew rates is done via two feedback loops. One loop controls the output switch collector voltage dV/dt and the other loop controls the emitter current dI/dt. Output slew control is achieved by comparing the currents generated by these two slewing events to currents created by external resistors R_{VSL} and R_{CSL}. The two control loops are combined internally to provide a smooth transition from current slew control to voltage slew control.

Internal Regulator

Most of the control circuitry operates from an internal 2.4V low dropout regulator that is powered from V_{IN}. The internal low dropout design allows V_{IN} to vary from 2.7V to 23V with virtually no change in device performance. When the part is put into shutdown, the internal regulator is turned off, leaving only a small (12μA typ) current drain from V_{IN}.

Protection Features

There are three modes of protection in the LT1533. The first is overcurrent limit. This is achieved via the clamping action of the V_C pin. The second is thermal shutdown that disables both output drivers and pulls the V_C pin low in the event of excessive chip temperature. The third is undervoltage lockout that also disables both outputs and pulls the V_C pin low whenever V_{IN} drops below 2.5V.

50% Duty Cycle Mode

Since the LT1533 has dual out-of-phase outputs, it is ideal for driving push-pull transformers. For simple DC transformer applications, the part can be forced into a 50% duty cycle mode using the DUTY pin. Grounding the DUTY pin will override the internal control circuitry and force the outputs to switch with a 50% duty cycle at one-half the oscillator frequency. Slew control also applies in the 50% duty cycle mode.

APPLICATIONS INFORMATION

Reducing EMI from switching power supplies has traditionally invoked fear in designers. Many switchers are designed solely on efficiency and as such produce waveforms filled with high frequency harmonics that then propagate through the rest of the power supply.

The LT1533 provides control over two of the more important variables for controlling EMI with switching inductive loads: switch voltage slew rate and switch current slew rate. The use of this part will reduce noise and EMI over conventional switch mode controllers. Because these variables are under control, a supply built with this part will exhibit far less tendency to create EMI and less chance of wandering into problems during production.

APPLICATIONS INFORMATION

It is beyond the scope of this data sheet to get into EMI fundamentals. However, following some basic guidelines will greatly mitigate EMI generation in switching regulator circuits.

1. Use switcher topologies that have better EMI characteristics. This will typically entail keeping current continuous and avoiding fast switch nodes. For instance, push-pull designs will tend to produce lower conducted emissions.
2. Discern whether conducted emissions or radiated emissions (or both) are the problem. Understanding this can help determine whether noise problems are magnetic or electrostatic.
3. Construct magnetics to lessen radiation; for instance, avoid open core magnetics. Magnetic components built on rods or barrels do not provide close magnetic return paths for flux and as such can induce problems on nearby sensitive circuits. Torroids and E cores are preferred embodiments.
4. Select capacitors for optimal ESR. Many problems are the result of voltage-induced transients in the ESR of the capacitors.
5. Use careful board layout. Trace-to-trace coupling of high current lines or capacitive coupling of lines with high dV/dt can be a problem. The area of current loops with high current components should also be minimized.

The following general example illustrates the benefits of slew control: the harmonics of a square wave will roll off from the fundamental at a 1/f rate. If the edges of the square wave are slew limited, an additional 1/f rolloff occurs at a frequency of $1/t_{SLEW}$, where t_{SLEW} is the transition time for the slew period. This is the basis for providing improved noise performance with the LT1533.

Oscillator Frequency

The oscillator determines the switching frequency and therefore the fundamental positioning of all harmonics. The use of good quality external components is important to ensure oscillator frequency stability. The oscillator is a sawtooth design. A current defined by external resistor R_T is used to charge and discharge the capacitor C_T. The discharge rate is approximately ten times the charge rate.

By allowing the user to have control over both components, trimming of oscillator frequency can be more easily achieved.

The external capacitance C_T is chosen by:

$$C_{T(nF)} = 2180/[f_{OSC(kHz)} \bullet R_{T(k\Omega)}]$$

where f_{OSC} is the desired oscillator frequency in kHz.

For R_T equal to 16.9k, this simplifies to:

$$C_{T(nF)} = 129/f_{OSC(kHz)}$$

A good quality low TC capacitor should be chosen.

Nominally R_T should be 16.9k. Since it sets up current, its temperature coefficient should be selected to compliment the capacitor. Ideally, both should have low temperature coefficients. It is possible to kit R_T and C_T for lower oscillator frequency production tolerance.

When the DUTY pin is high or floating, the outputs will be turned off during the discharge time of the oscillator. Due to slew rate control, turning off the outputs does not produce immediate transitions. Turn-off will require the current to ramp down and the switch voltage to ramp up. If the DUTY pin is grounded, then the outputs will turn on or off starting with the clock discharge.

If the FB pin is below 0.4V the oscillator discharge time will increase, causing the oscillation frequency to increase to approximately 6:1. This feature helps minimize power dissipation during start-up and short-circuit conditions.

Oscillator frequency is important for noise reduction in two ways: 1) the lower the oscillator frequency the lower the harmonics of waveforms are, making it easier to filter them, 2) the oscillator will control the placement of output frequency harmonics which can aid in specific problems where you might be trying to avoid a certain frequency bandwidth that is used for detection elsewhere.

Oscillator Sync

If a more precise frequency is desired (e.g., to accurately place harmonics) the oscillator can be synchronized to an external clock. Set the RC timing components for an oscillator frequency 10% lower than the desired sync frequency.

APPLICATIONS INFORMATION

Drive the SYNC pin with a square wave (with greater than 1.4V amplitude). The rising edge of the sync square wave will initiate clock discharge. The sync pulse should have a minimum of 0.5μs pulse width.

Be careful in sync'ing to frequencies much different from the part since the internal oscillator charge slope determines slope compensation. It would be possible to get into subharmonic oscillation if the sync doesn't allow for the charge cycle of the capacitor to initiate slope compensation. In general, this will not be a problem until the sync frequency is greater than 1.5 times the oscillator free-run frequency.

Slew Rate Setting

Setting the voltage and current slew rates is easy. External resistors to ground on the R_{VSL} and R_{CSL} pins determine the slew rates. Determining what slew rate to use is more difficult. There are several ways to approach the problem.

First start by putting a 50k resistor pot with a 3.9k series resistance on each pin. In general, the next step will be to monitor the noise that you are concerned with. Be careful in measurement technique. Keep probe ground leads very short.

Usually it will be desirable to keep the voltage and current slew resistors approximately the same. There are circumstances where a better optimization can be found by adjusting each separately, but as these values are separated further, a loss of independence of control will occur.

Starting from the lowest resistor setting adjust the pots until the noise level meets your guidelines. Note that slower slewing waveforms will dissipate more power so that efficiency will drop. You can also monitor this as you make your slew adjustment.

It is possible to use a single slew setting resistor. In this case the R_{VSL} and R_{CSL} pins are tied together. A resistor with a value of 2k to 34k (one half the individual resistors) can then be tied from these pins to ground.

Emitter Inductance

A small inductance in the power ground minimizes a potential dip in the output current falling edge that can occur under fast slewing, 25nH is usually sufficient. Greater than 50nH may produce unwanted oscillations in the voltage output. The inductance can be created by wire or board trace with the equivalent of one inch of straight length. A spiral board trace will require less length.

Positive Output Voltage Setting

Sensing of a positive output voltage is usually done using a resistor divider from the output to the FB pin. The positive input to the error amp is connected internally to a 1.25V bandgap reference. The FB pin will regulate to this voltage.

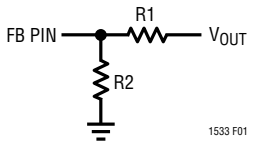


Figure 1

Referring to Figure 1, R1 is determined by:

$$R1 = R2\left(\frac{V_{OUT}}{1.25} - 1\right)$$

The FB bias current represents a small error and can usually be ignored for values of R1|| R2 up to 10k.

One word of caution. Sometimes a feedback zero is added to the control loop by placing a capacitor across R1 above. If the feedback zero capacitively pulls the FB pin above the internal regulator voltage (2.4V typ), output regulation may be disrupted. A series resistance with the feedback pin can eliminate this potential problem.

Negative Output Voltage Setting

Negative output voltage can be sensed using the NFB pin. In this case regulation will occur when the NFB pin is at –2.5V. The input bias current for the NFB is –25μA (I_{NFB}) which needs to be accounted for in setting up the divider.

Referring to Figure 2, R1 is chosen such that:

$$R1 = R2\left(\frac{\left|V_{OUT}\right| - 2.5}{2.5 + R2 \bullet 25\mu A}\right)$$

APPLICATIONS INFORMATION

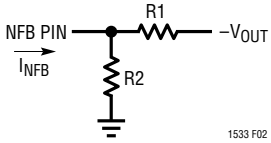


Figure 2

A suggested value for R2 is 2.5k. The NFB pin is normally left open if the FB pin is being used.

Dual Polarity Output Voltage Sensing

Certain applications may benefit from sensing both positive and negative output voltages. When doing this each output voltage resistor divider is individually set as previously described. When both FB and NFB pins are used, the LT1533 will act to prevent either output from going beyond its set output voltage. The lowest output (heaviest load) will dominate control of the regulator. This technique would prevent either output from going unregulated high at no load. However, this technique will also compromise output load regulation.

Shutdown

If the shutdown pin is pulled low, the regulator will turn off. The supply current will be reduced to less than 20µA.

Thermal Considerations

Computing power dissipation for this IC requires careful attention to detail. Reduced output slewing causes the part to dissipate more power than would occur with fast edges. However, much improvement in noise can be produced with modest decrease in supply efficiency.

Power dissipation is a function of topology, input voltage, switch current and slew rates. It is impractical to come up with an all-encompassing formula. It is therefore recommended that package temperature be measured in each application. The part has an internal thermal shutdown to prevent device destruction, but this should not replace careful thermal design.

1. Dissipation due to input current:

$$P_{VIN} = V_{IN}\left(11mA + \frac{I}{60}\right)$$

where I is the average switch current.

2. Dissipation due to the drivers saturation:

$P_{VSAT} = (V_{SAT})(I)(DC_{MAX})$

where V_{SAT} is the output saturation voltage which is approximately 0.1 + (0.4)(I), DC_{MAX} is the maximum duty cycle.

3. Dissipation due to output slew using approximations for slew rates:

$$P_{SLEW} = \left(\frac{(V_{IN})\left(I^2 + \frac{\Delta I^2}{4}\right)}{(33)(10^9)}(R_{CSL}) + \frac{(I)\left(V_{IN}^{\,2} - \frac{V_{SAT}^{\,2}}{4}\right)}{(220)(10^9)}(R_{VSL}) \right)(f_{OSC})$$

Note if V_{SAT} and ΔI are small with respect to V_{IN} and I, then:

$$P_{SLEW} = \left(\frac{(I)(R_{CSL})}{(33)(10^9)} + \frac{(V_{IN})(R_{VSL})}{(220)(10^9)} \right)(f_{OSC})(V_{IN})(I)$$

where ΔI is the ripple current in the switch, R_{CSL} and R_{VSL} are the slew resistors and f_{OSC} is the oscillator frequency.

Power dissipation P_D is the sum of these three terms. Die junction temperature is then computed as:

$T_J = T_{AMB} + (P_D)(\theta_{JA})$

where T_{AMB} is ambient temperature and θ_{JA} is the package thermal resistance. For the 16-pin SO θ_{JA} is 100°C/W.

For example, with f_{OSC} = 40kHz, 0.4A average current and 0.1A of ripple, the maximum duty cycle is 90%. Assume slew resistors are both 17k and V_{SAT} is 0.26V, then:

P_D = 0.176W + 0.094W + 0.158W = 0.429W

In an S16 package the die junction temperature would be 43°C above ambient.

APPLICATIONS INFORMATION

Frequency Compensation

Loop frequency compensation is accomplished by way of a series RC network on the output of the error amplifier (V_C pin). Referring to Figure 3, the main pole is formed by capacitor C_{VC} and the output impedance of the error amplifier (approximately 400kΩ). The series resistor R_{VC} creates a "zero" which improves loop stability and transient response. A second capacitor C_{VC2}, typically one-tenth the size of the main compensation capacitor, is sometimes used to reduce the switching frequency ripple on the V_C pin. V_C pin ripple is caused by output voltage ripple attenuated by the output divider and multiplied by the error amplifier. With the second capacitor, V_C pin ripple is:

$$V_{CPIN\ RIPPLE} = \frac{(1.25)(V_{RIPPLE})(g_m)(R_{VC})}{V_{OUT}}$$

where V_{RIPPLE} = Output ripple (V_{P-P})
g_m = Error amplifier transconductance
R_C = Series resistor on V_C pin
V_{OUT} = DC output voltage

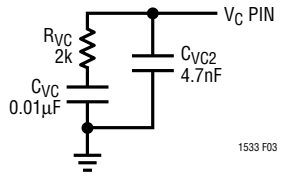


Figure 3

To prevent irregular switching, V_C pin ripple should be kept below $50mV_{P-P}$. Worst-case V_C pin ripple occurs at maximum output load current and will also be increased if poor quality (high ESR) output capacitors are used. The addition of a 0.0047µF capacitor on the V_C pin reduces switching frequency ripple to only a few millivolts. A low value for R_C will also reduce V_C pin ripple, but loop phase margin may be inadequate.

Magnetics

Design of magnetics is again dependent on topology. For a push-pull converter the transformer stores little energy. As such its design is based on being able to supply the voltage and current and ensure that saturation doesn't occur.

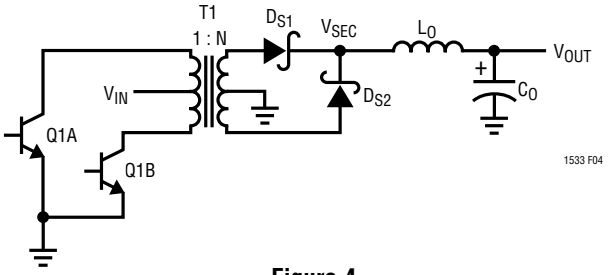


Figure 4

For the configuration of Figure 4 the following design equations apply:

N is determined by volt-sec balance in the transformer.

$$N = \frac{V_{OUT} + V_F}{DC_{MAX}\left(V_{IN(MIN)} - V_{SAT}\right)}$$

where $V_{IN(MIN)}$ is the minimum input voltage, DC_{MAX} is the maximum duty cycle, V_F is the diode forward drop and V_{SAT} is the driver on voltage.

L_O is determined by desired ripple current and oscillator frequency:

$$L_O = \frac{(V_{OUT} + V_F)(1 - DC_{MIN})}{(I_{RIPPLE})(f_{OSC})}$$

where DC_{MIN} is the duty cycle at maximum input, I_{RIPPLE} is the desired ripple current and f_{OSC} is the oscillator frequency. As an example, a 5V ±10% to 12V, 150kHz converter with 200mA output and 40mA ripple will require:

$$N = \frac{12 + 0.4}{90\%(4.5 - 0.5)} = 3.5,$$

$$L_O = \frac{(12 + 0.4)(1 - 71\%)}{(40mA)(150k)} = 600\mu H$$

APPLICATIONS INFORMATION

The transformer needs to be designed such that the primary inductance is five to ten times greater than the reflected L_O inductance (L_O/N^2) which is 49µH in this case. The transformer must also have a volt-sec rating greater than:

$$\frac{V_{IN} - V_{SAT}}{f_{OSC}}\left(DC_{MAX}\right)$$

which would be 24V-µs in this case.

Capacitors

Correct choice of input and output capacitors can be very important to low noise switcher performance. Push-pull topologies and other low noise topologies will in general have continuous currents which reduce the requirements for capacitance. However, noise depends more on the ESR of the capacitors.

Input capacitors must also withstand surges that occur during the switching of some types of loads. Some solid tantulum capacitors can fail under these surge conditions.

Design Note 95 offers more information but the following is a brief summary of capacitor types and attributes.

Aluminum Electrolytic: Low cost but rarely used above 100kHz.

Solid Tantalum: Small size and low impedance. Typically available for voltages below 50V. Possible problem with surge currents (AVX TPS line addresses this issue).

OS-CON: Lower impedance than aluminum but only available for 25V or less. Form factor may be a problem. Sometimes their very low ESR can cause loop stability problems.

Ceramic: Generally used for high frequency and high voltage bypass. They too can have such a low ESR as to cause loop stability problems. Often they can resonate with their ESL before ESR becomes effective.

A high frequencies most capacitors have inductive impedance that can be reduced by paralleling capacitors.

Input Capacitor

The input capacitor is an important component in the design of a low noise switcher. The ESR of this capacitor acts with high frequency current components to produce much of the conducted noise of the switcher.

It is possible that the input capacitor will see a large surge current when certain loads are connected (for instance, batteries or large capacitors). Solid tantalum capacitors can fail under these conditions. Value of 1µF to 22µF are recommended with ESR under 0.3Ω.

Output Filter Capacitor

Output capacitors are usually chosen on the basis of ESR since this will determine output ripple. Typical required ESR will be in the 0.05Ω to 0.5Ω range.

The specific value for capacitance will depend on topology. A typical output capacitor is an AVX type TPS, 22µF and 25V with a guaranteed ESR less than 0.2Ω. To further reduce ESR, multiple output capacitors can be used in parallel. The value in microfarads is not particularly important. A small 22µF trantalum capacitor will have high ESR and higher output voltage ripple. Table 1 shows some typical solid tantalum surface mount capacitors.

Table 1

SIZE	CAPACITOR	ESR (MAX Ω)
E CASE	AVX TPS, Sprague 593D	0.1 to 0.3
	AVX TAJ	0.7 to 0.9
D CASE	AVX TPS, Sprague 593D	0.1 to 0.3
	AVX TAJ	0.9 to 2.0
C CASE	AVX TPS	0.2 (Typ)
	AVX TAJ	1.8 to 3.0
B CASE	AVX TAJ	2.5 to 10

Switching Diodes

In general, switching diodes should be Schottky diodes such as 1N5818 or MBR130 (1A/30V). Low output current applications may use 1N4148 switching diodes.

APPLICATIONS INFORMATION

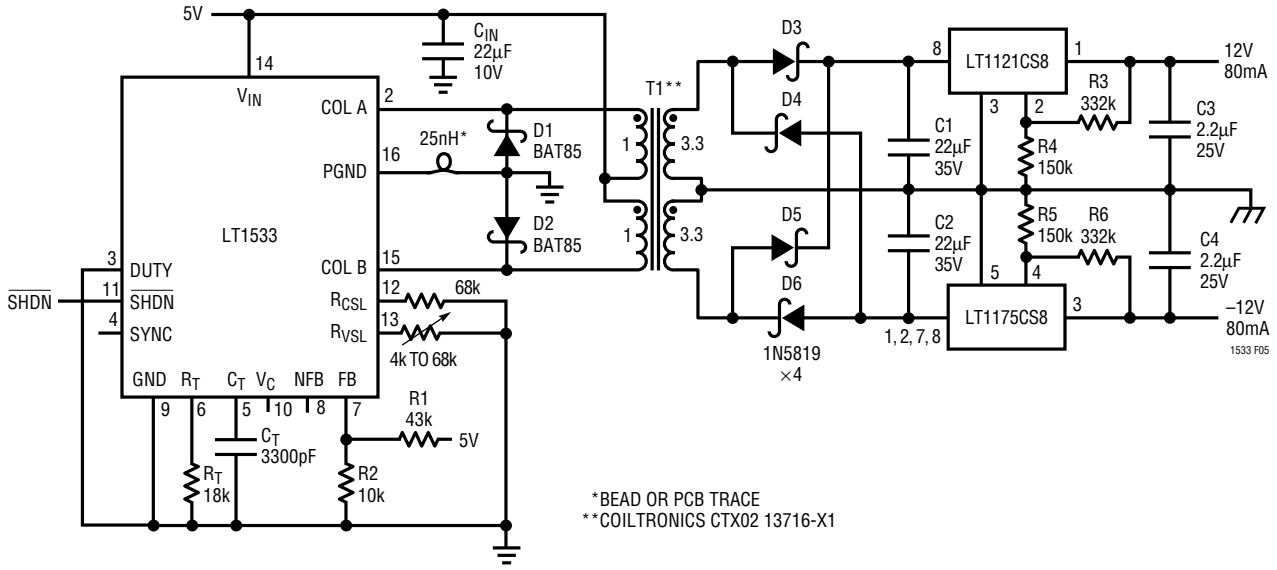


Figure 5. 5V to ±12V DC Transformer

Unregulated Applications

The LT1533 can be used to create a low noise "DC transformer" unregulated power supply. DC transformers are open-loop switching regulators where the output voltage is controlled by the turns ratio of the transformer. A DC transformer provides a low cost isolated supply.

For such applications, the DUTY pin of the LT1533 should be grounded. This will force the outputs into a 50% on, 50% off mode. Note that because of slew control there will be some variance from 50%. Figure 5 shows a 5V to ±15V DC transformer.

One concern with this type of application is having both switch outputs transition at the same time. This can cause both primary side windings to have positive EMF added to the winding, causing the current to run away. Since this part controls slew rate this won't happen. It is possible to see slightly increased total current draw when both drivers are on, but this will be controlled and observable. Since the outputs share a common sense resistor, the outputs will turn off when the total current in both exceeds the limit set by the V_C pin.

The FB pin should be DC biased between 0.7V and 1.2V to prevent frequency shifting from occuring. This also ensures that the V_C pin is set to its upper clamp, providing peak output current.

The slew rate adjustment should be made by putting a 3.9k resistor in series with a 50k pot on the R_{VSL} and R_{CSL} pins (or a 2k resistor in series with a 25k pot with both pins tied together). Monitor output noise or other system signal while increasing the resistance until desired noise performance is reached. System efficiency can also be monitored.

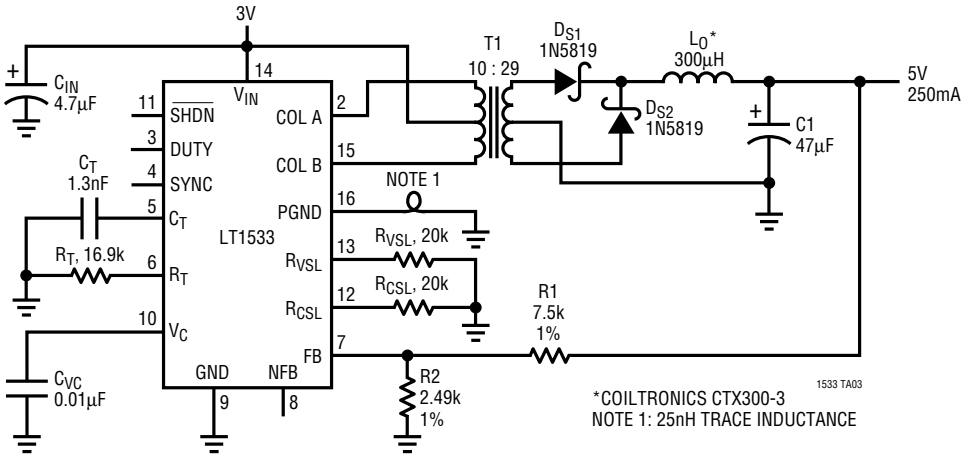
While this topology is not as quiet as a push-pull converter, it can provide a low cost, isolated power supply that has decreased noise relative to other solutions.

More Help

Our Application Department is always ready to lend a helping hand.

TYPICAL APPLICATION

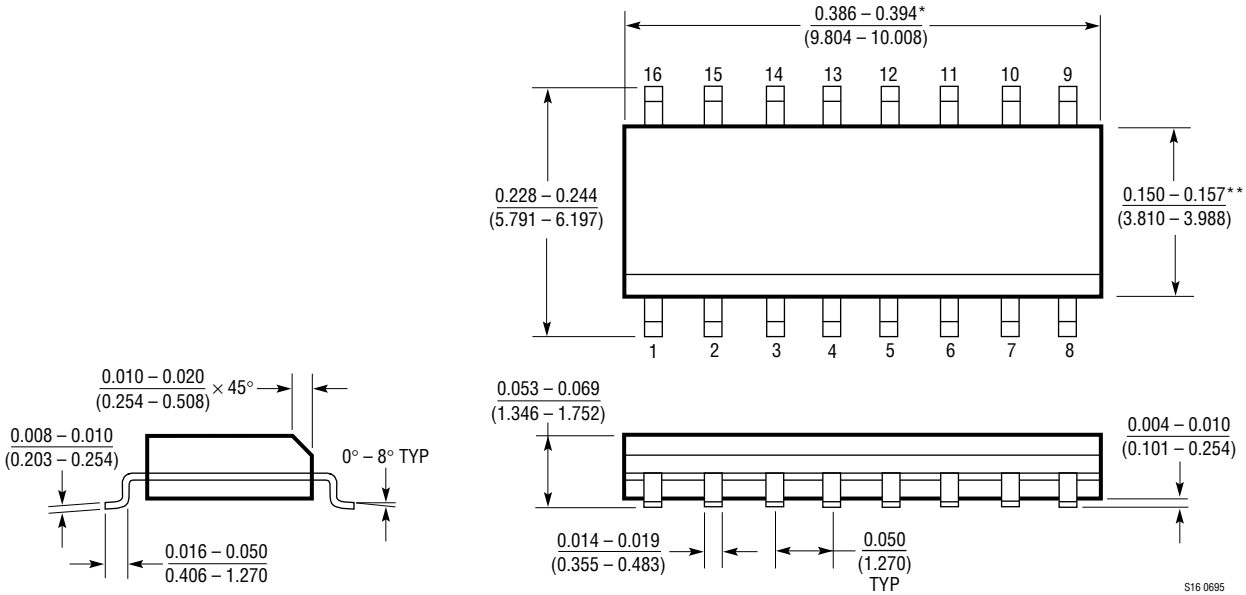
3V to 5V Forward Push-Pull DC/DC Converter



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1129	700mA Micropower Low Dropout Regulator	0.4V Dropout Voltage, Reverse Battery Protection
LT1175	500mA Negative Low Dropout Micropower Regulator	Positive or Negative Shutdown Logic
LT1377	1MHz High Efficiency 1.5A Switching Regulator	High Frequency, Small Inductor
LT1425	Isolated Flyback Switching Regulator	Excellent Regulation Without Transformer “Third Winding”
LTC®1436	High Efficiency Synchronous Switching Regulator	Adaptive Power™ Mode, Phase Locked Loop

Adaptive Power is a trademark of Linear Technology Corporation.

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