

MAXIM

MAX3680 Evaluation Kit

Evaluates: MAX3680

General Description

The MAX3680 evaluation kit (EV kit) simplifies evaluation of the MAX3680 622Mbps, SDH/SONET 1:8 deserializer. The EV kit requires only a +3.3V supply, and includes all the external components necessary to interface with 3.3V PECL/TTL logic. The board can be connected directly to the output of a clock-and-data-recovery circuit (such as the MAX3675) and to the TTL input of an overhead termination circuit. It can also be used with a signal generator and an oscilloscope to evaluate the MAX3680's basic functionality.

Component List

DESIGNATION	QTY	DESCRIPTION
C1-C4	4	0.1 μ F ceramic capacitors
C5	1	33 μ F, 10V tantalum capacitor AVX TAJC336K010 or Sprague 293D336X0010C2
C6	1	2.2 μ F tantalum capacitor AVX TAJA225K010 or Sprague 293D225X0010A2
C7-C12	6	100pF ceramic capacitors
J3-J16	14	SMA connectors (PC edge mount)
L1	1	56nH inductor Coilcraft 0805CS-560-XKBC
R1, R3, R5, R7	4	82 Ω , 5% resistors
R2, R4, R6, R8	4	130 Ω , 5% resistors
R9-R17	9	2.4k Ω , 5% resistors
+3.3V, GND JR9-JR17	11	2-pin headers
U1	1	MAX3680EAI
None	1	MAX3680 data sheet

Component Suppliers

SUPPLIER	PHONE	FAX
AVX	(803) 946-0690	(803) 626-3123
Coilcraft	(847) 639-6400	(847) 639-1469
Sprague	(603) 224-1961	(603) 224-1430

Please indicate that you are using the MAX3680 when contacting the above component suppliers.

Features

- ◆ **Single +3.3V Supply**
- ◆ **Inputs Terminated for Interfacing with 3.3V PECL**
- ◆ **Outputs Configured for 50 Ω or High-Impedance Interface**
- ◆ **Fully Assembled and Tested**

Ordering Information

PART	TEMP. RANGE	BOARD TYPE
MAX3680EVKIT-SO	-40°C to +85°C	Surface Mount

Detailed Description

The MAX3680 EV kit simplifies evaluation of the MAX3680 622Mbps, SDH/SONET 1:8 deserializer. The EV kit operates from a single +3.3V supply and includes all the external components necessary to interface with 3.3V PECL/TTL logic.

Each PECL input (SCLK+, SCLK-, SD+, SD-) is terminated on the EV board with the Thevenin equivalent of 50 Ω to (V_{CC} - 2V). These inputs can be driven directly by any 3.3V PECL device's output, such as a clock-and-data-recovery circuit (e.g., the MAX3675). The synchronization input (SYNC) is a TTL input.

The TTL outputs (PCLK, PD_) can interface to either 50 Ω or high-impedance inputs. To interface to 50 Ω inputs, connect the inputs directly to the SMA connectors labeled PCLK and PD0-PD7. This configuration forms a 50-to-1 voltage divider that maintains a high-impedance load to each TTL output while interfacing to 50 Ω . To interface to high-impedance inputs, connect the inputs to the 2-pin headers at R9-R17, which provide direct connections to the TTL outputs.

Layout Considerations

To minimize propagation-delay skew, all PECL input signal lines are 50 Ω transmission lines of equal length. To allow accurate characterization of the parallel-clock to data-output delay, the output data lines (prior to the series 2.4k Ω termination resistors) are matched and kept as short as possible. Excluding the series termination resistor, each output data line measures approximately 3pF at the 2-pin header (JR9-JR17).



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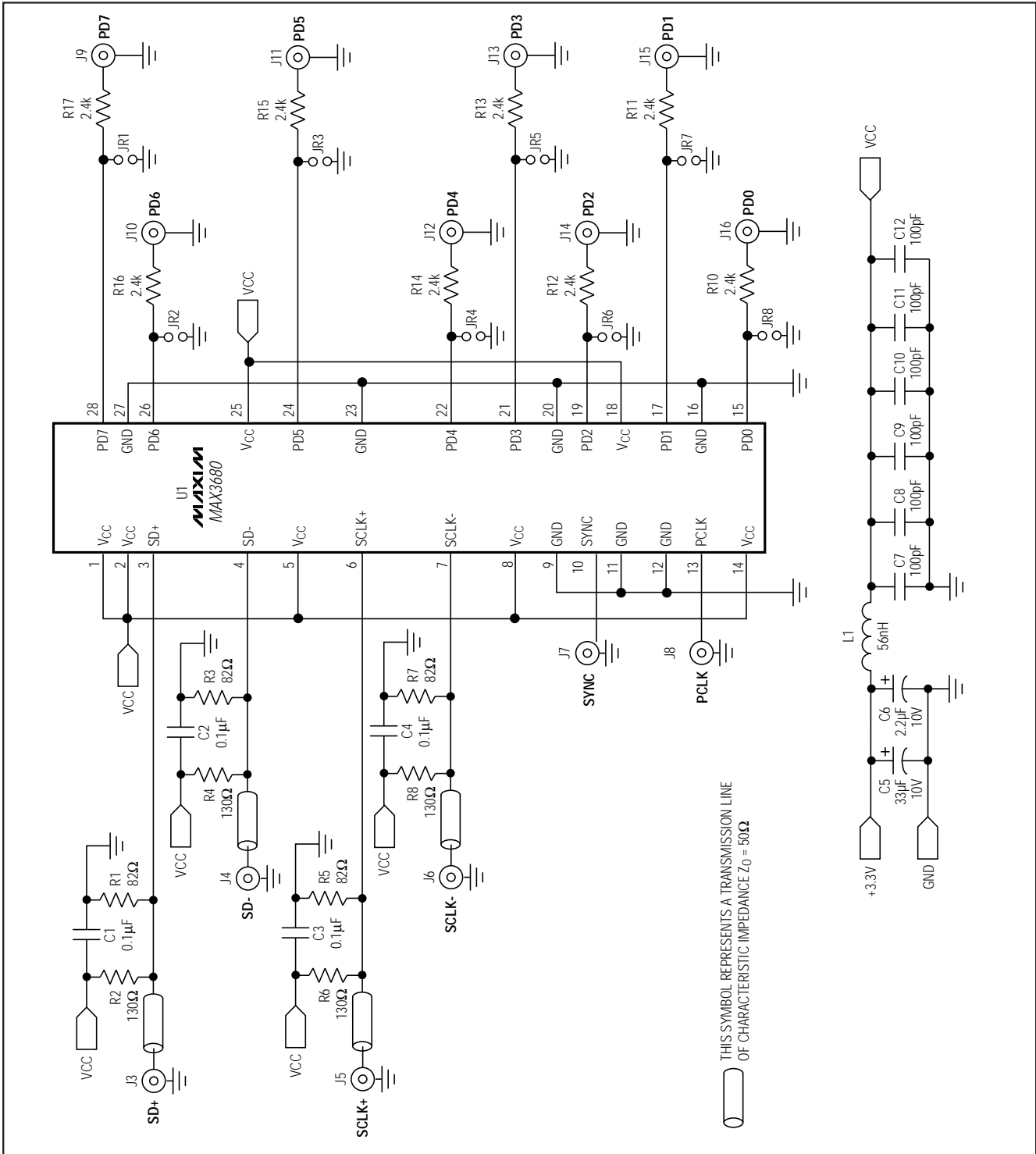


Figure 1. MAX3680 EV Kit Schematic

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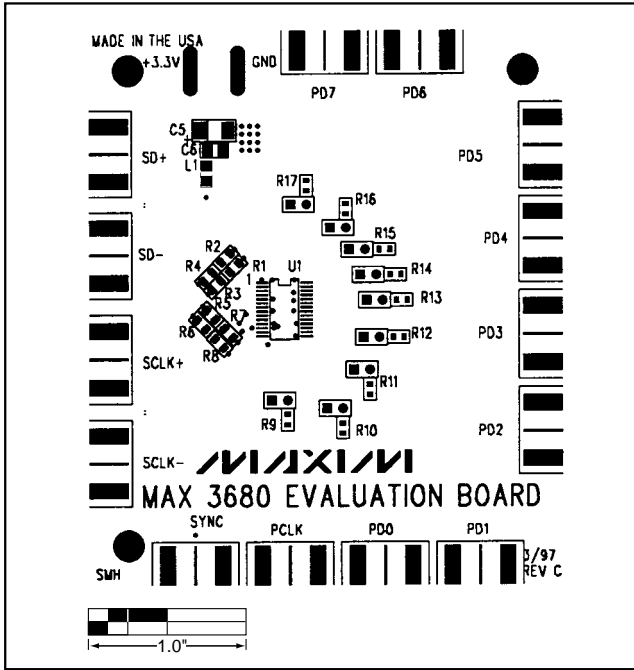


Figure 2. MAX3680 EV Kit Component Placement Guide

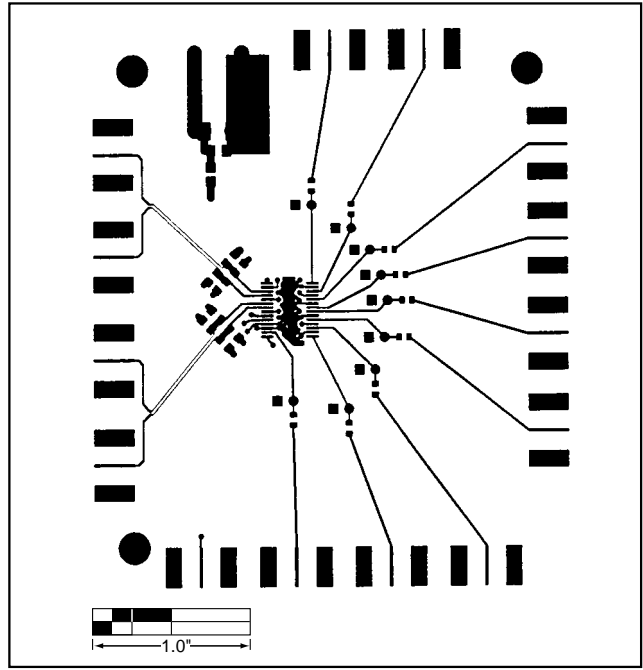


Figure 3. MAX3680 EV Kit PC Board Layout—Component Side*

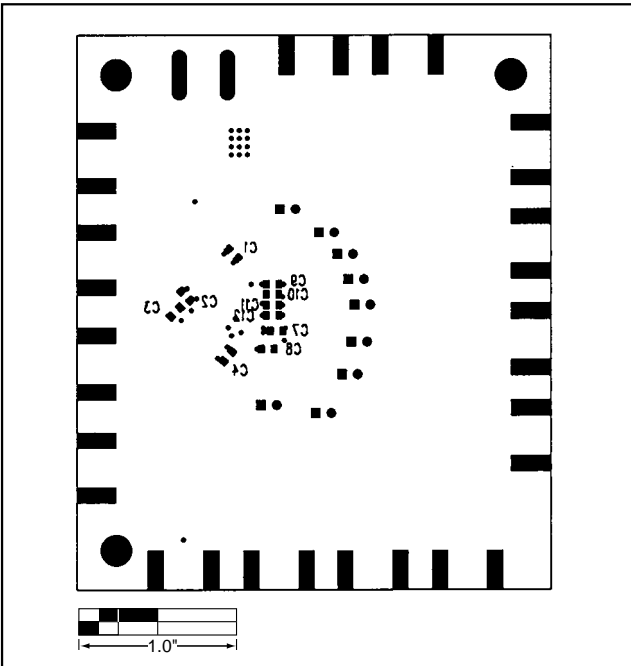


Figure 4. MAX3680 EV Kit PC Board Layout—Bottom Silkscreen*

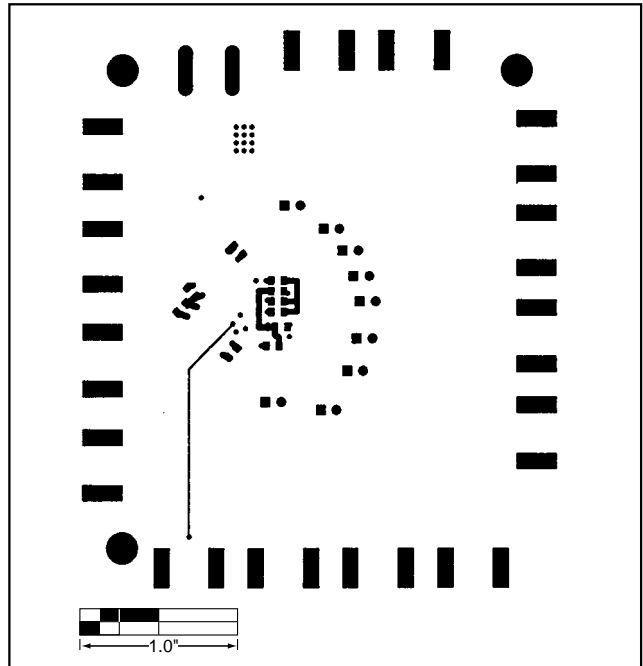


Figure 5. MAX3680 EV Kit PC Board Layout—Solder Side*

*Not to scale

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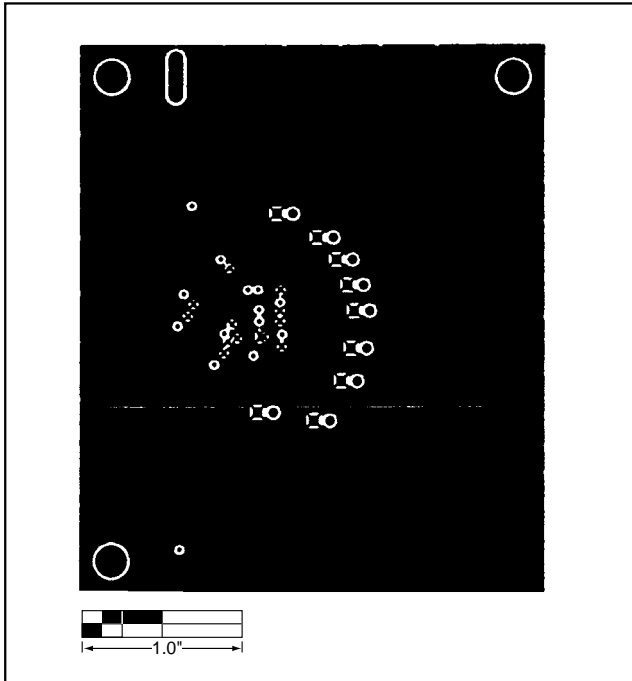


Figure 6. MAX3680 EV Kit PC Board Layout—GND Plane*

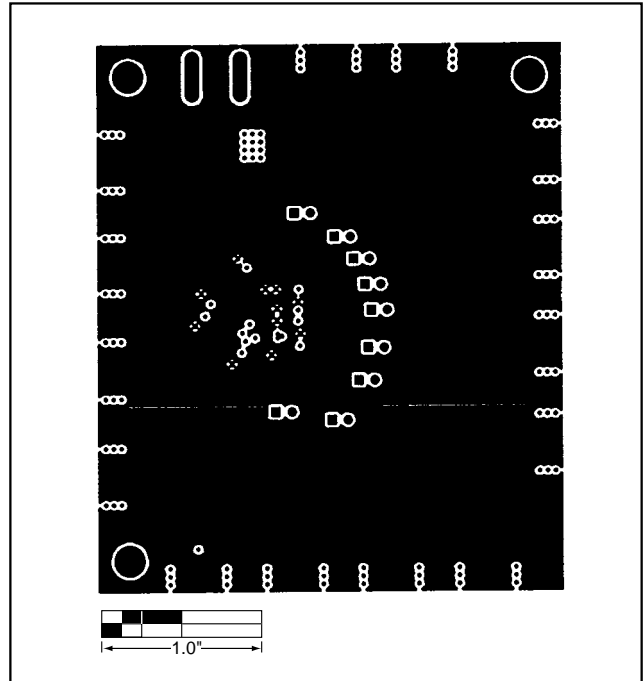


Figure 7. MAX3680 EV Kit PC Board Layout— Power Plane*

*Not to scale

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