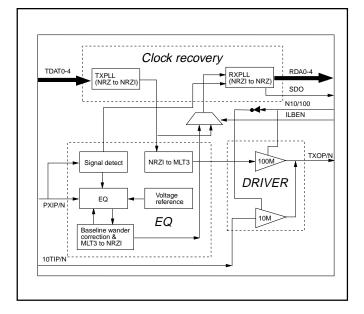## 100 BASE-TX PHY-PMD TRANSCEIVER

1. FEATURES

- Complies with IEEE 802.3 Standards
- Integral 10 Mb/s Buffer for Dual 10 Mb/s&100 Mb/s Applications
- Baseline Wander correction
- Adapative Equalization
- 25 MHz to 125 MHz Transmit Clock Multiplier

- Five Bit TTL Nibble at 25 MHz Input/Output
- 25 MHz received recovery clock
- Operates over 100 Meters of STP and Category 5 UTP Cable (>7.5 dB)
- Single +5V Supply
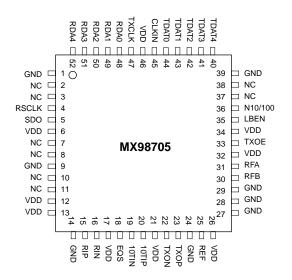- 52 PQFP package

2. GENERAL DISCRIPTION

The MX98705 is a fully intergrated physical layer device supporting 100Base-TX or FDDI over copper applications. The MX98705 integrates 125 MHz clock recovery/generation, receive adaptive equalization, and baseline wander correction, it provides 5-bit parallel interface to any MAC controller.

The MX98705 receive section includes an adaptive equalizer with DC baseline wander compensation, MLT-3 to NRZ decoder, and a 125 MHz receive clock recovery circuit. The transmit section provide NRZ to MLT-3 for 100Base-TX and a buffer for 10 Mb/s application.

3. BLOCK DIAGRAM

4. PIN CONFIGURATION

5. PIN DESCRIPTION

PIN	PIN NAME	TYPE	DESCRIPTION
1	GND	-	Ground for PADs
2, 3	NC	O	No connection
4	RSCLK	TTLO	25MHZ recovered receive clock
5	SDO	TTLO	Signal detect output. Being high after RXH/RXL inputs is available (>40ms)
6	VDD	-	VDD for PLL digital circuits
7, 8	NC	O	No connection
9	GND	-	Ground for receive PLL
10	NC	I	No connection
11	NC	O	No connection
12	VDD	-	VDD for receive PLL
13	VDD	-	VDD for EQ circuit
14	GND	-	Ground for EQ circuit
15, 16	RIP	I	Differential receive signal input form magnetics
17	RIN	-	VDD for EQ circuit
18	EQS	I	3 level mode select for equaliser, high=min, open=auto, low=full
19, 20	10TIN 10TIP	I	Differential 10 base T input. This signal is output on the TXON & TXOP when N10/100 is held low
21	VDD	-	VDD for output line Driver
22, 23	TXON	O	Differential line driver outputs to drive magnetics
24	TXOP	-	Ground for output line Driver
25	TXREF	I	Line driver current reference set-up pin. By connecting 500Ω resistor to GND is recommended.
26	VDD	-	VDD for PHY bias circuit
27	GND	-	Ground for chip substrate GND connectionn
28	GND	-	Ground for EQ circuit
29	GND	-	Ground for Transmit PLL
30	RFB	-	Internal Ground reference. NC or Connect to GND
31	RFA	I	Internal feedback reference current generation point. By connecting 1.4KΩ resistor to GND or RFB
32	VDD	-	VDD for Transimit PLL
33	TXOE	I	Output Enable. Tri -state TX drivers when TXOE is low.
34	VDD	-	VDD for PHY WELL contact
35	LBEN	TTLI	Loopback enable input. High is loopback mode, low is normal mode
36	N10/100	TTLI	10/100M driver selection. High is 100M, low is 10M driver
37, 38	NC	O	No connection
39	GND	-	Ground for PADs
40-44	TDAT4-0	TTLI	Parallel input to transmit channel
45	CLKIN	TTLI	25 MHz reference clock to PLLs
46	VDD	-	VDD for PADs
47	TCLK	TTLO	25 MHz transmit reference clock from transmit PLL
48-52	RDA0-4	TTLO	5-bit parallel received data

6. FUNCTIONAL DESCRIPTION

The functional blocks of the device are shown in Fig.1 These are described below:

6.1 Transmit Section

6.1.1 Transmit 125 MHz Phase Lock Loop (PLL)
This circuit consist of a VCO with 125MHz central frequency and built-in loop filter. The 125 Mhz is divided by 5 to generate a 25 Mhz output clock which is phase compared with a 25 MHz crystal reference clock which is an input through pin CLKIN. This 25 MHz clock is then sent to the PCS layer to pace in the 5 bit nibble data. Due to built-in filter, no extra filter components are needed which simply the system design.

6.1.2 Five Bit Nibble or 125 MHz Shifter
Data is input to the transmit side in 5-bit form on pins TDAT0-4. This NRZ data is clocked in on the posotive edge of the 25 MHz clock through TXCLK pin. The parallel data is first loaded into a 5 bit wide register prior to being loaded into a 5 bit PISO where it is converted into a serial data stream. The last stage of the shifter is a converter to change the data from NRZ to NRZI.

6.1.3 NRZI to MLT3 Encoder
The serial data from the shifter then passes through an encoder which converts the NRZI binary data into the three level MLT-3 format for transmission by the "TXO" outputs.

6.1.4 Transmit Line Driver
Both of the 10Mb/s and 100Mb/s line driver share the same output pins TXOP and TXON. The N10/100 pin is used to control which driver is active and allowed to driver the line. When N10/100 is held high the MLT-3 data is output by the 100Mb/s driver. This driver is designed to drive a nominal output impedance of 50Ω. Output current is set by the value of an external resistor (Rext) from pin "REF" to GND.

Final output current at the "TXO" output is a multiple of this current and is defined as:

$$I_{TXO}(mA)=23/R_{EXT}(k\Omega)$$

Transition times of the "TXO" outputs are matched and internally limited to approx. 3.0ns to reduce EMI emissions.

When N10/100 is held low, the 10Mb/s driver is selected. This 10Mb/s driver consists of a differential analog buffer designed to take a fully cable conditioned 10Mb/s signal from the filter output of existing 10BaseT electronics. The 10BaseT signal is input on pins 10TIP/N. The output current of the buffer is determined by the same external R_{EXT} as 100Mb/s driver.

The unselected driver is switched to a tristated mode for saving power. In additional, when TXOE pin is held low, both 10Mb/s and 100Mb/s drivers are tri-stated regardless of the mode selected by N10/100 pin.

When operating in single 100Mb/s applications a 1:1 turn ratio magnetics is recommand, therefore, to attain the desired line driving current of 40mA out of the secondary a TXO output driver of 40mA is required. Using the above formula it will be found that 560Ω is the nearest prefered value to that required to give the 40mA.

6.2 Receiver Section

6.2.1 Equalizer
The equalizer circuit is necessary to compensate for signal degradation due to cable lossers, however over-equalization must be avoided to present excessive overshoots resulting in errors during the reception of MLT-3 data. Three operating modes are therefore provided.

These three operating modes are controlled by the state of tristate input "EQS" and are described below:

1)Auto Equalization ("EQS" floating)
Fully automatics equalization is achieved through the use of a feedback loop driven by a control signal derived from the signal amplitude. This provides adaptive control and prevents over-modulation of the signal when short cable lengths are used.

2)Full Equalization ("EQS" low)
In the mode, full equalization is applied to the input signal irrespective of amplitude.

3)No equalization ("EQS" high)
The equalization circuit is disabled completely during this mode.

6.2.2 Baseline wander correction
Any DC offset existing on the received signals will be corrected by this feed forward baseline tracking circuit.

6.2.3 Signal Detector

A signal detect circuit is provided. The circuit continuously monitors the amplitude of the input signal being received on pins RXIP/N. While the input signal reaches the specified level (>0.6V$_{PP}$), the equalization circuits start to pre-process, then the SDO is asserted high after 80ms (max.) pre-process time. Conversely if the signal level falls below a threshold, then SDO will go low.

6.2.4 Receive PLL Clock Recovery

This block generates 125 MHz recovered clock that is locked to the incoming data stream which is feed from MLT-3 to NRZI converter. The PLL is first centered to the transmit clock multiplier, once a valid input signal is present, the PLL will lock to the incoming data stream.

6.2.5 125 MHz shifter to Parallel Data

The data stream is clocked into the serial to parallel register using the 125 MHz clock. This data is latch prior to being clocked out on pins RDAT0-4. A 25 MHz clock, derived from the 125 MHz PLL clock divided by 5, is used to clock the parallel data and is output to pin RSCLK.

6.2.6 Loopback Logic

A low level on 'LBEN' pin defines normal operation, a high level defines loopback mode. In loopback mode, the transmit data is internally routed to the receive circuitry, SDO is forced to be high on level and the TXOP/N outputs are disabled.

7. ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Vcc Supply Voltage Range .... -0.3V to 6V
Storage Temperatur .... -65°C to 150°C

Input Voltage Range
Lead Temperature (10 sec) .... 60°C
Digital Inputs .... -0.3V to Vcc
ESD .... 2k VHHBM

Output Current
TXOP, TXON 70mA
All other outputs 10mA

8. RECOMMENDED OPERATION CONDITIONS

Vcc Supply Voltage	5V to 5%
Operating temperature	0°C to 70°C
Rext	560Ω ± 1%
REF	1.4KΩ ± 1%

9. ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min.	Value Typ.	Max.	Units	Conditions
Power supply current	I_{DD}		95		mA	device only
TTL input high voltage	V_{IH}	2		-	V	
TTL input low voltage	v_{IL}			0.8	V	
EQS input high voltage	V_{IH}	4.2			V	
EQS input low voltage	V_{IL}			0.8	V	
EQS floating voltage	V_{IZ}		$V_{DD}/2$		V	
EQS input high current	V_{IH}		500		uA	$V_{EQS}=V_{DD}$
EQS input low current	V_{IL}		-500		uA	$V_{EQS}=0V$
TTI output high voltage	V_{OH}	2.4			V	$I_{OH}=4mA$
TTL output low voltaage	V_{OL}			0.4	V	$I_{OL}=4mA$
TXOP/N output current			40			$R_{ext}=500\Omega$, 100Mb/s
			70		mA	10Mb/s
Differential RXIP/N signal voltage			1.4	V_{P-P}		measured on device pins 100 Mb/s data, 0m Cable
RXIP/N common mode voltage	V_{COM}		3.3		V	RXIP/N floating
RXIP/N impedance	Z_{IN}		10		KW	
Signal detect threshold	V_{TH}		0.6		Vpp	

10. AC CHARACTERISTICS

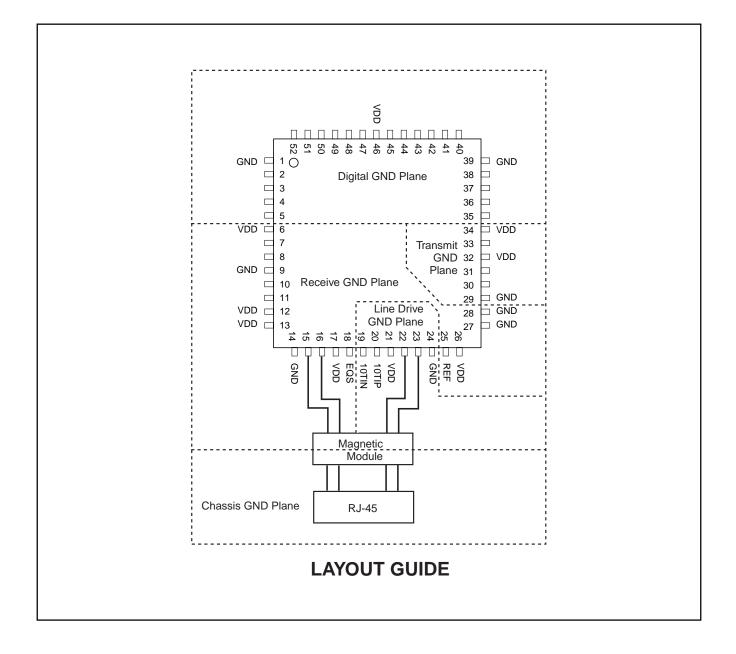| Characteristics	Wareform	Min.	Value Typ.	Max.	Units	Conditions
TXOP/N rise/fall times			2.5		ns	50W load
RSCLK frequency			25		MHz	
RSCLK tolerence			100		ppm	
RSCLK M/S tatio		40/60		60/40	%	
RSCLK to CLKIN propagation delay	(1)		4.5		ns	Transimit PLL is lock
TDAT0-4 to TXCLK setup time	(2)	10			ns	
TDAT0-4 TXCLK hold time	(3)	0			ns	
RDAT0-4 valid to RSCLK	(4)	15			ns	
RSCLK to RDAT0-4 invalid	(5)	15			ns	
RSCLK M/S ratio		40/60		40/60	ns	
TDAT0-4 to CLKIN setup time	(6)		5		ns	
RXIP valid to SDT time delay	(7)			80	ms	

11. WAVEFORM TIMING

12. APPLICATION NOTE

LAYOUT GUIDE

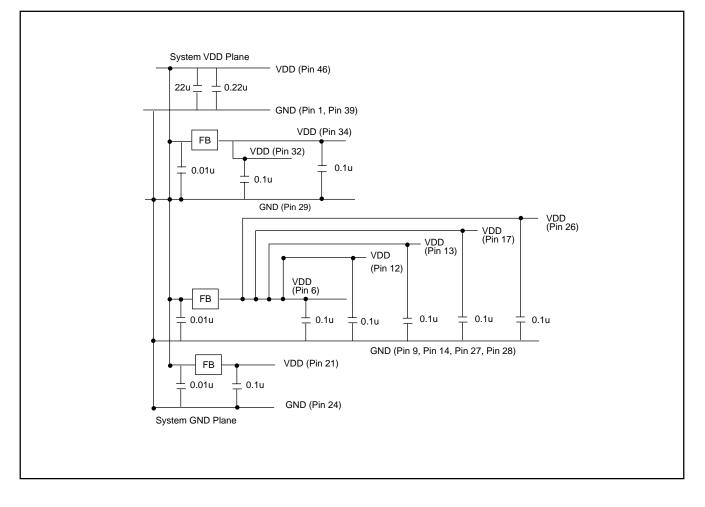## 12.1 LAYOUT GUIDE

Note :
The MX98705 is designed with Macronix mixed mode technology. The above layout guide is recommended for good performance. The GND plane is devided into digital ground, transmit ground, receive ground and line drive ground. Following the layout guide, the system will be with best noise emmunity.

Pin1 and Pin39 are connected to digital GND plane. Pin34 is connected to Transmit GND plane. Pin9, Pin14, Pin27 and Pin28 are connected to Receive GND plane. Pin24 is connected to Line Drive GND plane.

13. PACKAGE INFORMATION

52--Pin Plastic Quad Flat Pack

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