SIEMENS

Mini IOM-2 Controller MICO
PEF 2015 Version 1.1

Addendum 03.98 to the Data Sheet 12.97

Bus Interface Timing

For proper operation of the MICO the timings in figures 19a and 20 (Data Sheet 12.97) are depicted more detailed concerning the \overline{RD} , \overline{WR} , \overline{CS} signals (Siemens/Intel mode) and the R/W, \overline{DS} signals (Motorola mode), respectively.

Between two read (write) accesses in Intel mode the according control signal RD (WR) has to be deactivated. Thus a read/write cycle control by only asserting and deasserting CS is not possible.

The same applies to the DS signal in Motorola mode.

Bus Interface Timing

| Parameter | Symbol | Limit Values | | Unit |
|------------------------------------|-------------------|--------------|------|------|
| | | min. | max. | |
| R or W set-up to DS | $t_{	extsf{DSD}}$ | 0 | | ns |
| R or W hold time from DS | t_{RWh} | | 10 | ns |
| RD-pulse width | t_{RR} | 80 | | ns |
| RD-control interval | t_{RI} | 40 | | ns |
| Data output delay from RDxCS,DSxCS | t_{RD} | | 80 | ns |
| Data float delay from RDxCS, DSxCS | $t_{	extsf{DF}}$ | | 25 | ns |
| WR-pulse width | $t_{\sf WW}$ | 45 | | ns |
| WR-control interval | t_{WI} | 40 | | ns |
| Data set-up time to WRxCS, DSxCS | $t_{\sf DW}$ | 0 | | ns |
| Data hold time from WRxCS, DSxCS | t_{WD} | 15 | | ns |

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Revision History: Previous Version:

Major Changes:

DS 1

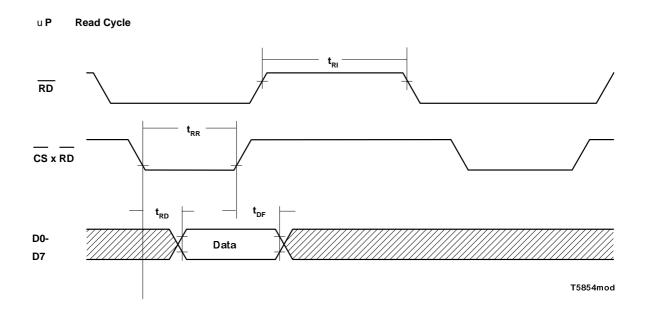


Figure 1 Siemens/Intel Bus Mode

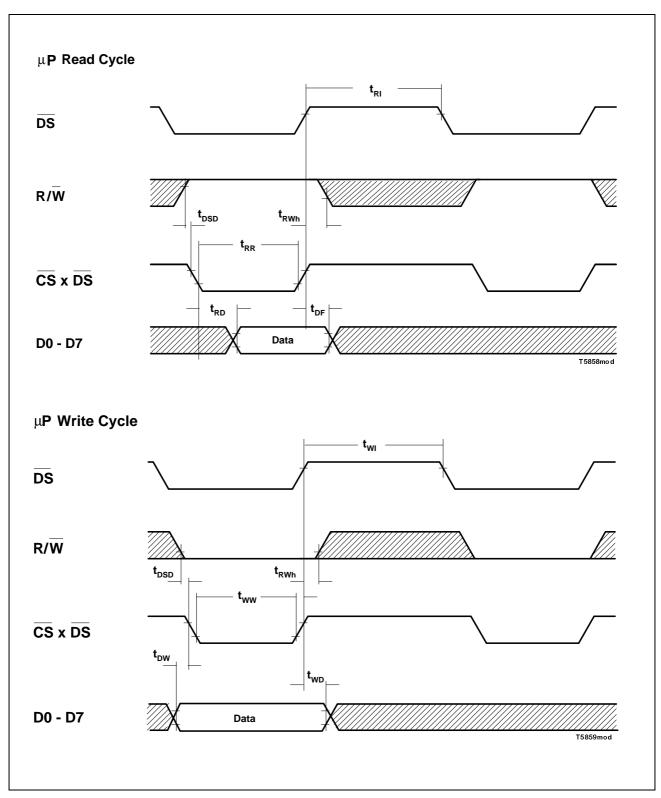


Figure 2 Motorola Mode