LANfinity™ RS7112

Multifunction Controller With Integrated HomePNA 1.0 Physical Layer

The introduction of the **RS7112** Home Networking multifunction controller with integrated HomePNA 1.0 physical layer presents a simple way to network PCs and peripherals in the home while sharing Internet access. This highly integrated, low-cost, and feature-rich solution combines Conexant's experience with multifunction Ethernet controllers and high-speed analog modems with support for the emerging Home Networking standard.

The **RS7112** supports the home phoneline networking standard proposed by the Home Phoneline Networking Alliance (HomePNA 1.0). Products that comply with this specification and combine home networking with high-speed Internet access will change the way people use computers at home. The HomePNA phoneline network utilizes existing telephone wiring to connect computers and devices without interrupting phone service. Industry-standard home networking products will enable a variety of home computing opportunities including

- shared Internet access using a single phone line
- printer/peripheral sharing
- file and application sharing
- networked gaming

Conexant's success in a variety of core technologies used in the **RS7112** allows us to provide a complete home networking solution. In addition to supporting the 1 Mbps home phoneline network standard, the **RS7112** supports PCI and CardBus interfaces, 10/100 Ethernet PHYs, and Conexant's line of 56 Kbps (V.90) modems, including both host-controlled (HCF) and soft (HSF) implementations. The **RS7112** also incorporates all IEEE 802.3 Media Access Control (MAC) functions, provides complete buffer management, the Media Independent Interface (MII), the 7-wire serial interface, and a Flash ROM interface.

When combined with a Conexant HCF or HSF V.90/K56flex modem along with a 10/100 Mbps PHY, the **RS7112** can be used to provide a variety of low-cost home networking plus 56 Kbps modem plus 10/100 Mbps LAN solutions.

Distinguishing Features

- Single-chip multifunction controller supports both CardBus and PCI Bus interfaces
- 100 Mbps IEEE 802.3u 100BASE-T compliant
- 10 Mbps IEEE 802.3 10BASE-T compliant
- Supports the HomePNA 1 Mbps home phoneline network standard (HomePNA 1.0)
- Multifunction logic supports simultaneous modem/network operation
- Power Management Features
  - PCI Power Management compliant
  - PCI Power Management for CardBus compliant
  - PC-98/99 compliant
  - Network Wake-Up Packet (NWUP) support
  - Supports MAGIC PACKET™[1] Wake-Up Technology
- Supports host-controlled HCF and HSF V.90/K56flex™ modems to reduce system chip count and power requirements
- Configurable for full-duplex operation on both 10 Mbps and 100 Mbps
- Separate receive and transmit FIFOs and corresponding DMA controllers
- Smart TX-DMA/RX-DMA arbitration scheme on full duplex model
- Supports a variety of flexible address filtering modes
- Automatic loading of subvendor ID and CardBus Card Information Structure (CIS) pointer from serial ROM to configuration registers

[1] Magic Packet is a trademark of Advanced Micro Devices, Inc.

Distinguishing Features (continued)

- 512 byte CIS RAM for CardBus configuration storage
- Programmable auto-transmit-padding function
- Auto-retransmit
- SNMP 802.3 MIB statistics collection
- Media Independent Interface (MII)
- 7-wire serial interface for home phoneline networking support and Ethernet ENDEC components
- Six general purpose I/O (GPIO) pins and control register
- General purpose timer
- 33 MHz operation (using PCI Clock)
- 3.3 Volt operation with 5 Volt Tolerant I/O
- 176-pin TQFP package or 13 mm (176-pin) BGA

Ordering Information

Product	Package	Device Number
RS7112 Multifunction PCI/CardBus Ethernet and HomeLAN Controller with Integrated HomePNA 1.0 Physical Layer and 56 Kbps HCF/HSF Modem Interface	176-pin TQFP	11623-14
	13 mm BGA	11623D11-16
RS7112-LAN Multifunction PCI/CardBus Ethernet and HomeLAN Controller with Integrated HomePNA 1.0 Physical Layer Only	176-pin TQFP	11623-12
Related Products		
RS7111A Multifunction PCI/CardBus Ethernet and HomeLAN Controller with V.90 HCF Modem Interface	176-pin TQFP	11617-14
RS7111A-LAN Multifunction PCI/CardBus Ethernet and HomeLAN Controller Only	176-pin TQFP	11617-12
RS7220 HomePNA 1.0 Physical Layer device	64-pin TQFP	R8293-11
CN7221 HomePNA 1.0 Physical Layer with Integrated Analog Front End	32-pin TQFP	11625-11

Technical Specifications

Description

The typical application shown in Figure 1 displays a multifunction PCI Network Interface Card (NIC). The NIC incorporates the **RS7112**, a V.90 56 Kbps host-controlled (HCF) modem, and a 10/100 Mbps Ethernet PHY. The system shown provides simultaneous Home Networking/modem functionality, or simultaneous Ethernet LAN/modem functionality.

Home Networking

The home phoneline network is an Ethernet-compatible LAN running over the random-tree wiring found in nearly all homes. It does not require any hubs, routers, splitters, filters or terminations. Home phoneline networking PC network interface cards will interface home computers directly to the network via an in-home telephone jack. Home phoneline networking will also work with current Internet access technologies, such as cable modems, V.90 and ADSL.

Host-Controlled Modem Interface

The **RS7112's** integrated multifunction logic provides the capability for simultaneous modem and network operation Additionally, the **RS7112** supports both HCF and HSF Conexant modems, providing superior system design flexibility.

Both modem designs integrate the functionality of a modem controller fully within the host. This results in a reduced chip count that simplifies system designs, lowers system costs, and reduces power requirements. The **RS7112's** HCF modem interface links directly to a modem datapump, while support for HSF modems provides an even lower system chip count by eliminating the need for a separate modem datapump.

PCI/CardBus Multifunction Interface

The single-chip **RS7112** supports both a direct interface to the PCI Bus or CardBus and a modem interface. The integrated multifunction logic provides the capability for simultaneous modem and network operation. The modem interface is linked to a host-controlled modem. The multifunction logic determines for which function, modem or network, the single interrupt request line, INTA, is intended.

Interactions between the PC host and **RS7112** occur in two modes; programmed I/O (PIO) and bus master. In PIO mode the PC can read and write to control and status registers within the **RS7112** target device, using direct or memory-mapped I/O transactions. This provides the host PC with access to all the control and status registers including the flash ROM and serial EEPROM devices using byte, word, or double word transactions. When operating as bus master the **RS7112** performs Direct Memory Access (DMA) transactions automatically, transferring Ethernet data between its internal FIFOs and PC host memory using efficient burst transactions.

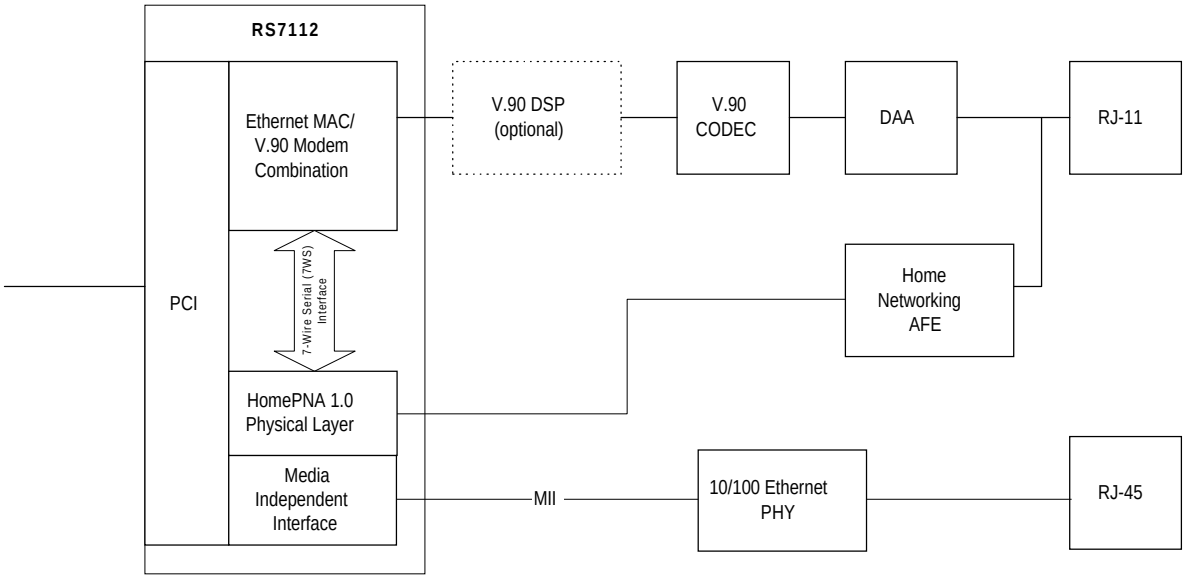


Figure 1. Typical Application

Functional Description

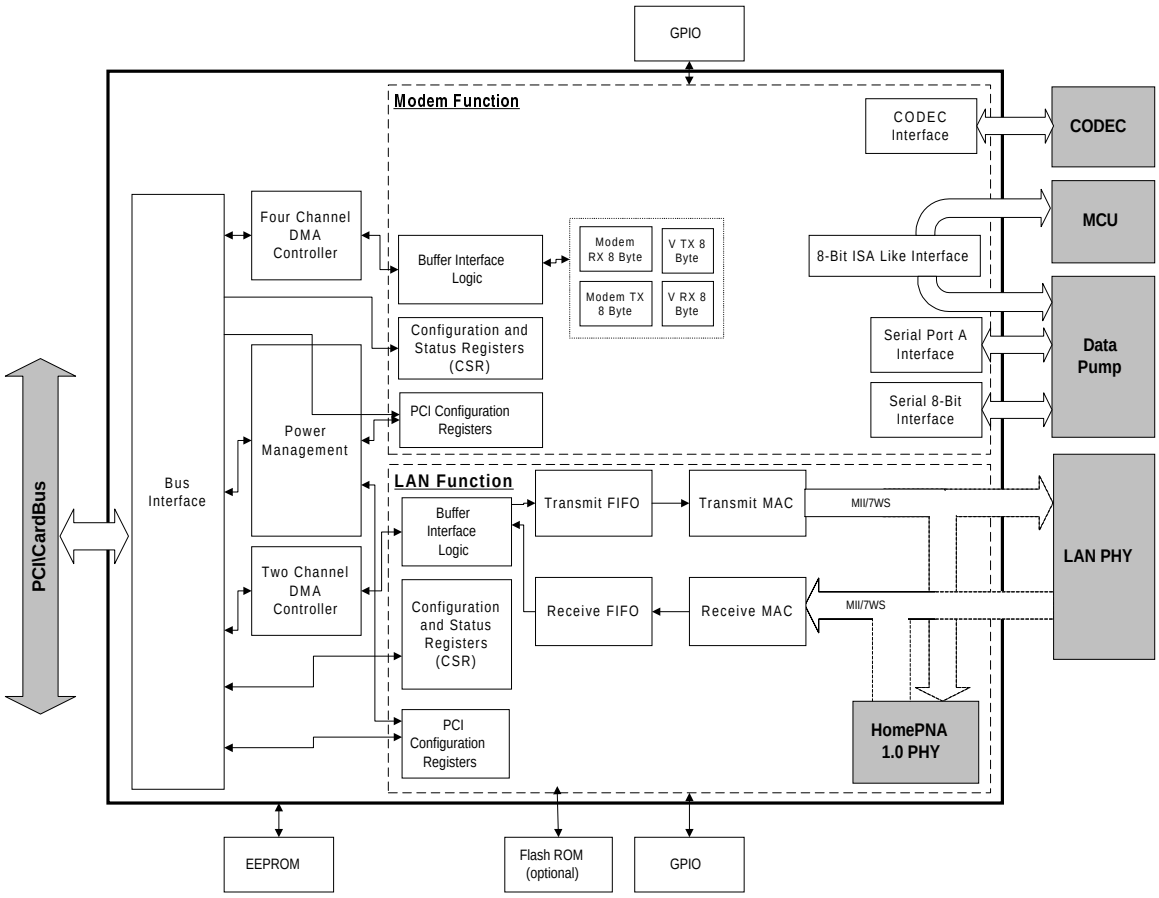


Figure 2. RS7112 Device Architecture Diagram (LAN-only versions do not support modem functionality)

Media Access Controller (MAC)

The **RS7112** supports the MAC sublayer of the IEEE 802.3. It can operate in half-duplex, full duplex, and loopback modes.

In half-duplex mode, the **RS7112** checks the line condition before starting to transmit. If the condition is clear, the **RS7112** starts transmitting. Full duplex operation allows simultaneous transmission and reception of data that can effectively double data throughput to 20 or 200 Mbps.

Physical Layer (PHY) Interface

The integrated HomePNA 1.0 physical layer-portion of the **RS7112** resides between the MAC-portion and the physical medium. It is responsible for receiving and transmitting data on the physical medium, detecting collisions on the physical medium, and translating data to and from the MAC-portion of the **RS7112**.

Buffer Management

The **RS7112** provides a buffer management scheme supporting either chain or ring buffer structures for flexible buffer management. Two DMA engines shuttle the receive and transmit data between the host and **RS7112** automatically.

The buffer management architecture minimizes data handling of the information, thereby reducing CPU overhead. The packet can be in a single fragment or broken into multiple fragments, and is referenced by either single or multiple descriptors respectively. This allows quick access and minimal handling of the data. Data is transferred in the most efficient manner using PCI burst transfers and direct memory access.

Two large independent internal FIFOs, each 32-bits wide, provide multiple data packet transmit and receive buffering with programmable thresholds and store-and-forward modes. The receive FIFO is 4K bytes and the transmit FIFO is 2K bytes.

Address Filtering

The **RS7112** device supports five types of address filtering. Each is described in more detail in the following sections. The filtering is configured through setup frames sent to the **RS7112**.

16-address perfect filtering: The **RS7112** provides support for the perfect filtering of up to 16 Ethernet unicast or multicast addresses. Any mix of addresses can be used.

One unicast address perfect and unlimited multicast address imperfect filtering: The **RS7112** supports one, single unicast address to be perfectly filtered with an unlimited number of multicast addresses to be imperfectly filtered.

Unlimited unicast addresses and multicast addresses imperfect filtering: The **RS7112** supports imperfect filtering for an unlimited number of unicast addresses as well as multicast addresses. This feature permits the reception of more than 16 multicast addresses while supporting applications requiring more than one unicast address to be filtered as the station address.

Promiscuous mode: The **RS7112** supports the reception of all good frames.

Pass all multicast: The **RS7112** supports the reception of all multicast frames.

Loopback Operations

The **RS7112** supports internal and external loopback modes. Internal loopback mode can be used to verify the correct operation of internal logic operations. External loopback mode can be used to verify that the logic operations up to the Ethernet wire function correctly.

Power Management Features

PC-98/99-compliance

The **RS7112** implements power management features to minimize system power consumption, manage system thermal limits, and maximize system battery life. The device complies with the Communications and Network Class Power Management Specifications, PCI Bus Power Management Interface Specification v1.1, and the draft PCI Power Management for CardBus Specification. This assures the device will comply with Microsoft's OnNow and PC-98/99 specifications.

3.3Vaux Auxiliary Power-On Support

The **RS7112** supports PC systems that comply with the PCI Bus Power Management Interface Specification. To support keep-alive circuitry, power managed systems must provide an optional 3.3Vaux auxiliary power source because the VCC pins on the PCI expansion slot have been turned off. Auxiliary power can be provided by an on-board battery, an AC adapter (externally provided power source), or by auxiliary power supplied by the system.

Wake-up Technologies

Network Wake-Up Packet (NWUP) Support

The **RS7112** supports a network wake-up frame detection scheme. Every incoming packet can be checked against a matching wake-up frame template to determine if a wake-up event has occurred. The template is stored in the **RS7112's** 2 Kbyte transmit FIFO. If a wake-up event has occurred, the **RS7112** will restore the host system to a state that will permit the operating system to function.

This Wake-on-LAN feature can be used to wake-up a device on the network for a variety of purposes:

- To request network management information
- To use a service or resource located on the device

MAGIC PACKET

MAGIC PACKET technology has been implemented in the **RS7112**. A MAGIC PACKET is a protocol independent Ethernet frame sent to a single network node that allows sleeping Green PCs to be remotely woken up. When a MAGIC PACKET is received, the **RS7112** device asserts a Power Management Enable (PME) interrupt to wake up the host. Previously, once a Green PC was shutdown to conserve power, network administrators wishing to perform a task had to physically locate the node and turn it on. With MAGIC PACKET technology this function can be performed using software commands from a management console.

Wake on Ring

The **RS7112** device supports Wake on Ring, a feature that allows a PC to power on when receiving an incoming call. Upon the first ring received, the device asserts a Power Management Enable (PME) interrupt to wake up the host. It also stores the Caller ID information received between rings. The host powers up upon receiving the interrupt and begins processing the call.

Configuration

The serial EEPROM interface is used to load the CIS information required for CardBus information. The CIS information is read from the serial EEPROM and stored in host memory. The **RS7112** configuration information requires 21 bytes of data for the modem function and 10 bytes of data for the LAN function. The minimum serial EEPROM size is 512 bytes (4096 bits).

The **RS7112** device functions as memory slave and bus master for PC memory accesses. One memory block of 64K is allocated to the modem function and one block of 16K is allocated to the LAN function.

7-Wire Serial Interface (7WS)

The serial port consists of seven signals that provide a conventional interface to 10 Mbps Ethernet ENDEC components. In addition, the 7WS supports the 1 Mbps home networking PHY. The 7WS signals are multiplexed with the MII signals so that the **RS7112** alternately supports either an Ethernet 10/100 PHY or the 1 Mbps home networking PHY.

MII Interface

The MII port provides a simple and easily implemented interconnection between the **RS7112** and PHY sublayer. The MII port is media independent, multi-vendor interoperable, and supports all data rates and physical standards. It consists of data paths that are 4-bits wide in each direction as well as control and management signals.

External Ports

Flash ROM Interface

The **RS7112** provides a ROM interface that may be optionally used on a network adapter. The flash ROM may contain code that can be executed for device-specific initialization and potentially for system boot. During machine boot, the BIOS looks for bootable devices by searching a specific signature (55AAh). When found, the BIOS copies the code from the Flash ROM to a shadow RAM in the host memory and executes the code from that RAM.

The interface supports:

- 3V, 5V, or 12V flash memory
- Up to 64 KB address space

Serial EEPROM Interface

The serial EEPROM interface is used to load the PCI/CardBus configuration information as well as the CIS information required for CardBus information. The CIS information for each function, LAN and modem, is read from the serial EEPROM and stored in each function's internal CIS RAM. The **RS7112** PCI/CardBus configuration information requires 25 bytes of data for the modem function and 27 bytes of data for the LAN function. The minimum serial EEPROM size is 512 bytes (4096 bits).

The **RS7112** device functions as memory slave and bus master for PC memory accesses. One memory block of 64K is allocated to the modem function and one block of 16K is allocated to the LAN function.

The CIS information for each function is read from the serial EEPROM and stored in the internal RAM of the **RS7112**. The serial EEPROM may be programmed in system. The pins of the serial EEPROM are directly programmable via PIO.

GPIO Interface

The **RS7112** provides six General Purpose Input/Output (GPIO) pins. General Purpose pins can be used by software as either status pins or control pins and configured by software to perform either input or output functions. Two GPIO pins are dedicated to modem functionality and the remaining four are dedicated to LAN functionality.

Pinout Diagrams[2]

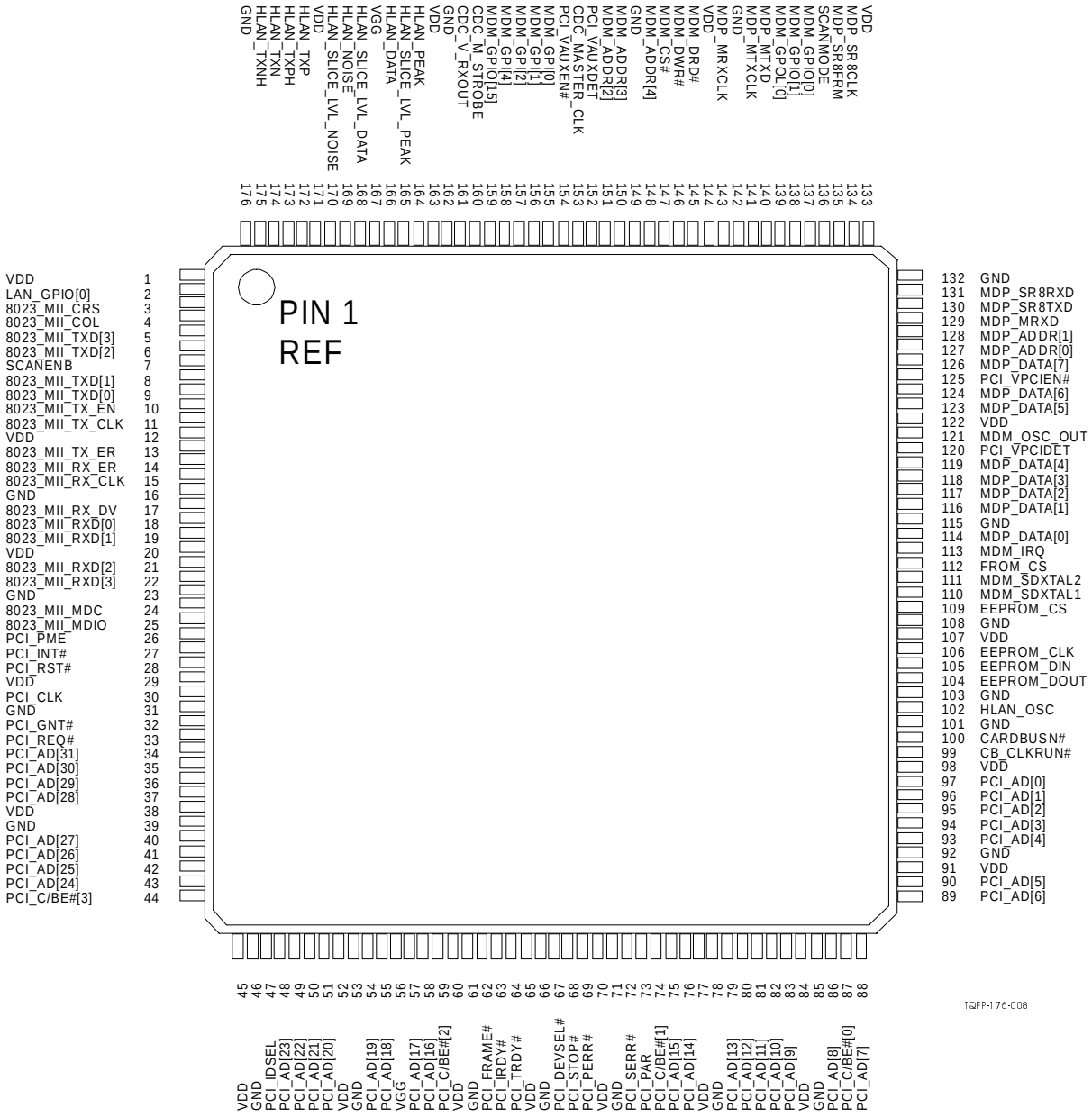
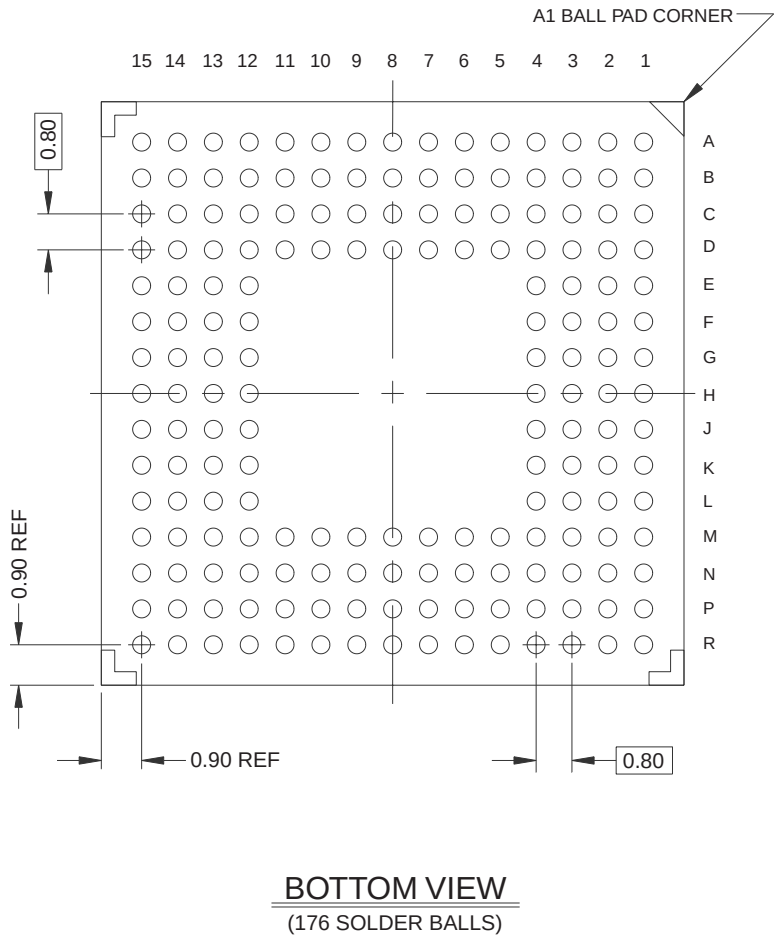


Figure 3. RS7112 176-pin TQFP Pinout Diagram (Device Number 11623-14)

[2] Logic low active signals are followed by a pound (#).



Refer also to Table 2, 176-pin BGA Pin Designations by Number.

Figure 4. RS7112 176-pin BGA Pinout Diagram (Device Number 11623D11-16)

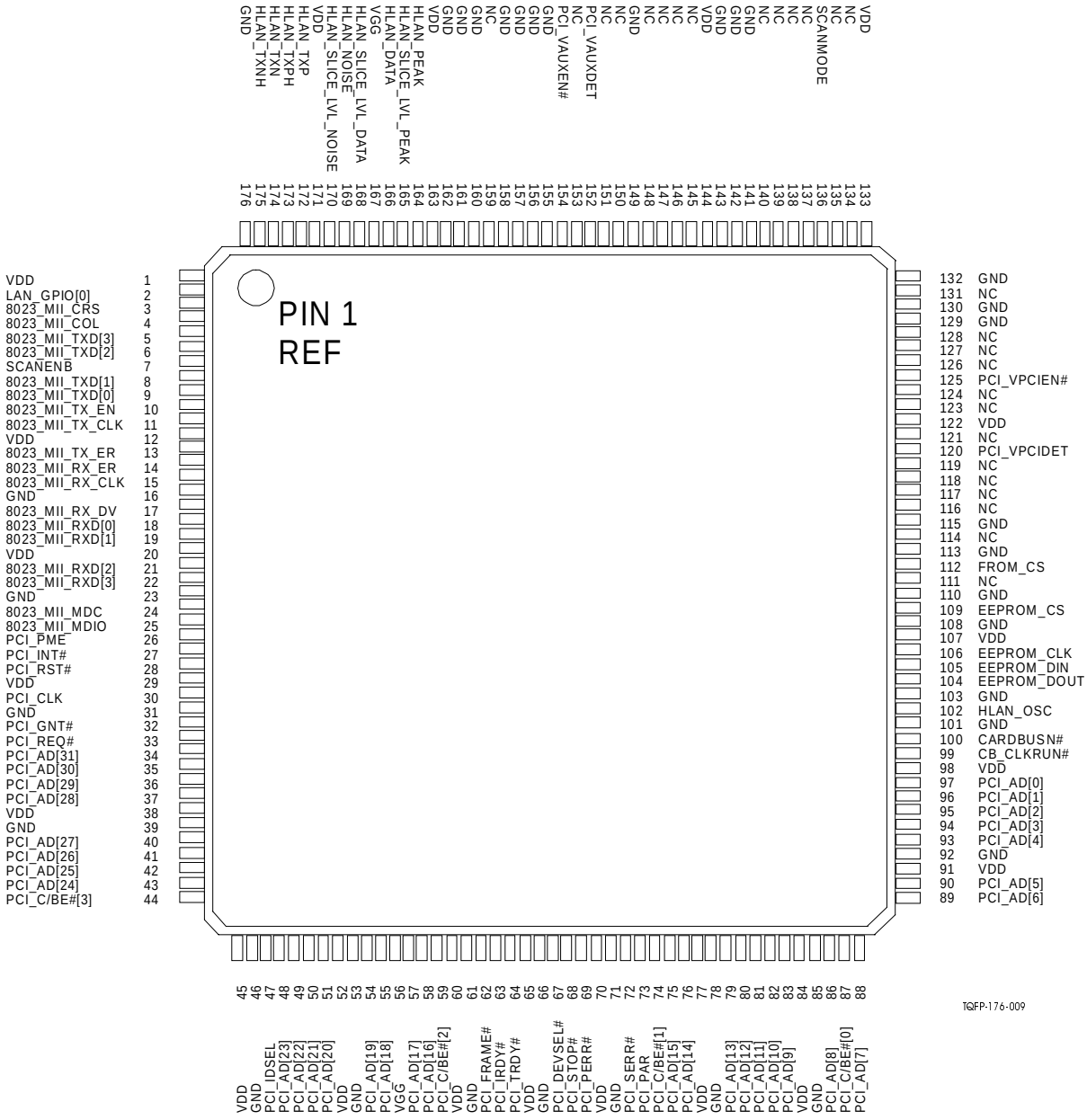


Figure 5. RS7112-LAN 176-pin TQFP Pinout Diagram (Device Number 11623-12)

Table 1. RS7112 176-pin TQFP Pin Designations by Number[3] (Device Number 11623-14)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	VDD	45	VDD	89	PCI_AD[6]	133	VDD
2	LAN_GPIO[0]	46	GND	90	PCI_AD[5]	134	MDP_SR8CLK
3	*8023_MII_CRS*	47	PCI_IDSEL	91	VDD	135	MDP_SR8FRM
4	*8023_MII_COL*	48	PCI_AD[23]	92	GND	136	SCANMODE
5	*8023_MII_TXD[3]*	49	PCI_AD[22]	93	PCI_AD[4]	137	MDM_GPIO[0]
6	8023_MII_TXD[2]	50	PCI_AD[21]	94	PCI_AD[3]	138	MDM_GPIO[1]
7	SCANENB	51	PCI_AD[20]	95	PCI_AD[2]	139	MDM_GPOL[0]
8	8023_MII_TXD[1]	52	VDD	96	PCI_AD[1]	140	*MDP_MTXD*
9	8023_MII_TXD[0]	53	GND	97	PCI_AD[0]	141	*MDP_MTXCLK*
10	*8023_MII_TX_EN*	54	PCI_AD[19]	98	VDD	142	GND
11	*8023_MII_TX_CLK*	55	PCI_AD[18]	99	CB_CLKRUN#	143	*MDP_MRXCLK*
12	VDD	56	VGG	100	CARDBUSN#	144	VDD
13	8023_MII_TX_ER	57	PCI_AD[17]	101	GND	145	*MDM_DRD#*
14	8023_MII_RX_ER	58	PCI_AD[16]	102	HLAN_OSC	146	*MDM_DWR#*
15	*8023_MII_RX_CLK*	59	PCI_C/BE#[2]	103	GND	147	MDM_CS#
16	GND	60	VDD	104	*EEPROM_DOUT*	148	MDM_ADDR[4]
17	8023_MII_RX_DV	61	GND	105	*EEPROM_DIN*	149	GND
18	8023_MII_RXD[0]	62	PCI_FRAME#	106	*EEPROM_CLK*	150	MDM_ADDR[3]
19	8023_MII_RXD[1]	63	PCI_IRDY#	107	VDD	151	MDM_ADDR[2]
20	VDD	64	PCI_TRDY#	108	GND	152	PCI_VAUXDET
21	8023_MII_RXD[2]	65	VDD	109	EEPROM_CS	153	CDC_MASTER_CLK
22	*8023_MII_RXD[3]*	66	GND	110	MDM_SDXTAL1	154	PCI_VAUXEN#
23	GND	67	PCI_DEVSEL#	111	MDM_SDXTAL2	155	MDM_GPI[0]
24	8023_MII_MDC	68	PCI_STOP#	112	FROM_CS	156	MDM_GPI[1]
25	8023_MII_MDIO	69	PCI_PERR#	113	MDM_IRQ	157	MDM_GPI[2]
26	PCI_PME	70	VDD	114	MDP_DATA[0]	158	MDM_GPI[4]
27	PCI_INT#	71	GND	115	GND	159	MDM_GPIO[15]
28	PCI_RST#	72	PCI_SERR#	116	MDP_DATA[1]	160	CDC_M_STROBE
29	VDD	73	PCI_PAR	117	MDP_DATA[2]	161	CDC_V_RXOUT
30	PCI_CLK	74	PCI_C/BE#[1]	118	MDP_DATA[3]	162	GND
31	GND	75	PCI_AD[15]	119	MDP_DATA[4]	163	VDD
32	PCI_GNT#	76	PCI_AD[14]	120	PCI_VPCIDET	164	HLAN_PEAK
33	PCI_REQ#	77	VDD	121	MDM_OSC_OUT	165	HLAN_SLICE_LVL_PEAK
34	PCI_AD[31]	78	GND	122	VDD	166	HLAN_DATA
35	PCI_AD[30]	79	PCI_AD[13]	123	MDP_DATA[5]	167	VGG
36	PCI_AD[29]	80	PCI_AD[12]	124	MDP_DATA[6]	168	HLAN_SLICE_LVL_DATA
37	PCI_AD[28]	81	PCI_AD[11]	125	PCI_VPCIEN#	169	HLAN_NOISE
38	VDD	82	PCI_AD[10]	126	MDP_DATA[7]	170	HLAN_SLICE_LVL_NOISE
39	GND	83	PCI_AD[9]	127	MDP_ADDR[0]	171	VDD
40	PCI_AD[27]	84	VDD	128	MDP_ADDR[1]	172	HLAN_TXP
41	PCI_AD[26]	85	GND	129	*MDP_MRXD*	173	HLAN_TXPH
42	PCI_AD[25]	86	PCI_AD[8]	130	*MDP_SR8TXD*	174	HLAN_TXN
43	PCI_AD[24]	87	PCI_C/BE#[0]	131	*MDP_SR8RXD*	175	HLAN_TXNH
44	PCI_C/BE#[3]	88	PCI_AD[7]	132	GND	176	GND

[3] Logic low active signals are followed by a pound (#). Multiplexed signals are in *italics*.

Table 2. RS7112 176-pin BGA Pin Designations by Number[4] (Device Number 11623D11-16)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
A1	VDD	C15	*MDP_SR8TXD*	H12	GND	N2	PCI_AD[24]
A2	GND	D1	8023_MII_TXD[2]	H13	MDM_SDXTAL1	N3	VDD
A3	HLAN_TXN	D2	*8023_MII_TX_EN*	H14	FROM_CS	N4	PCI_AD[20]
A4	HLAN_TXPH	D3	SCANENB	H15	GND	N5	PCI_AD[18]
A5	VDD	D4	HLAN_NOISE	J1	GND	N6	PCI_C/BE#[2]
A6	HLAN_SLICE_LVL_DATA	D5	HLAN_SLICE_LVL_PEAK	J2	PCI_RST#	N7	PCI_IRDY#
A7	VDD	D6	CDC_V_RXOUT	J3	GND	N8	GND
A8	MDM_GPIO[15]	D7	MDM_GPI[2]	J4	8023_MII_MDIO	N9	PCI_DEVSEL#
A9	MDM_ADDR[3]	D8	PCI_VAUXDET	J12	*EEPROM_DOUT*	N10	VDD
A10	*MDM_DWR#*	D9	MDM_ADDR[4]	J13	VDD	N11	PCI_C/BE#[1]
A11	*MDP_MTXCLK*	D10	VDD	J14	EEPROM_CS	N12	GND
A12	MDM_GPIO[1]	D11	*MDP_MTXD*	J15	*EEPROM_CLK*	N13	PCI_AD[10]
A13	SCANMODE	D12	PCI_VPCIEN#	K1	PCI_AD[29]	N14	PCI_AD[4]
A14	MDP_SR8FRM	D13	VDD	K2	PCI_GNT#	N15	GND
A15	VDD	D14	MDP_ADDR[1]	K3	PCI_PME	P1	PCI_C/BE#[3]
B1	*8023_MII_CRS*	D15	*MDP_MRXD*	K4	VDD	P2	GND
B2	LAN_GPIO[0]	E1	8023_MII_TXD[0]	K12	CARDBUSN#	P3	PCI_AD[22]
B3	HLAN_TXNH	E2	8023_MII_TX_ER	K13	GND	P4	PCI_AD[19]
B4	HLAN_TXP	E3	8023_MII_TX_CLK	K14	*EEPROM_DIN*	P5	PCI_AD[17]
B5	VGG	E4	8023_MII_TXD[1]	K15	HLAN_OSC	P6	GND
B6	HLAN_PEAK	E12	MDM_OSC_OUT	L1	GND	P7	VDD
B7	CDC_M_STROBE	E13	MDP_DATA[3]	L2	PCI_AD[30]	P8	PCI_STOP#
B8	MDM_GPI[1]	E14	MDP_DATA[5]	L3	PCI_CLK	P9	PCI_SERR#
B9	CDC_MASTER_CLK	E15	MDP_ADDR[0]	L4	PCI_REQ#	P10	PCI_AD[14]
B10	GND	F1	8023_MII_RX_ER	L12	PCI_AD[1]	P11	PCI_AD[13]
B11	*MDM_DRD#*	F2	8023_MII_RX_DV	L13	CB_CLKRUN#	P12	VDD
B12	GND	F3	*8023_MII_RX_CLK*	L14	GND	P13	PCI_C/BE#[0]
B13	MDM_GPIO[0]	F4	VDD	L15	PCI_AD[0]	P14	PCI_AD[5]
B14	MDP_SR8CLK	F12	MDP_DATA[2]	M1	PCI_AD[26]	P15	VDD
B15	GND	F13	MDP_DATA[0]	M2	PCI_AD[27]	R1	VDD
C1	*8023_MII_COL*	F14	PCI_VPCIDET	M3	PCI_AD[31]	R2	PCI_IDSEL
C2	*8023_MII_TXD[3]*	F15	MDP_DATA[6]	M4	PCI_AD[28]	R3	PCI_AD[23]
C3	HLAN_SLICE_LVL_NOISE	G1	8023_MII_RXD[0]	M5	VDD	R4	PCI_AD[21]
C4	HLAN_DATA	G2	8023_MII_RXD[2]	M6	VGG	R5	GND
C5	GND	G3	8023_MII_RXD[1]	M7	VDD	R6	PCI_AD[16]
C6	MDM_GPI[4]	G4	GND	M8	PCI_TRDY#	R7	PCI_FRAME#
C7	MDM_GPI[0]	G12	MDM_IRQ	M9	PCI_PERR#	R8	GND
C8	PCI_VAUXEN#	G13	MDM_SDXTAL2	M10	PCI_PAR	R9	PCI_AD[15]
C9	MDM_ADDR[2]	G14	MDP_DATA[1]	M11	VDD	R10	PCI_AD[12]
C10	MDM_CS#	G15	MDP_DATA[4]	M12	PCI_AD[11]	R11	PCI_AD[9]
C11	*MDP_MRXCLK*	H1	PCI_INT#	M13	PCI_AD[2]	R12	GND
C12	MDM_GPOL[0]	H2	8023_MII_MDC	M14	VDD	R13	PCI_AD[8]
C13	MDP_DATA[7]	H3	*8023_MII_RXD[3]*	M15	PCI_AD[3]	R14	PCI_AD[7]
C14	*MDP_SR8RXD*	H4	VDD	N1	PCI_AD[25]	R15	PCI_AD[6]

Refer to Figure 4 for position of pins on BGA

[4] Logic low active signals are followed by a pound (#). Multiplexed signals are in *italics*.

Table 3. RS7112-LAN 176-pin TQFP Pin Designations by Number[5] (Device Number 11623-12)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	VDD	45	VDD	89	PCI_AD[6]	133	VDD
2	LAN_GPIO[0]	46	GND	90	PCI_AD[5]	134	NC
3	8023_MII_CRS	47	PCI_IDSEL	91	VDD	135	NC
4	8023_MII_COL	48	PCI_AD[23]	92	GND	136	SCANMODE
5	8023_MII_TXD[3]	49	PCI_AD[22]	93	PCI_AD[4]	137	NC
6	8023_MII_TXD[2]	50	PCI_AD[21]	94	PCI_AD[3]	138	NC
7	SCANENB	51	PCI_AD[20]	95	PCI_AD[2]	139	NC
8	8023_MII_TXD[1]	52	VDD	96	PCI_AD[1]	140	NC
9	8023_MII_TXD[0]	53	GND	97	PCI_AD[0]	141	GND
10	8023_MII_TX_EN	54	PCI_AD[19]	98	VDD	142	GND
11	8023_MII_TX_CLK	55	PCI_AD[18]	99	CB_CLKRUN#	143	GND
12	VDD	56	VGG	100	CARDBUSN#	144	VDD
13	8023_MII_TX_ER	57	PCI_AD[17]	101	GND	145	NC
14	8023_MII_RX_ER	58	PCI_AD[16]	102	HLAN_OSC	146	NC
15	8023_MII_RX_CLK	59	PCI_C/BE#[2]	103	GND	147	NC
16	GND	60	VDD	104	EEPROM_DOUT	148	NC
17	8023_MII_RX_DV	61	GND	105	EEPROM_DIN	149	GND
18	8023_MII_RXD[0]	62	PCI_FRAME#	106	EEPROM_CLK	150	NC
19	8023_MII_RXD[1]	63	PCI_IRDY#	107	VDD	151	NC
20	VDD	64	PCI_TRDY#	108	GND	152	PCI_VAUXDET
21	8023_MII_RXD[2]	65	VDD	109	EEPROM_CS	153	NC
22	8023_MII_RXD[3]	66	GND	110	GND	154	PCI_VAUXEN#
23	GND	67	PCI_DEVSEL#	111	NC	155	GND
24	8023_MII_MDC	68	PCI_STOP#	112	FROM_CS	156	GND
25	8023_MII_MDIO	69	PCI_PERR#	113	GND	157	GND
26	PCI_PME	70	VDD	114	NC	158	GND
27	PCI_INT#	71	GND	115	GND	159	NC
28	PCI_RST#	72	PCI_SERR#	116	NC	160	GND
29	VDD	73	PCI_PAR	117	NC	161	GND
30	PCI_CLK	74	PCI_C/BE#[1]	118	NC	162	GND
31	GND	75	PCI_AD[15]	119	NC	163	VDD
32	PCI_GNT#	76	PCI_AD[14]	120	PCI_VPCIDET	164	HLAN_PEAK
33	PCI_REQ#	77	VDD	121	NC	165	HLAN_SLICE_LVL_PEAK
34	PCI_AD[31]	78	GND	122	VDD	166	HLAN_DATA
35	PCI_AD[30]	79	PCI_AD[13]	123	NC	167	VGG
36	PCI_AD[29]	80	PCI_AD[12]	124	NC	168	HLAN_SLICE_LVL_DATA
37	PCI_AD[28]	81	PCI_AD[11]	125	PCI_VPCIEN#	169	HLAN_NOISE
38	VDD	82	PCI_AD[10]	126	NC	170	HLAN_SLICE_LVL_NOISE
39	GND	83	PCI_AD[9]	127	NC	171	VDD
40	PCI_AD[27]	84	VDD	128	NC	172	HLAN_TXP
41	PCI_AD[26]	85	GND	129	GND	173	HLAN_TXPH
42	PCI_AD[25]	86	PCI_AD[8]	130	GND	174	HLAN_TXN
43	PCI_AD[24]	87	PCI_C/BE#[0]	131	NC	175	HLAN_TXNH
44	PCI_C/BE#[3]	88	PCI_AD[7]	132	GND	176	GND

[5] Logic low active signals are followed by a pound (#).

Table 4. Pin Designations by Group[6]

PCI/CardBus Signals[7]

Pin Name	Type	Schmitt	Resistive	Drive	Description
PCI_AD[31:0]	I/O	×	—	PCI CardBus	Multiplexed Address/Data
PCI_C/BE#[3:0]	I/O	×	—	PCI CardBus	Command/Byte Enables for PCI/CardBus Bus Indicates the bytes to be transferred in the currently addressed DWORD as well as the data path(s) to be used during the transfer.
PCI_FRAME#	I/O	×	—	PCI CardBus	Frame Driven by the transaction initiator to indicate the start and duration of the transaction.
PCI_IRDY#	I/O	×	—	PCI CardBus	Initiator Ready Driven by the current Bus Master. Indicates that the Bus Master is driving valid data on the bus or is ready to accept valid data.
PCI_TRDY#	I/O	×	—	PCI CardBus	Target Ready Driven by the current Target to indicate that it is ready to complete the current data phase.
PCI_PAR	I/O	×	—	PCI CardBus	Parity (Even) Driven by the initiator or the target to ensure even parity of the AD and C/BE# lines.
PCI_STOP#	I/O	×	—	PCI CardBus	Target Stop Asserted by the Target to stop the current transaction.
PCI_DEVSEL#	I/O	×	—	PCI CardBus	Device Select Asserted by the Target when the Target has decoded its address.
PCI_IDSEL	I	×	—	—	Initialization Device Select An input to a PCI device used as a chip select during access to a device's configuration register(s). This signal should be tied high (asserted) in a CardBus environment
PCI_PERR#	I/O	×	—	PCI CardBus	Parity Error Asserted by the Target to indicate that a parity error was detected.
PCI_SERR#	I/O	—	—	PCI CardBus	System Error Used by a PCI device to indicate a catastrophic system error.
PCI_REQ#	O	×	—	PCI CardBus	Master Request Asserted by a Bus Master to request access to the bus.
PCI_GNT#	I	×	—	—	Grant Asserted by the Bus Master Arbiter to indicate that it is the particular Master's turn to use the bus.
PCI_CLK	I	×	—	—	PCI Clock Signal Input to all devices residing on the PCI bus. All inputs are sampled on the rising edge of the PCI_CLK signal.
PCI_RST#	I	×	—	—	Reset Causes all PCI devices to return to an initialized state.
PCI_INT#	O	—	—	PCI CardBus	Interrupt Asserted by a PCI device to indicate a hardware interrupt.
PCI_PME	O	—	—	2mA	PCI/CardBus Power Management Event Signal.

[6] Logic low active signals are followed by a pound (#). Open drain signals are designated by OD. Tristate signals are indicated by TS and Sustained Tri State signals by STS. Sustained tristate signals are driven high before going into tri-state.
Schmitt: — = does not apply, × = does not support, ✓ = supports
Resistive: — = does not apply, ↑ = pull-up, ↓ = pull-down

[7] See PCI Local Bus Specification, Rev. 2.1, April 1994

Pin Name	Type	Schmitt	Resistive	Drive	Description
					This signal is active high and requires an external FET to connect to PCI PME#.
CB_CLKRUN#	I/O	×	—	CardBus	Clock Run signal for CardBus This signal should be tied low (always asserted) in a PCI environment since the PCI Bus does not provide this signal.
CARDBUSN#	I	×	↑	—	Controls the drive strength of bus interface signals. 0: CardBus 1: PCI

Home LAN

Pin Name	Type	Schmitt	Resistive	Drive	Description
HLAN_OSC	I			CMOS	60 MHz oscillator input
HLAN_TXP	O			12mA	Positive transmit output
HLAN_TXPH	O			12mA	High-power positive transmit output
HLAN_TXNH	O			12mA	High-power negative transmit output
HLAN_TXN	O			12mA	High power negative transmit output
HLAN_SLICE_LVL_NOISE	O			6mA	Pulse width modulated D/A output for slice level on NOISE comparator
HLAN_SLICE_LVL_DATA	O			6mA	Pulse width modulated D/A output for slice level on DATA comparator
HLAN_SLICE_LVL_PEAK	O			6mA	Pulse width modulated D/A output for slice level on PEAK comparator
HLAN_NOISE	I			CMOS	Rising edge on signal crossing NOISE threshold
HLAN_PEAK	I			CMOS	Rising edge on signal crossing PEAK threshold
HLAN_DATA	I			CMOS	Rising edge on signal crossing DATA threshold

Codec Interface

Pin Name	Type	Schmitt	Resistive	Drive	Description
CDC_M_STROBE					Serial Frame Synchronization (strobe)
CDC_V_RXOUT					Serial data input from Voice
CDC_V_CTRL *multiplexed signal* *MDM_DRD#*					Serial Control Output
CDC_M_RXOUT *multiplexed signal* *MDP_MRXD*					Serial Data from Codec
CDC_MASTER_CLK					Codec Master Clock
CDC_M_CTRL *multiplexed signal* *MDP_SR8TXD*					Serial Control Output
CDC_V_STROBE *multiplexed signal* *MDP_SR8RXD*					Serial Frame Synchronization (strobe)
CDC_M_TXSIN *multiplexed signal* *MDP_MTXD*					Serial Data to Codec
CDC_V_CLK *multiplexed signal*					Voice Clock from Modem Codec

Pin Name	Type	Schmitt	Resistive	Drive	Description
MDP_MTXCLK					
CDC_V_TXSIN *multiplexed signal* *MDM_DWR#*					Serial output to Voice Codec
CDC_M_CLK *multiplexed signal* *MDP_MRXCLK*					Modem clock from Modem IA

Serial Peripheral Interface (SPI) Signals

Pin Name	Type	Schmitt	Resistive	Drive	Description
SPI_DOUT *multiplexed signal* *EEPROM_DOUT*	O	—	—	2ma	Serial Peripheral Interface (SPI) Data Output Data is read from an external SPI device on this pin. See the LANfinity Software Designer's Guide's documentation on the LAN Serial Port Register for information on driving this signal using software.
SPI_DIN *multiplexed signal* *EEPROM_DIN*	I	×	—	—	Serial Peripheral Interface (SPI) Data Input Data is written to an SPI device using this pin. See the LANfinity Software Designer's Guide's documentation on the LAN Serial Port Register for information on driving this signal using software.
SPI_CLK *multiplexed signal* *EEPROM_CLK*	O	—	—	2ma	Serial Peripheral Interface Clock This pin serves as the clock for an external device. Software is responsible for generating the clock. See the LANfinity Software Designer's Guide's documentation on the LAN Serial Port Register for information on driving this signal using software. Refer to the serial device's data sheet to determine the maximum clock rate the device can support.

PCI Power Management Signals

Pin Name	Type	Schmitt	Resistive	Drive	Description
PCI_VAUXEN#	O	—	—	2mA	1 = Disable the FET connecting VAUX power supply to the Device 0 = enable the FET. Optional for WAKE UP
PCI_VPCIEN# Defined for PCI Only	O	—	—	2mA	1 = enables the Vpci FET
PCI_VPCIDET Defined for PCI Only	I	✓	↓	—	Logical input connected to Vpci
PCI_VAUXDET Defined for PCI Only	I	✓	↓	—	Logic input connected to 3.3Vaux

Modem Data Pump (MDP) Signals

Pin Name	Type	Schmitt	Resistive	Drive	Description
MDM_ADDR[4:2]	O	—	—	2ma	Address Lines to MCU or MDP
MDM_DWR# *multiplexed signal* *CDC_V_TXSIN*	O	—	—	2ma	Modem Device Write Enable Connected to MCU or MDP
MDM_DRD# *multiplexed signal* *CDC_V_CTRL*	O	—	—	2ma	Modem Device Read Enable Connected to MCU or MDP

Pin Name	Type	Schmitt	Resistive	Drive	Description
MDM_CS#	O	—	—	2ma	MDP Chip Select
MDM_IRQ	I	×	—	—	MDP Interrupt Request
MDM_GPI[0]	I	✓	—	—	General Purpose Input for Modem Function
MDM_GPI[1]	I	✓	↑ 75Kohm	—	
MDM_GPI[2]	I				
MDM_GPI[4]	I				
MDM_GPIO[1:0]	I/O	✓	↑	12mA	General Purpose I/O pins
MDM_GPOL[0]	O	—	—	4mA	General Purpose Output for Modem Function Reset to low after deassertion of PCI_RST#.
MDP_MRXD *multiplexed signal* *CDC_M_RXOUT*	I	×	—	—	Modem Receive Data from Data Pump
MDP_MRXCLK *multiplexed signal* *CDC_M_CLK*	I	×	—	—	Modem Receive Clock from MDP
MDP_MTXCLK *multiplexed signal* *CDC_V_CLK*	I	×	—	—	Modem Transmit Clock from MDP
MDP_MTXD *multiplexed signal* *CDC_M_TXSIN*	O	—	—	2mA	Modem Transmit Data to MDP
MDP_SR8CLK	I/O	×	—	4mA	Serial interface clock from MDP
MDP_SR8TXD *multiplexed signal* *CDC_M_CTRL*	O	—	—	2mA	Serial interface Transmit Data to MDP
MDP_SR8RXD *multiplexed signal* *CDC_V_STROBE*	I	×	—	—	Serial interface Receive Data from MDP
MDP_SR8FRM	I/O	×	—	4mA	Serial Interface Frame signal from MDP
MDM_GPIO[15]	I/O	✓			General Purpose Input/Output for Modem Function
MDM_SDXTAL1	I	×	—	—	28.224 MHz clock for running Modem interface Should be tied to clock output of MDP or an oscillator
MDM_SDXTAL2	O				
MDP_DATA[7:0]					
MDM_OSC_OUT	O				
MDP_ADDR[1:0]					

LAN Flash ROM Interface Signals

Pin Name	Type	Schmitt	Resistive	Drive	Description
FROM_CS#	O	—	—	2ma	Flash ROM Chip Select

7-Wire Serial Interface Signals

Pin Name	Type	Schmitt	Resistive	Drive	Description
7WS_TX_CLK *multiplexed signal* *8023_MII_TX_CLK*	I	×	—	—	Transmit Clock Transmit Clock from Physical Layer (PHY) to MAC. Provided as a clock for MAC activity. The rising edges may be used to validate 7WS_TXD.
7WS_TXD *multiplexed signal* *8023_MII_TXD[3]*	O	—	—	2ma	Transmit Data Transmit Data bus from the MAC to the PHY. 7WS_TXD is a bit provided by the MAC synchronously with 7WS_TX_CLK. The bit stream includes preamble, SFD, data and CRC, if enabled.
7WS_TX_EN *multiplexed signal* *8023_MII_TX_EN*	O	—	—	2ma	Transmit Enable Transmit Enable indicator from MAC to PHY indicates that valid data is being presented on 7WS_TXD. 7WS_TX_EN is synchronized with the 7WS_TX_CLK and is sampled synchronously with 7WS_TX_CLK by the PHY. The 7WS_TX_EN is asserted by the MAC on the first byte of the preamble and remains asserted until the last bit of the frame is transferred.
7WS_CRS *multiplexed signal* *8023_MII_CRS*	I	×	—	—	Carrier Sense Provided by the PHY to indicate that Carrier is currently present on the physical media. If this signal is high it indicates that valid data is available on 7WS_RXD or you are transferring in half-duplex mode.
7WS_COL *multiplexed signal* *8023_MII_COL*	I	×	—	—	Collision Indication Provided by the PHY to indicate that a collision has been detected on the physical media.
7WS_RX_CLK *multiplexed signal* *8023_MII_RX_CLK*	I	×	—	—	Receive Clock A recovered clock provided to the MAC synchronously with 7WS_RXD. If 7WS_RX_DV is high, 7WS_RXD is sampled on the rising edges of this clock.
7WS_RXD *multiplexed signal* *8023_MII_RXD[3]*	I	×	—	—	Receive Data Receive Data bus from the PHY to the MAC. 7WS_RXD is accepted by the MAC for each clock period of 7WS_RX_CLK while 7WS_RX_EN is asserted. 7WS_RXD is a bit which is provided by the PHY synchronously with 7WS_RX_CLK. If 7WS_RX_DV is high, 7WS_RXD is sampled on the rising edges of 7WS_RX_CLK.

Media Independent Interface (MII)[8]

Pin Name	Type	Schmitt	Resistive	Drive	Description
8023_MII_TX_CLK *multiplexed signal* *7WS_TX_CLK*	I	×	—	—	Transmit Clock Transmit Clock from Physical Layer (PHY) to MAC This clock is provided by the PHY as a reference for the MAC. At both 10 Mbps and 100 Mbps, the permissible duty cycle is between 40% to 60%. The nominal case is 50% 25 MHz ± 100 PPM in 100 Mbps mode 2.5 MHz ± 100 PPM in 10 Mbps mode
8023_MII_TXD[3] *multiplexed signal* *7WS_TXD*	O	—	—	2ma	Transmit Data Transmit data bus from the MAC to the PHY. 8023_MII_TXD are provided for transmission for each clock period 0f 8023_MII_TX_CLK while 8023_MII_TX_EN is asserted. 8023_MII_TXD[3:0} is a 4-bit data nibble which is provided by the MAC synchronously to 8023_MII_TX_CLK.
8023_MII_TXD[2]	O	—	—	2ma	
8023_MII_TXD[1]	O	—	—	2ma	
8023_MII_TXD[0]	O	—	—	2ma	
8023_MII_TX_EN *multiplexed signal* *7WS_TX_EN*	O	—	—	2ma	Transmit Enable Transmit Enable indicator from MAC to PHY indicates that valid 4-bit nibble of data is being presented at 8023_MII_TXD[3:0]. 8023_MII_TX_EN is synchronized with the 8023_MII_TX_CLK and is sampled synchronously with 8023_MII_TX_CLK by the PHY. The 8023_MII_TX_EN is asserted by the MAC on the first byte of the preamble and remains asserted until the last nibble/bit of the frame is transferred.
8023_MII_TX_ER	O	—	—	2ma	Transmit Error Used by the MAC to indicate to the PHY that a coding or transmit underrun error has occurred. Transmit Error is asserted synchronously to 8023_MII_TX_CLK while 8023_MII_TX_EN is asserted to indicate a Transmit Coding Error or transmit underrun of a frame. It is intended to provide a frame abort mechanism and shall cause the PHY to emit one or more ABORT control symbols. The ABORT control symbol is not a valid symbol for Ethernet, therefore, the receiving MAC will recognize the invalid control symbol and indicate a receive error at the receiving end.
8023_MII_MDC	O	—	—	2ma	Management Data Clock Clock for Serial Management Interface (SMI). Software provides 8023_MII_MDC to the PHY as a reference clock. It is used in conjunction with the 8023_MII_MDIO signal for reading or writing Link Management or Operation information to and from the PHY.
8023_MII_MDIO	I/O	×	—	2ma	Serial Management Data Input/Output I/O signal for SMI. This pin is used to read/write data to/from the PHY. Data is synchronized with 8023_MII_MDC. When connecting the MAC to an MII connector instead of a PHY, an external 1.5k ohm pull-up resistor is recommended for this line to allow the attached MAC to determine the attachment of a PHY.
8023_MII_CRS *multiplexed signal* *7WS_CRS*	I	×	—	—	Carrier Sense Provided by the PHY to indicate that Carrier is currently present on the physical media.
8023_MII_COL *multiplexed signal*	I	×	—	—	Collision indication Provided by the PHY to indicate that a collision has been detected on the physical media.

[8] See IEEE 802.3u Section 22

Pin Name	Type	Schmitt	Resistive	Drive	Description
7WS_COL					
8023_MII_RX_DV	I	×	↓	—	Receive data valid Provided by the PHY to indicate to the MAC that a valid 4-bit nibble of data is available on 8023_MII_RXD[3:0]. 8023_MII_RX_DV is synchronized with 8023_MII_RX_CLK by the PHY and is sampled synchronously with 8023_MII_RX_CLK by the MAC. 8023_MII_RX_DV is asserted by the PHY on the first nibble of the preamble and remains asserted until the last nibble of the frame, excluding any end of frame delimiter, is transferred from the PHY to the MAC.
8023_MII_RX_ER	I	×	—	—	Receive Error Produced by the PHY to indicate that it has detected an error in the current packet. This signal is only valid when 8023_MII_RX_DV is asserted.
8023_MII_RX_CLK *multiplexed signal* *7WS_RX_CLK*	I	×	—	—	Receive Clock Produced by PHY as a timing reference for 8023_MII_RX_DV, 8023_MII_RXD, and 8023_MII_RX_ER signals. The permissible duty cycle is between 35% and 65% inclusive. The nominal case is 50%. 25 MHz ± 2500 Hz in 100 Mbps mode 2.5MHz ± 250Hz in 10 Mbps mode 8023_MII_RX_CLK and 8023_MII_TX_CLK may be referenced from the same source.
8023_MII_RXD[3] *multiplexed signal* *7WS_RXD*	I	×	—	—	Receive Data Receive Data bus from the PHY to the MAC. 8023_MII_RXD[3:0] are accepted by the MAC for each clock period of 8023_MII_RX_CLK while 8023_MII_RX_EN is asserted. 8023_MII_RXD[3:0] is a 4-bit data nibble which is provided by the PHY synchronously to 8023_MII_RX_CLK.
8023_MII_RXD[2]	I	×	—	—	
8023_MII_RXD[1]	I	×	—	—	
8023_MII_RXD[0]	I	×	—	—	

IEEE 802.3 Fast Ethernet Signals

Pin Name	Type	Schmitt	Resistive	Drive	Description
LAN_GPIO[0]	I/O	×	↓	4mA	LAN Function General Purpose I/O pin May be individually configured for input/output using the LAN_GPIO register. If configured for input it can generate level sensitive hardware interrupts. May be used to reset peripheral devices that require active high reset.

Serial EEPROM Interface Signals

Pin Name	Type	Schmitt	Resistive	Drive	Description
EEPROM_DOUT *multiplexed signal SPI_DOUT*	O	—	—	2ma	EEPROM Data Output Data is read from an external EEPROM on this pin. The pin must have a 10K pull-up or pull-down attached on the board. Pulling the pin low (logical 0) will cause the MAC to skip the EEPROM Read process after a PCI RST# is de-asserted. See the LANfinity Software Designer's Guide's documentation on the LAN Serial Port Register for information on driving this signal using software.
EEPROM_DIN *multiplexed signal SPI_DIN*	I	×	—	—	EEPROM Data Input Data is written to an EEPROM device using this pin. This pin requires a 51K pull-down on the adapter. See the LANfinity Software Designer's Guide's documentation on the LAN Serial Port Register for information on driving this signal using software.
EEPROM_CS	O	—	—	2ma	EEPROM Chip Select This pin acts as the Chip Select for an external EEPROM. Refer to the RS7xxx Software Design Guide documentation on the LAN Serial Port Register for information about driving this signal using software. Note: This pin requires a 51K pull-down on the adapter
EEPROM_CLK *multiplexed signal SPI_CLK*	O	—	—	2ma	EEPROM Clock This pin serves as the clock for an external EEPROM. Following a reset of the device, the MAC controls the duty cycle during the automatic read process. Software is responsible for generating the clock during any reading or programming of the EEPROM. This pin requires a 51K pull-down on the adapter. See the LANfinity Software Designer's Guide's documentation on the LAN Serial Port Register for information on driving this signal using software. During the automatic read from EEPROM the CMAC will use the clock rate indicated: VCC Clock 5V 2 MHz 3.3V 1 MHz Refer to the EEPROM device's data sheet to determine the maximum clock rate the device can support.

Test Signals

Pin Name	Type	Schmitt	Resistive	Drive	Description
SCANMODE	I	×	↓	—	**Selects different scan modes**
SCANENB	I	×	↓	—	**Scan enable (1 = enable scan)**

Power Pins

Pin Name	Type	Characteristic	Description
VDD	P	3V	3.3 Volt Power
GND	G	GND	Ground
VGG	P	5V	5 V - attach to 5 V clamping during 3.3 V operation

Electrical Characteristics

176-pin TQFP

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{DD}		3.3		V
Input Voltage	V_{IN}		TBD		V
Operating Temperature Range	T	0	TBD	+70	^oC
Storage Temperature	T_{stg}	-65	TBD	+150	^oC
Voltage Applied to Outputs in High Z state	V_{hz}	-0.5	TBD	TBD	V
DC Input Clamp Current	I_{lk}	-20	TBD	+20	mA
DC Input Clamp Current	I_{ok}	-20	TBD	+20	mA
Static Discharge Voltage (25 ^oC)	ESD	-2500	TBD	+2500	V
Latch-up Current	I_{trig}	-400	TBD	+400	mA

Table 6. DC Electrical Characteristics

T_A = 0^{o}C to +70^{o}C, V_{DD} = +3.3V ± 5%, V_{SS} = 0V.

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{DD}		3.3		V
Input Voltage	V_{IN}		TBD		V
Operating Temperature Range	T	0	TBD	+70	^oC
Storage Temperature	T_{stg}	-65	TBD	+150	^oC
Voltage Applied to Outputs in High Z state	V_{hz}	-0.5	TBD	TBD	V
DC Input Clamp Current	I_{lk}	-20	TBD	+20	mA
DC Input Clamp Current	I_{ok}	-20	TBD	+20	mA
Static Discharge Voltage (25 ^oC)	ESD	-2500	TBD	+2500	V
Latch-up Current	I_{trig}	-400	TBD	+400	mA

Table 7. AC Electrical Characteristics

TA = 0°C to +70°C, VDD = +3.3V ± 5%, VSS = 0V.

Parameter	Symbol	Min	Typ	Max	Units
Frequency (PCI_CLK)	F_{pck}	25	33	33	MHz
Frequency (8023_MII_TX_CLK) 100 Mbps	F_{xtal}	25	25	25	MHz
Frequency (8023_MII_RX_CLK) 100 Mbps	TBD	25	25	25	MHz
Frequency (8023_MII_TX_CLK) 10 Mbps	TBD	2.5	2.5	2.5	MHz
Frequency (8023_MII_RX_CLK) 10 Mbps	TBD	2.5	2.5	2.5	MHz
Frequency (8023_MII_MDC)	TBD	0	2.5	2.5	MHz

Note: Setup, Hold and Delays are with respect to the rising edge of the respective clock unless specified. PCI Bus signals conform to the PCI Bus Timing Specification.

Table 8. Current and Power Characteristics

Mode	Typical Current (mA)	Maximum Current (mA)	Typical Power (W)	Maximum Power (W)	Notes
Active	TBD	TBD	TBD	TBD	
Idle	TBD	TBD	TBD	TBD	
Power down	TBD	TBD	TBD	TBD	

13 mm BGA - TBD

Table 9. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{DD}				V
Input Voltage	V_{IN}				V
Operating Temperature Range	T				^oC
Storage Temperature	T_{stg}				^oC
Voltage Applied to Outputs in High Z state	V_{hz}				V
DC Input Clamp Current	I_{lk}				mA
DC Input Clamp Current	I_{ok}				mA
Static Discharge Voltage (25 °C)	ESD				V
Latch-up Current	I_{trig}				mA

Table 10. DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +3.3V ± 5%, V_{SS} = 0V.

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{DD}				V
Input Voltage	V_{IN}				V
Operating Temperature Range	T				^oC
Storage Temperature	T_{stg}				^oC
Voltage Applied to Outputs in High Z state	V_{hz}				V
DC Input Clamp Current	I_{lk}				mA
DC Input Clamp Current	I_{ok}				mA
Static Discharge Voltage (25 °C)	ESD				V
Latch-up Current	I_{trig}				mA

Table 11. AC Electrical Characteristics

TA = 0°C to +70°C, VDD = +3.3V ± 5%, VSS = 0V.

Parameter	Symbol	Min	Typ	Max	Units
Frequency (PCI_CLK)	F_{pck}				MHz
Frequency (8023_MII_TX_CLK) 100 Mbps	F_{xtal}				MHz
Frequency (8023_MII_RX_CLK) 100 Mbps					MHz
Frequency (8023_MII_TX_CLK) 10 Mbps					MHz
Frequency (8023_MII_RX_CLK) 10 Mbps					MHz
Frequency (8023_MII_MDC)					MHz

Note: Setup, Hold and Delays are with respect to the rising edge of the respective clock unless specified. PCI Bus signals conform to the PCI Bus Timing Specification.

Table 12. Current and Power Characteristics

Mode	Typical Current (mA)	Maximum Current (mA)	Typical Power (W)	Maximum Power (W)	Notes
Active					
Idle					
Power down					

Package Dimensions

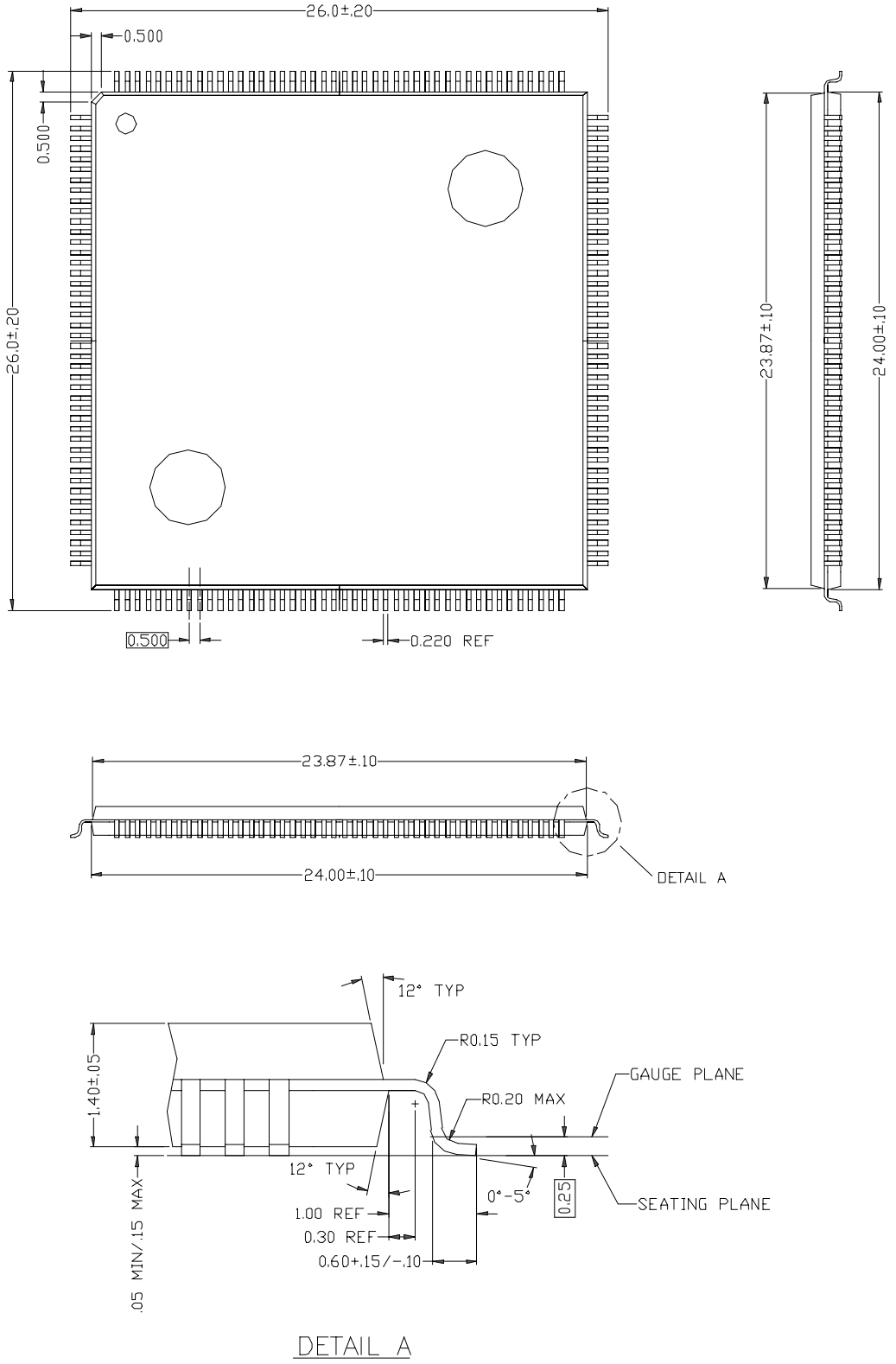
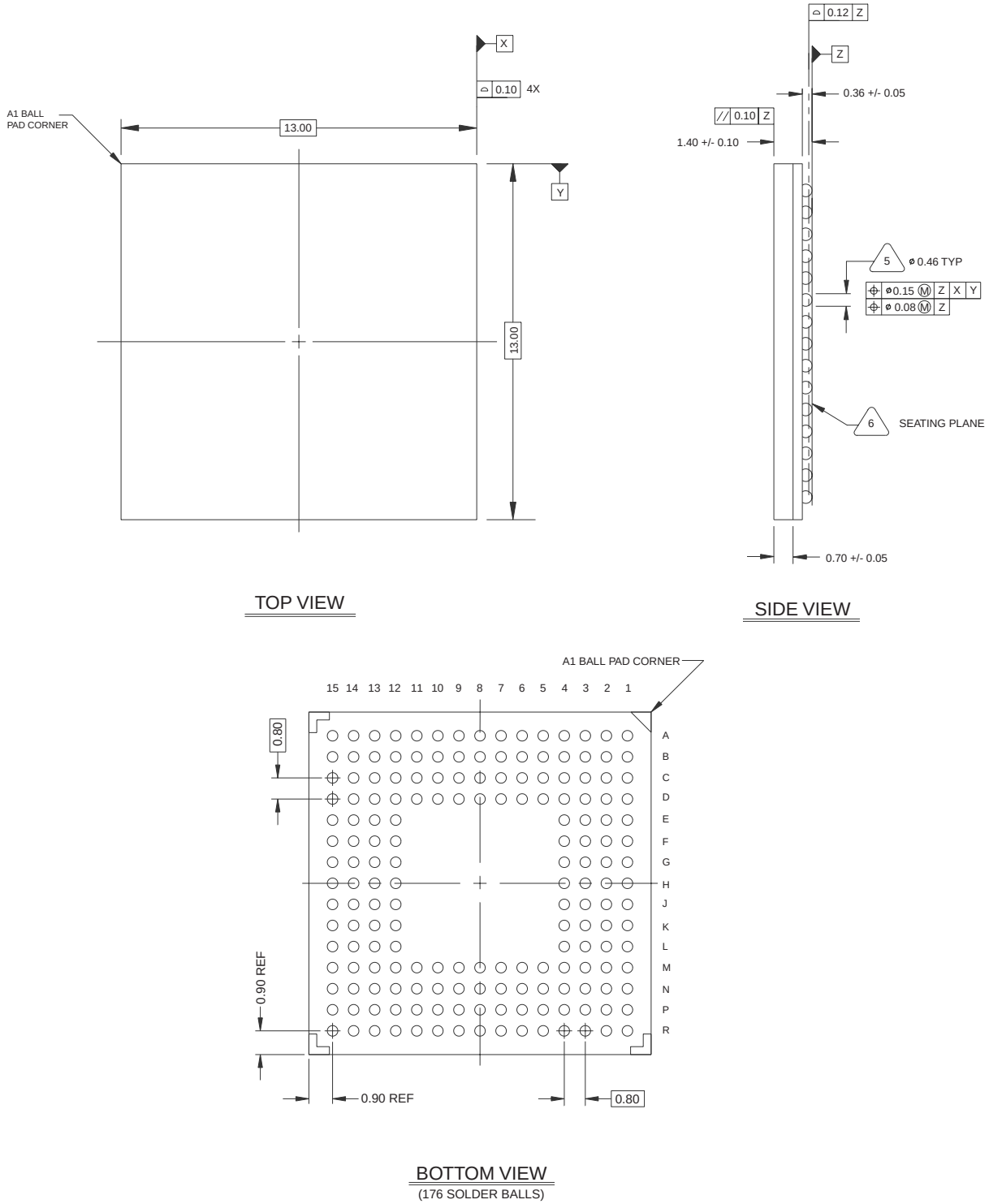


Figure 6. 176-Pin TQFP Package Dimensions



All dimensions in millimeters

Figure 7. 13 mm BGA Package Dimensions

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