S6B2104

80CH SEGMENT DRIVER FOR DOT MATRIX LCD

July. 2001

Ver. 0.0

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.

2. Always test and inspect products under the environment with no penetration of light.

S6B2104 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	July.2001

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CONTENTS

INTRODUCTION

The S6B2104 is a LCD driver IC which is fabricated by low power CMOS high voltage process technology. This device consists of 80 bit bi-directional shift register, 80 bit data latch and 80 bit driver.
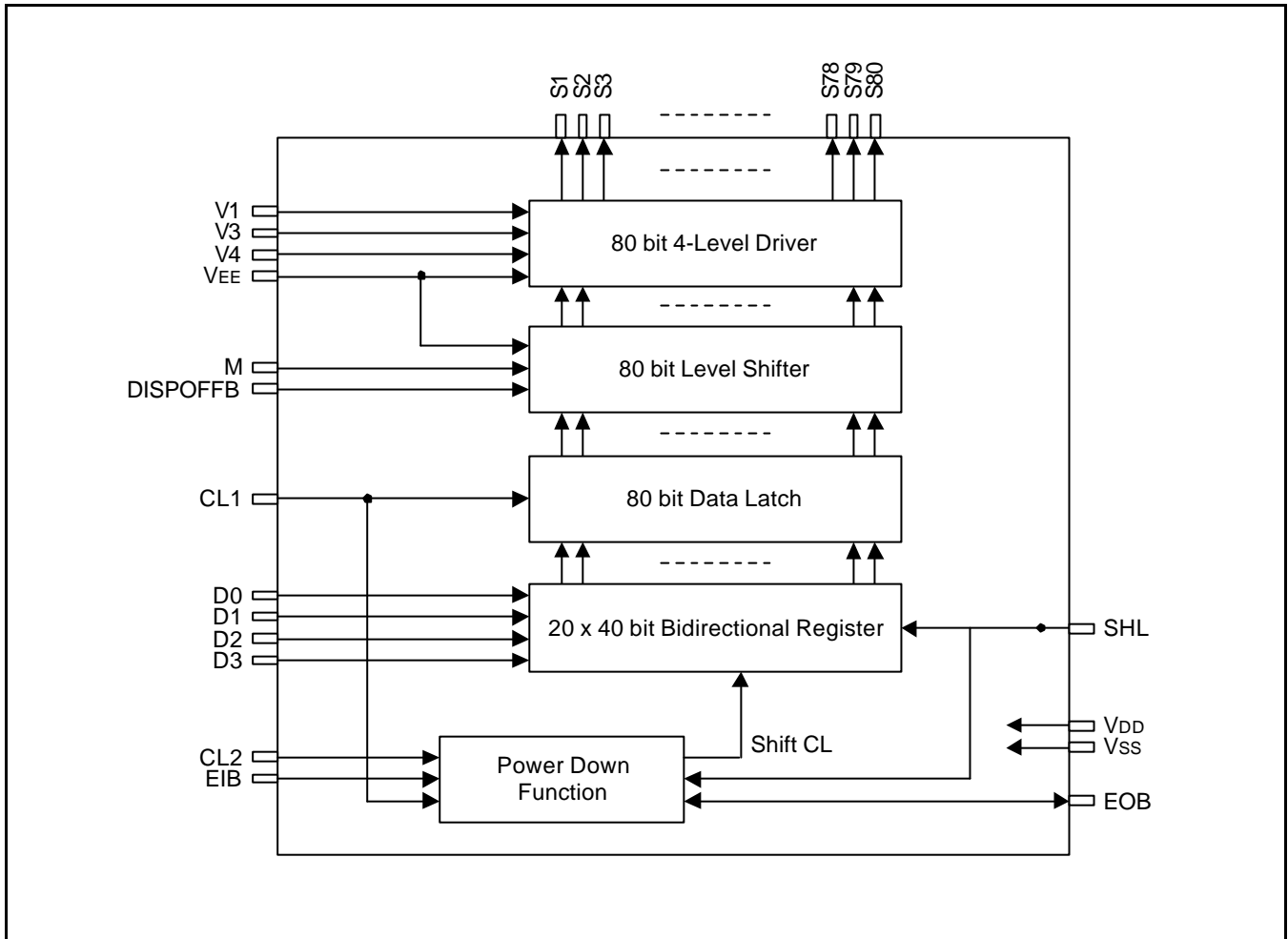
FEATURES

— Power supply voltage: +5V $\pm$ 10%, +3V $\pm$ 10%

— Supply voltage for display: 6 to 28V (V_{DD}-V_{EE})

— Parallel data processing (4 bit)
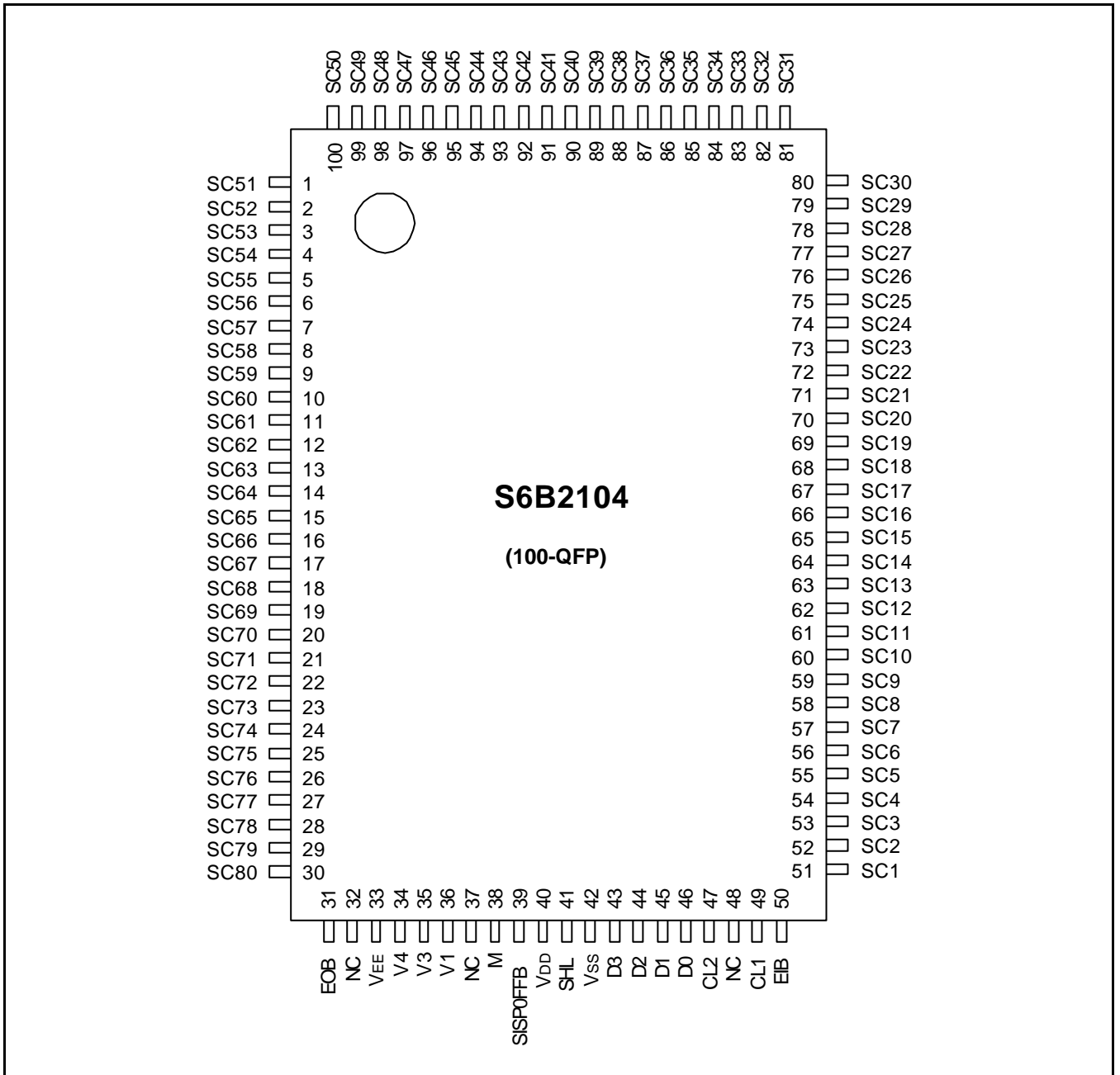
— Applicable LCD duty: 1/64 to 1/256

— Interface

Drivers	
COM	SEG (cascade)
S6B0086	Other S6B2104

— High voltage CMOS process

— 100 QFP or bare chip available

BLOCK DIAGRAM

PIN CONFIGURATION

Left pins		Right pins	
SC51	1	80	SC30
SC52	2	79	SC29
SC53	3	78	SC28
SC54	4	77	SC27
SC55	5	76	SC26
SC56	6	75	SC25
SC57	7	74	SC24
SC58	8	73	SC23
SC59	9	72	SC22
SC60	10	71	SC21
SC61	11	70	SC20
SC62	12	69	SC19
SC63	13	68	SC18
SC64	14	67	SC17
SC65	15	66	SC16
SC66	16	65	SC15
SC67	17	64	SC14
SC68	18	63	SC13
SC69	19	62	SC12
SC70	20	61	SC11
SC71	21	60	SC10
SC72	22	59	SC9
SC73	23	58	SC8
SC74	24	57	SC7
SC75	25	56	SC6
SC76	26	55	SC5
SC77	27	54	SC4
SC78	28	53	SC3
SC79	29	52	SC2
SC80	30	51	SC1

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(100-QFP)

Top pins (100–81): SC50, SC49, SC48, SC47, SC46, SC45, SC44, SC43, SC42, SC41, SC40, SC39, SC38, SC37, SC36, SC35, SC34, SC33, SC32, SC31

Bottom pins (31–50): EOB, NC, V$_{EE}$, V4, V3, V1, NC, M, SISP0FFB, V$_{DD}$, SHL, V$_{SS}$, D3, D2, D1, D0, CL2, NC, CL1, EIB

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit
Operating voltage	V_{DD}	-0.3 - 6.0	V
Driver supply voltage	V_{LCD}	0 - 30	
Input voltage	V_{IN}	-0.3 - V_{DD} +0.3	
Operating temperature	T_{OPR}	-30 - +85	°C
Storage temperature	T_{STG}	-55 - +150	

Voltage greater than above may result in damage to the circuit.
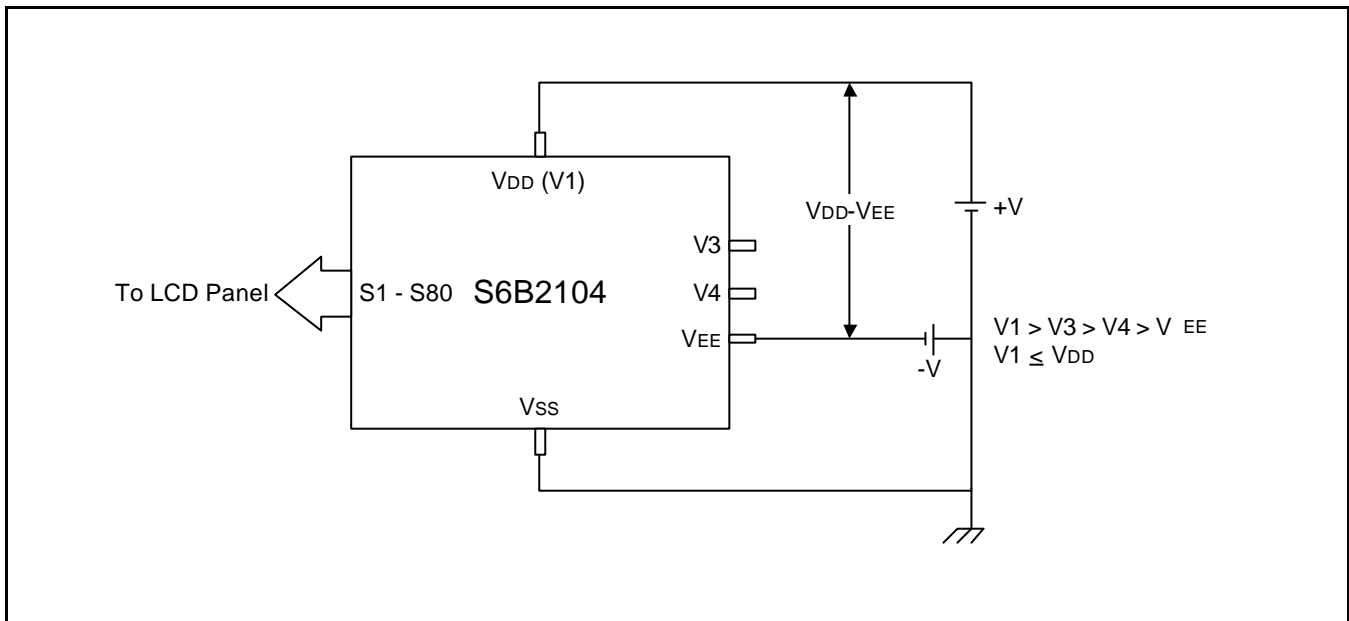
ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 5.5V, V_{SS} = 0V, Ta = -30 to +85°C, C_L = 15pF)

Characteristics	Symbol	Condition		Min	Typ	Max	Unit
Operating voltage	V_{DD}	-		2.7	-	5.5	V
Driver supply voltage	V_{LCD}	V_{LCD}= V_{DD} - V_{EE}		6	-	28	
Input voltage [1]	V_{IH}	-		$0.8V_{DD}$	-	-	
	V_{IL}	-		0	-	$0.2V_{DD}$	
Output voltage [2]	V_{OH}	I_{OH} = -0.4mA		V_{DD}-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 [1]	I_{IL1}	V_{IN} = V_{DD} to V_{SS}		-1	-	1	µA
Input leakage current 2 [3]	I_{IL2}	V_{IN} = V_{DD} to V_{EE}		-25	-	25	
On resistance [4]	R_{ON}	I_{ON} = 100µA		-	2	4	kΩ
Supply current	I_{STB}	f_{CL2} = 1MHz,	V_{DD} = 5.5V [5]	-	-	200	µA
	I_{DD}	f_{CL2} = 19.2kHz,	V_{DD} = 5.5V [6]	-	-	3	mA
		f_M = 40Hz, V_{LCD} = 26V	V_{DD} = 2.7V [6]	-	-	1	mA
	I_{EE}	No Load	V_{DD} = 5.5V [7]	-	150	500	µA

NOTES:

1. Applied to CL1, CL2, EIB, EOB, D0 to D3, SHL, DISPOFFB, M pin.
2. EIB, EOB pin
3. V1, V3, V4 pin
4. V_{DD}-V_{EE} = 26V(V_{DD} = 3V), V_{EE} = 28V(V_{DD} = 5V), V1 = V_{DD}, V3 = V_{DD}-2/10(V_{DD}-V_{EE}), V4 = V_{EE}+2/10(V_{DD}-V_{EE}), S1 to S80 pin
5. Display data pattern: 0000, Current from V_{DD} to V_{SS} when the display data is not processing (SHL = V_{SS}, D0 to D3 = V_{SS}, DISPOFFB = V_{DD}, M = V_{SS})
6. Display data pattern: 1010, Current from V_{DD} to VSS when the display data is processing
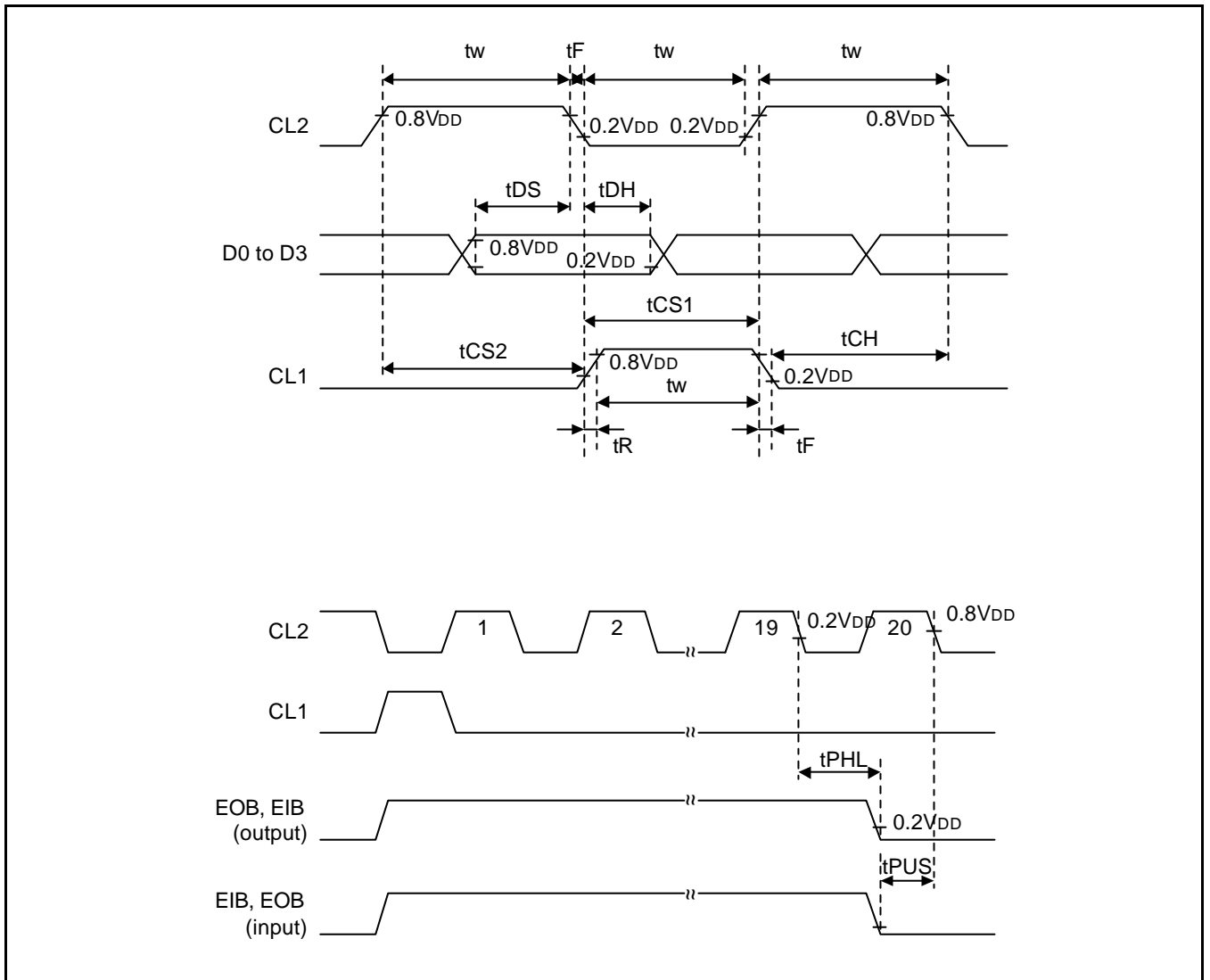7. Display data pattern: 1010, Current on V_{EE} pin

AC Characteristics

(V_{DD} = +5V $\pm$ 10%, V_{SS} = 0V, Ta = -30 to + 85 $^{\circ}$C, C_L = 15pF)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Clock cycle time	t_{CYC}	Duty = 50%	125	-	-	ns
Clock pulse width	t_W	-	45	-	-	
Clock rise/fall time	t_R/t_F	-	-	-	30	
Data set-up time	t_{DS}	-	30	-	-	
Data hold time	t_{DH}	-	30	-	-	
Clock set-up time1	T_{CS1}	-	80	-	-	
Clock set-up time2	T_{CS2}	-	10	-	-	
Clock hold time	t_{CH}	-	80	-	-	
Propagation delay time	t_{PHL}	EOB output	-	-	80	
		EIB output			80	
EIB, EOB set-up time	t_{PSU}	EOB input	30	-	-	
		EIB input	30			

(V_{DD} = +3V $\pm$ 10%, V_{SS} = 0V, Ta = -30 to + 85°C, C_L = 15pF)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Clock cycle time	t_{CYC}	Duty = 50%	250	-	-	ns
Clock pulse width	t_W	-	95	-	-	
Clock rise/fall time	t_R/t_F	-	-	-	30	
Data set-up time	t_{DS}	-	50	-	-	
Data hold time	t_{DH}	-	50	-	-	
Clock set-up time1	T_{CS1}	-	80			
Clock set-up time2	t_{CS2}	-	15	-	-	
Clock hold time	t_{CH}	-	120	-	-	
Propagation delay time	t_{PHL}	EOB output	-	-	155	
		EIB output			155	
EIB, EOB set-up time	t_{PSU}	EOB input	65	-	-	
		EIB input	65			

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Timing Characteristics

PIN DESCRIPTION

Table 1. Pin Description

Pin No	I/O	Name	Function	Interface
V_{DD} (40)	Power	Operating voltage	For logical circuit (+5V ± 10%, +3V ± 10%)	Power Supply
V_{SS} (42)			0V (GND)	
V_{EE} (33)		Negative supply voltage	For LCD drive circuit	
V1, V3, V4 (34-36)	I	LCD driver output voltage level	Bias supply voltage terminals to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source. (refer to note 1)	Power
S1-S80 (1-30, 51-100)	O	LCD driver output	Display data output pin which corresponds to the respective latch contents. One of V1, V3, V4 and V_{EE} is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to note 2)	LCD
CL2 (47)	I	Data shift clock	Clock pulse input for the 4 bit parallel shift register. The data is shifted to 80 bit shift register at the falling edge of the clock pulse. The clock pulse, which was input when the enable bit (EIB/EOB) is not active condition, is invalid.	Controller
M (38)	I	Alternate signal for LCD driver output	Alternate signal input pin for LCD driving. Normal frame inversion signal is input	Controller
CL1 (49)	I	Data latch clock	The signal for latching the shift register contents is input to this terminal. CL1 pulse "H" level initializes power-down function block.	Controller
DISPOFFB (39)	I	Output level control (Display off)	Control input pin for display data output level (S1-S80). V1 level is output from S1-S80 terminal during "L" level input. LCD becomes non-selected by V1 level output from every output of segment drivers and every output of common drivers.	Controller
SHL (41)	I	Data shift control	EOB and EIB can be used as either input terminal or output terminal according to the condition of SHL. The shifting direction of each data, D0-D3, the I/O condition of EOB and EIB, and the condition of SHL are described in the table below. (refer to note 3).	V_{DD}/V_{SS}

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Table 1. Pin Description (Continued)

Pin No	I/O	Name		Function			Interface
		Pin	I/O	SHL	Display data shift direction	Description	
Eob, Eib (31,50)	I/O	EOB	I	L	D0: S1→S5...→ S77	Enable input terminal of S6B2104.	
		EIB	O		D1: S2→S6...→S78 D2: S3→S7...→S79 D3: S4→S8...→S80	Enable output terminal of S6B2104. EIB is connected to next S6B2104's EOB when the S6B2104's are connected in series (cascade connection).	
		EIB	I	H	D0: 80→S76...→S4	Enable input terminal of S6B2104.	
		EOB	O		D1: 79→S75...→S3 D2: 78→S74...→S2 D3: 77→S73...→S1	Enable output terminal of S6B2104. EOB is connected to next S6B2104's EIB when the S6B2104's are connected in series (cascade connection)	
D0-D3 (43-46)	I	EOB	I	L			
		EIB	O				
		EIB	I	H			
		EOB	O				
		Display data input		Display data input pins for 4 bit parallel shift register and it is input synchronized with the clock pulse. The combination of D0-D3 level, M signal, display data output level and the display on the LCD panel is described on the table below. (DISPOFFB = H)			Controller

D0-D3	M	Display Data Output Level	Display on the LCD
L	L	V3	OFF
H	L	V1	ON
L	H	V4	OFF
H	H	V$_{EE}$	ON

NOTES:

1.

V1, V EE	Selected Level
V3, V4	Nonselected Level

n = 5 (1/64 duty) to 13 (1/256 duty)

2.

M	Latched Data	DISPOFFB	Output level (S1 - S80)
L	L	H	V3
L	H	H	V1
H	L	H	V4
H	H	H	V_{EE}
X	X	L	V1

"X" is don't care.

3. – EOB and EIB pins works as input terminals.
      ENABLE F/F stops display data at "H" level input. ENABLE F/F starts display data at "L" level input.
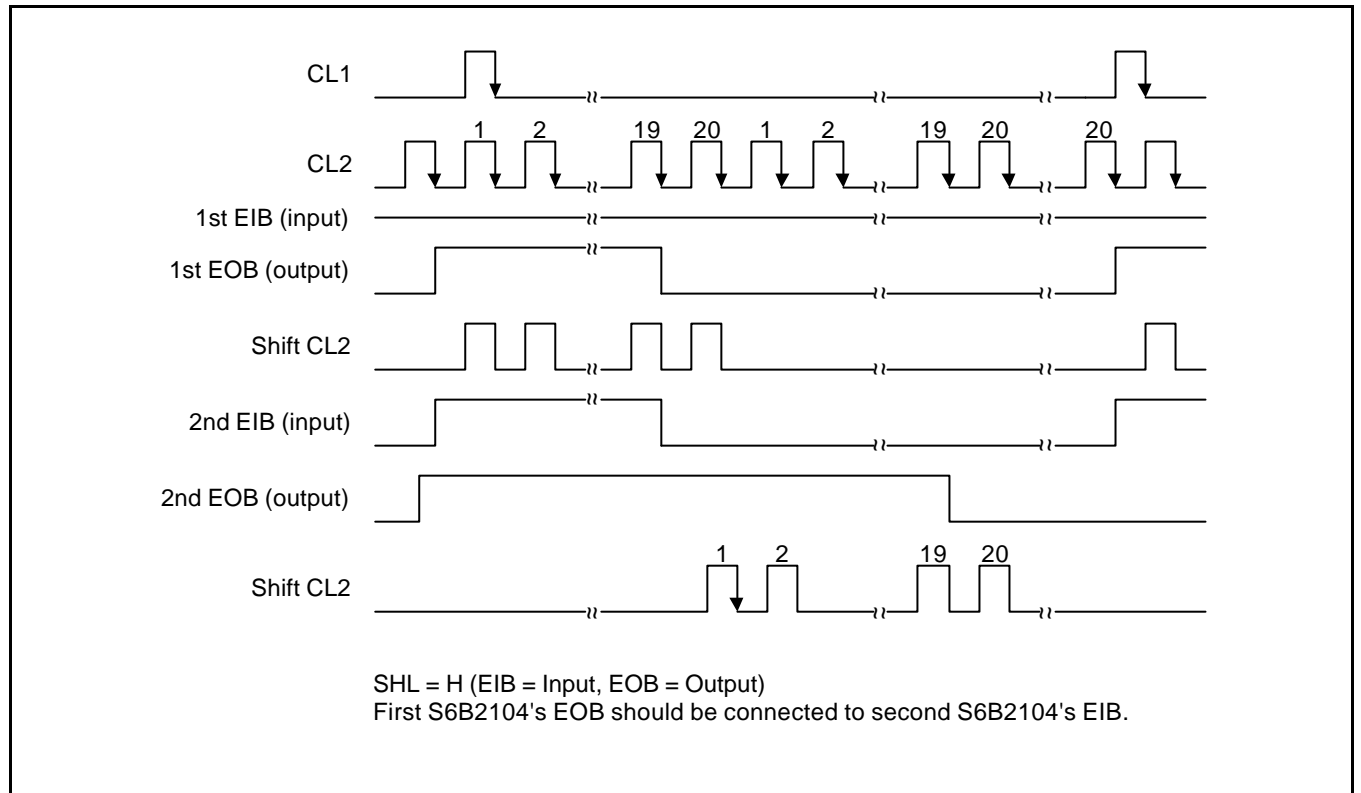   – EOB and EIB pins work as output terminals. These terminals are set to the "H" level immediately after ENABLE F/F is
      initialized by the load pulse. Upon completion of 80-bit serial/parallel conversion using the shift clock input from the
      CL2 terminal, these terminals are then set to the "L" level.
    – The operation of ENABLE F/F is terminated and held unchanged until the next load pulse is detected. (For cascade
      connection, refer to the application circuit drawing)

POWER DOWN FUNCTION

In order to reduce the power consumption, in case of cascade connection, S6B2104 has a "power down function".

EIB	Enable input	Enable	L
		Disable	H
EOB	Enable output	EOB of Nth driver is connected to EIB of (N+1)th driver S6B2104	

SHL = H (EIB = Input, EOB = Output)
First S6B2104's EOB should be connected to second S6B2104's EIB.

Timing Chart - 1/200 Duty, 1/15 Bias

$$V1 = V_{DD}$$
$$V2 = V_{DD}-1/10V_{LCD} \qquad V3 = V_{DD}-2/10V_{LCD}$$
$$V4 = V_{DD}-8/10V_{LCD} \qquad V5 = V_{DD}-9/10V_{LCD} \qquad V_{LCD} = V_{DD}\,V_{EE}$$

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