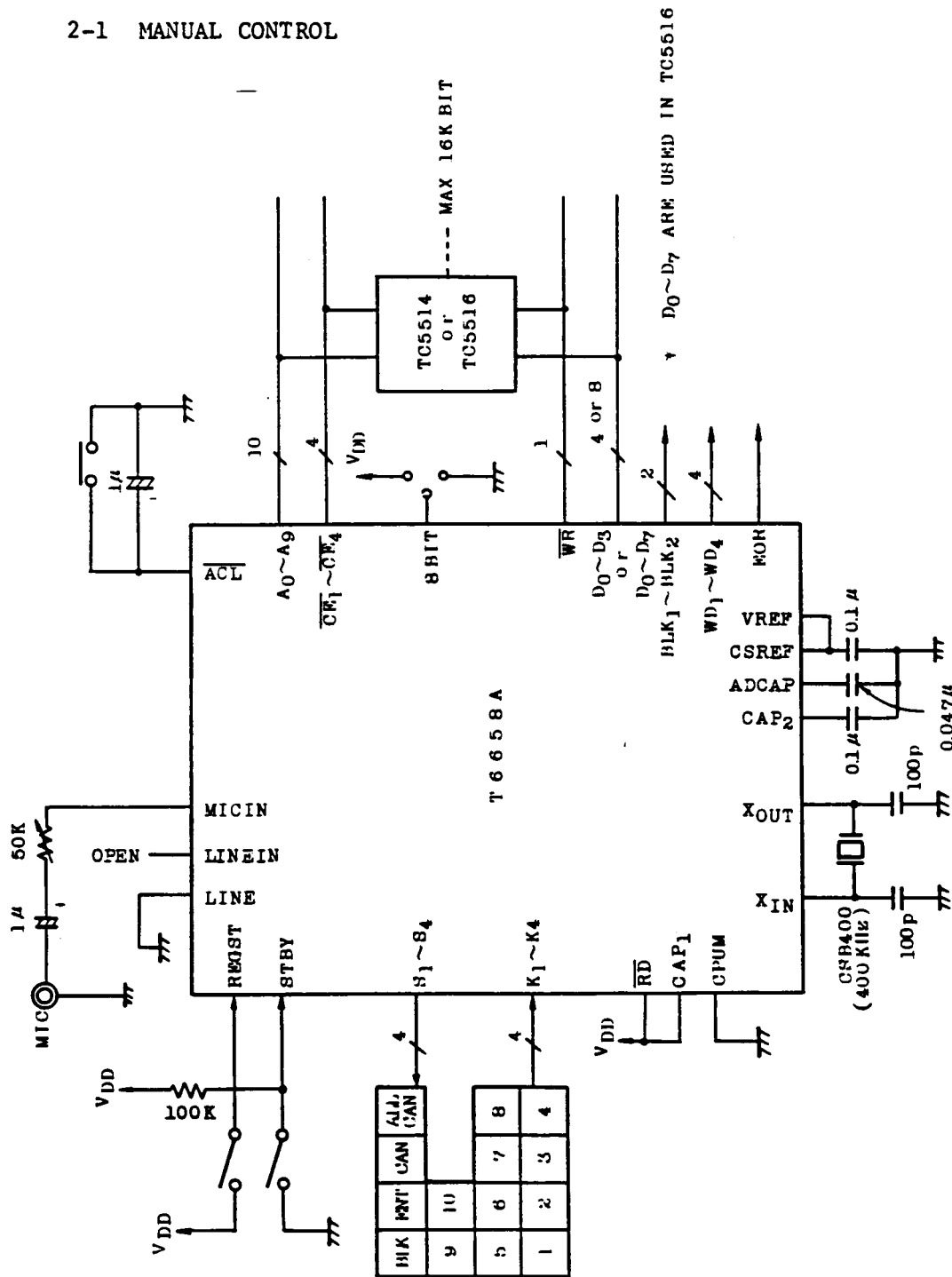


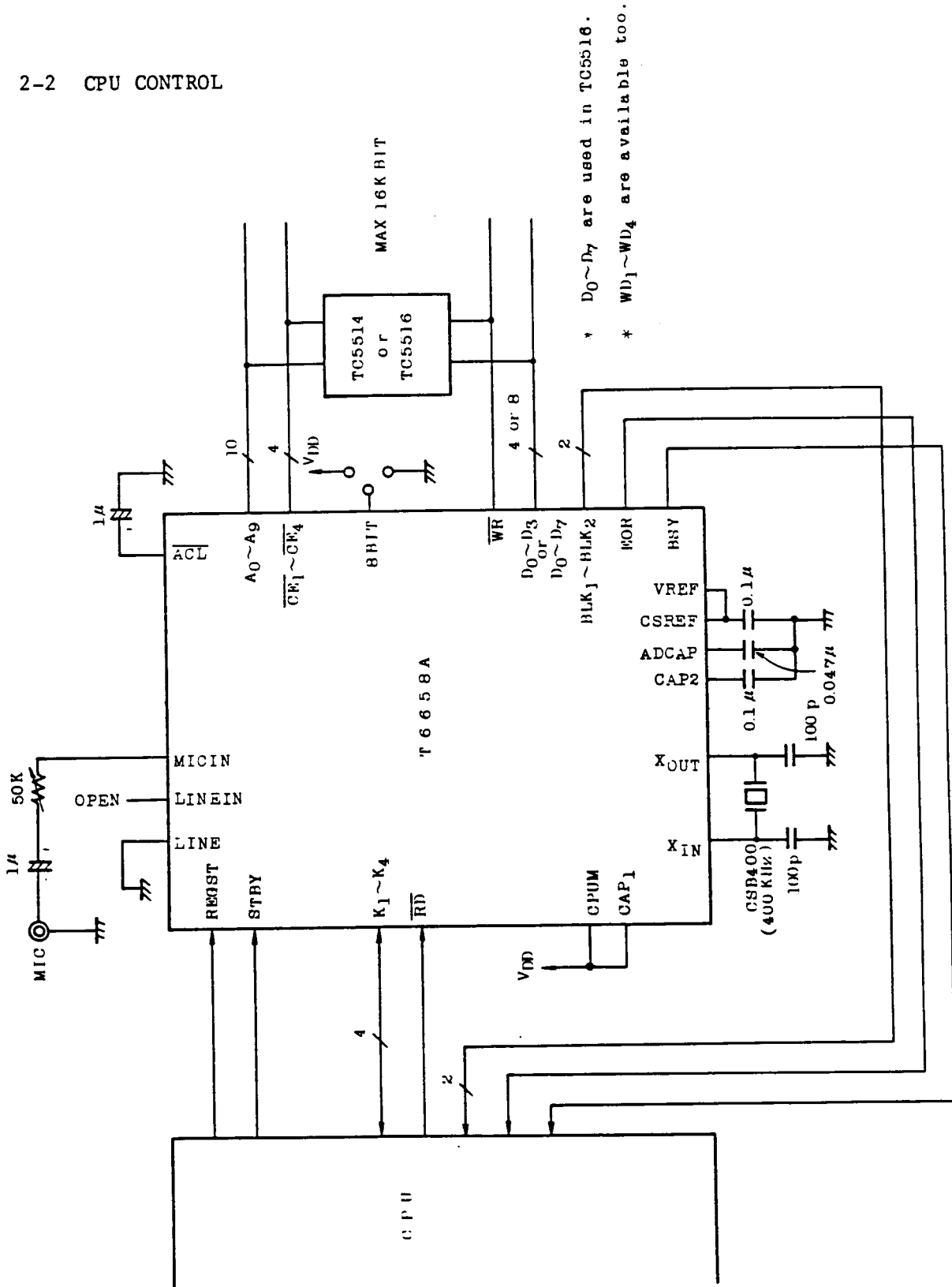


2. Example of System Configuration

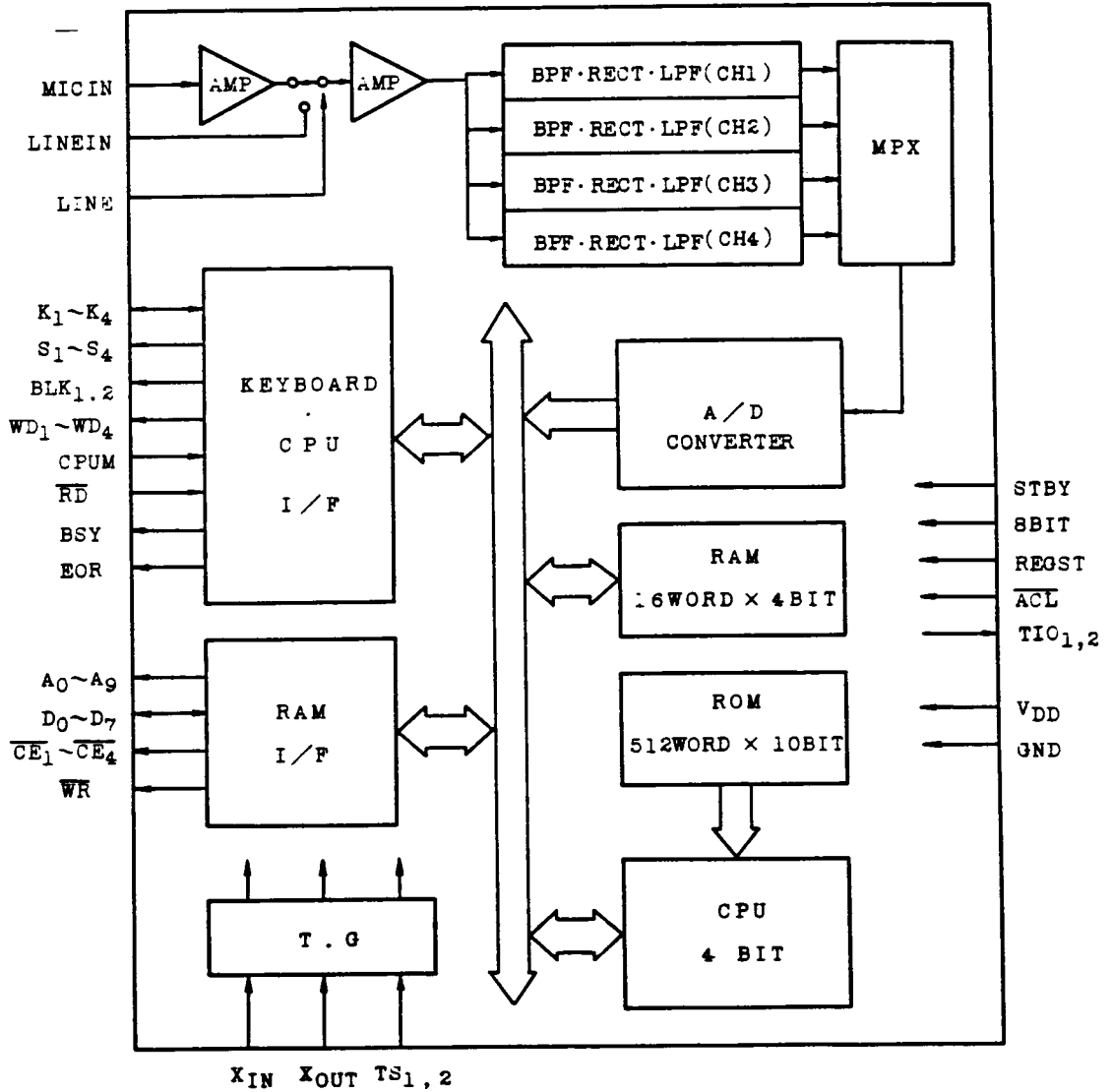
2-1 MANUAL CONTROL



### 2-2 CPU CONTROL



3. T6658A BLOCK DIAGRAM



4. Specifications

4-1 Recognition part

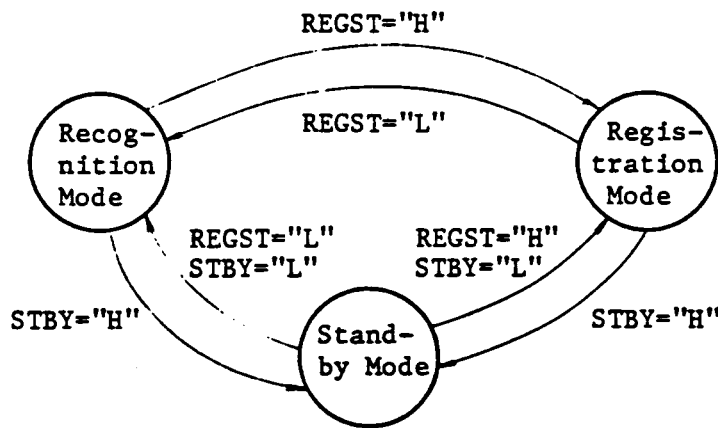
Recognition method	Speaker dependent word recognition
Voice analysis	4 channel - B.P.F.
Number of words registered	Maximum 40 words
Input voice length	0.16 ~ 0.96 sec.
Response time	Maximum 0.72 sec. (at 40 words registered)

4-2 Another part

Results of recognition	Block No.: 2 bits, Word No.: 4 bits
Command input	Manual mode: 4 × 4 key matrix CPU mode : 4 bit - data bus
Registration RAM	4Kbit - RAM up to 4 pieces or 16Kbit - RAM 1 piece
Clock frequency	400 KHz±10%

5. Operational Description

The operation of the T6658A is divided broadly into two modes; the registration mode and recognition mode. On the other hand, there are two methods for controlling the T6658A; the manual mode by means of an external keyboard and the CPU mode in which the T6658A is controlled by another micro-computer. Further, there is the stand-by mode to stop the operation of the T6658A to reduce power consumption. The registration and recognition modes are described in this section.



The registration mode is a mode to register words which are desired to be recognized and stored them in an external RAM. Words must always be registered prior to recognition.

The recognition mode is a mode to actually recognize words. In this recognition mode, the T6658A starts the recognition operation automatically whenever voice is input. Even after the T6658A has been placed in the recognition mode, it is possible to return to the registration mode again and make the addition and/or change of words to be registered or already registered words.

In the stand-by mode, the operation of the T6658A is completely stopped but contents of words registered in the external RAM are kept unchanged. It is possible to shift to this stand-by mode from both the recognition and registration modes. However, in case of the manual mode and registration mode, current flows into the built-in pull-down resistors and therefore, to operate the T6658A in the manual mode it is necessary to shift from the recognition mode to the stand-by mode.

## 5-1. Registration mode

This is the mode to register words to be recognized prior to recognition. It is necessary to execute the registration before actual recognition.

There are four commands (BLK, ENT, CAN and ALLCAN) available for the registration mode of the T6658A.

## (1) BLK Command

- Code 1 1 0 0 (Binary)
- Sequence  $\boxed{n} \cdot \boxed{BLK}$  n=Block No. (1 - 4)
- Operation This command specifies BLOCK No. to which words are registered or cancelled. This command is given to the T6658A following a numeral (1 - 4) specifying BLOCK No. After the execution of this command, the specified BLOCK No. is output to BLK<sub>1</sub>, BLK<sub>2</sub>. BLOCK No. once specified is held until next specification. However, at the start of the registration mode, the T6658A is in the state where BLOCK 1 is specified.

## (2) ENT Command

- o Code 1 1 0 1 (Binary)
- o Sequence ( $\boxed{n}$  ·  $\boxed{BLK}$ )  $\boxed{m}$   $\boxed{ENT}$  m = Word No. (1 - 10)
- o Operation This command specifies Word No. of an area in which words are registered. This command is given to the T6658A following numeral (1 - 10) specifying Word No. Thereafter, the T6658A is put in the state waiting voice input. Further, it is also possible to suspend the registration by giving optional code except NOP before voice input. This code is only a dummy, so it isn't processed as a command. After the registration process, registered BLOCK No. and Word No. or error code are output to  $BLK_1 - BLK_2$  and  $WD_1 - WD_4$ . If necessary, BLK command should be executed before this command.

## (3) CAN Command

- o Code 1 1 1 0 (Binary)
- o Sequence ( $\boxed{n}$  ·  $\boxed{BLK}$ )  $\boxed{m}$  ·  $\boxed{CAN}$  m = Word No. (1 to 10)
- o Operation This command cancels the word which is registered to the word No. specified. If necessary, BLK command should be executed before this command.

## (4) ALLCAN Command

- o Code 1 1 1 1 (Binary)
- o Sequence  $\boxed{ALLCAN}$
- o Operation This command cancels the registration of all words.



At the recognition mode, the T6658 skips the pattern matching process for any area in which no word is registered. Therefore, it is recommended for small word application to execute this command first in order to reduce response time and improve recognition accuracy.

(5) List of registration command (CPU mode)

Command name	Code				Operation
	K <sub>4</sub>	K <sub>3</sub>	K <sub>2</sub>	K <sub>1</sub>	
NOP	0	0	0	0	No operation, this code is given previously.
1	0	0	0	1	Block No., Word No. However block number is 1 - 4.
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
-	1	0	1	1	Inhibited
BLK	1	1	0	0	Block No. designation
ENT	1	1	0	1	1 word registration
CAN	1	1	1	0	1 word cancel
ALLCAN	1	1	1	1	All words cancel

Note) If at least 1 bit of K<sub>1</sub> - K<sub>4</sub> is "1" level, the T6658A operates as command input. Therefore, NOP command (All "0") are given previously. (Under CPU mode)

(6) Status output under registration mode

(1) BLK<sub>1</sub>, BLK<sub>2</sub>

Code BLK <sub>2</sub> BLK <sub>1</sub>		Meaning
0	0	be registered within block 1
0	1	be registered within block 2
1	0	be registered within block 3
1	1	be registered within block 4

Note) Block No. is 1 - 4 under the designation of BLK command, but outputs to BLK<sub>1</sub>, BLK<sub>2</sub> are 0 - 3. When an error occurred, BLK output is undefined.

(2) WD<sub>1</sub> -  
WD<sub>4</sub>

Code WD <sub>4</sub> WD <sub>3</sub> WD <sub>2</sub> WD <sub>1</sub>				Meaning
0	0	0	0	Unused
0	0	0	1	be registered to word 1
0	0	1	0	be registered to word 2
0	0	1	1	be registered to word 3
0	1	0	0	be registered to word 4
0	1	0	1	be registered to word 5
0	1	1	0	be registered to word 6
0	1	1	1	be registered to word 7
1	0	0	0	be registered to word 8
1	0	0	1	be registered to word 9
1	0	1	0	be registered to word 10
1	0	1	1	Unused (never be output)
1	1	0	0	Unused (never be output)
1	1	0	1	Unused (never be output)
1	1	1	0	Input voice is under 0.16 s.
1	1	1	1	Input voice is over 0.96 s.

(7) Precautions for registration operation  
(Common to Manual and CPU Mode)

- Once Block No. is designated, the same block becomes an object of registration and cancellation unless a new block is designated. However, the T6658A is in a state where Block 1 is designated immediately after the registration mode has started.
- If BLK, ENT or CAN command is given without giving primary figures specifying Block No. and Word No., Block No. and Word No. that become the objects of processing are indefinite. Therefore, use of the T6658A in such a manner as this should be avoided.
- If the registration is made again in the same Block No. and Word No. in which the registration has been made, the old contents of the registration are rewritten to the new contents.
- If any figure other than 1 through 4 is given to designate Block No., actually designated Block No. will be the given figure minus 4. In this case, however, BSY and EOR outputs are not properly carried out and therefore, control by an external CPU in the CPU mode may become impossible. If the redesignation is made using proper figures, BSY and EOR outputs are normally carried out.
- If plural figures are consecutively given, the lastly given figure is valid. Therefore, even when erroneous figures are given, if it is before giving BLK, ENT or CAN command, the proper operation can be made by giving proper figures.

Example: 5 . 6 . ENT      Registered in Word 6.

5-2. Recognition mode

Under the recognition mode, the T6658A starts the recognition process automatically when voices are input, and outputs the results to BLK<sub>1</sub> - BLK<sub>2</sub>, WD<sub>1</sub> - WD<sub>4</sub>. Therefore, it is only necessary for the host side to read outputs from the T6658A.

After end of the recognition, the T6658A does not accept next voice input for about 11 ms. This is a waiting time for the host system to surely read the result of recognition.

List of recognition output code

(1) BLK<sub>1</sub>, BLK<sub>2</sub>

Code BLK <sub>2</sub> BLK <sub>1</sub>		Meaning
0	0	be recognized within block 1
0	1	be recognized within block 2
1	0	be recognized within block 3
1	1	be recognized within block 4

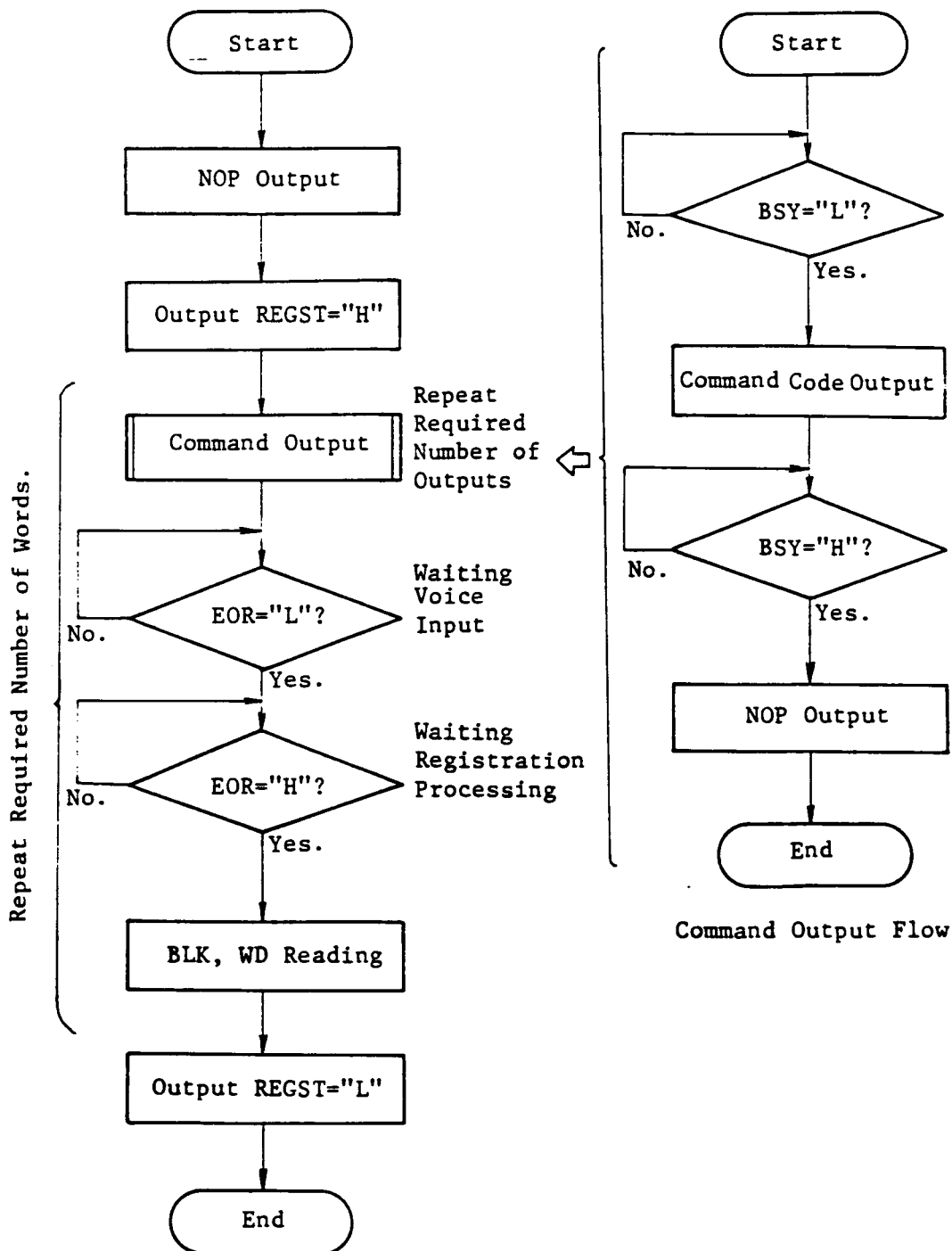
Note: When an error occurred, BLK output is undefined.

(2) WD<sub>1</sub> - WD<sub>4</sub>

Code WD <sub>4</sub> WD <sub>3</sub> WD <sub>2</sub> WD <sub>1</sub>				Meaning
0	0	0	0	Unused
0	0	0	1	be recognized as word 1
0	0	1	0	be recognized as word 2
0	0	1	1	be recognized as word 3
0	1	0	0	be recognized as word 4
0	1	0	1	be recognized as word 5
0	1	1	0	be recognized as word 6
0	1	1	1	be recognized as word 7
1	0	0	0	be recognized as word 8
1	0	0	1	be recognized as word 9
1	0	1	0	be recognized as word 10
1	0	1	1	Unused (never be output)
1	1	0	0	Unused (never be output)
1	1	0	1	Judged as unregistered word.
1	1	1	0	Input voice is under 0.16 s.
1	1	1	1	Input voice is over 0.96 s.

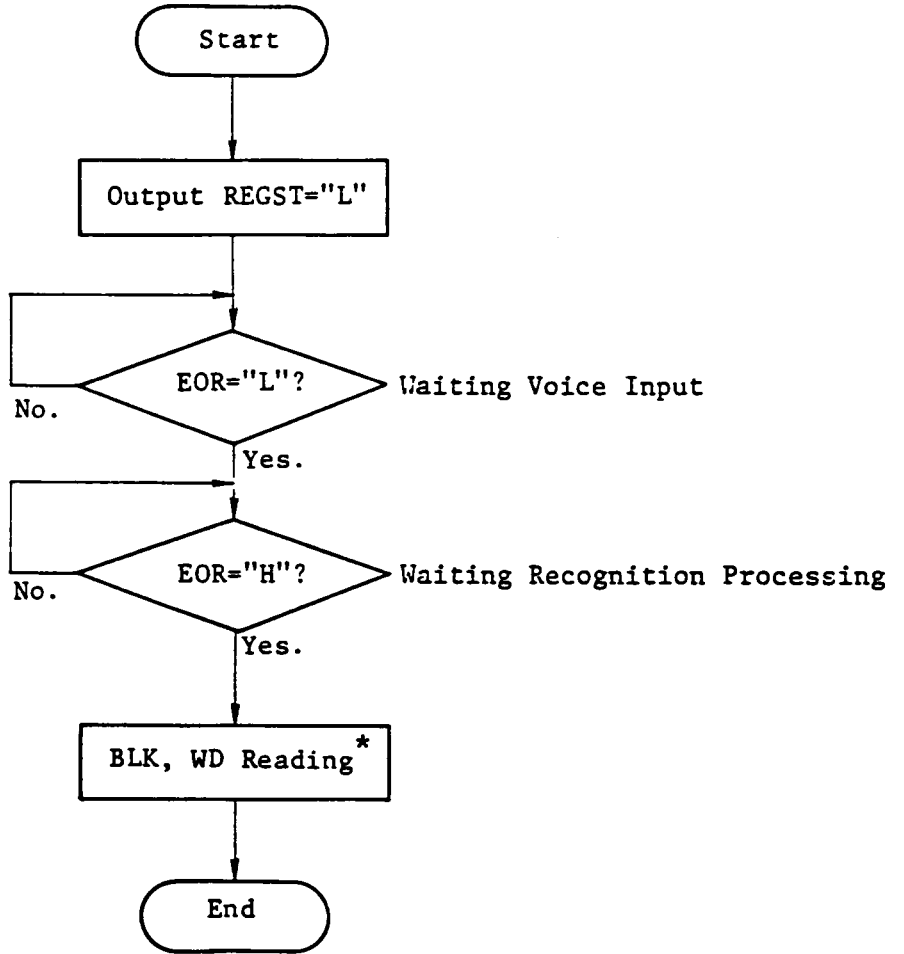
5-3. Examples of control in CPU mode

(1) Registration mode



One Word Registration Flow

(2) Recognition mode



Note) If reading of BLK<sub>1</sub> - BLK<sub>2</sub> and WD<sub>1</sub> - WD<sub>4</sub> is not completed within 11ms after the rise of EOR, there is a probability of the change of these outputs due to next voice input.

5-4 Example of operation in manual mode

In the manual mode, all the operation for registration are performed through the externally connected keyboard.

Meanings and sequence of commands are as described previously. Examples are shown below.

Kinds of Keys

n (Figure 1~10)	Block No., Word No.
BLK	Block designation
ENT	One word registration
CAN	One word cancel
ALL CAN	All words cancel

Example of Operation Flow

REGST="H"	(Set to Registration Mode)	
<u>ALL CAN</u>	All words cancel	
<u>1</u> <u>BLK</u> <u>1</u> <u>ENT</u>	Registration in Block 1, Word 1	} Order of Block No. or Word No. can be designated freely and be used repeatedly, if necessary.
"Voice"		
<u>2</u> <u>ENT</u>	Registration in Block 1, Word 2	
"Voice"		
}		
<u>2</u> <u>BLK</u> <u>1</u> <u>ENT</u>	Registration in Block 2, Word 1	
"Voice"		
}		
RESET="L"	(Set to Recognition Mode)	
"Voice"		
Output of recognition result		
}		

## 5-5 Stand-by Mode

## (1) State of T6658A in stand-by mode and precautions

- The clock is stopped, and  $BSY="H"$  and  $\overline{ACL}="L"$  are output.
- Result of recognition ( $BLK_1$ ,  $BLK_2$ ,  $WD_1 \sim WD_2$ ) is kept as it is. Therefore, in such a case where LED is kept ON by this output, it is necessary to turn off LED through the external circuit.
- If  $\overline{RD}="L"$  in the manual mode, current may flow to the internal pull-down resistors (connected to  $K_1 \sim K_4$ ). In the manual mode, therefore,  $\overline{RD}$  must be always kept at "H" level.
- If  $REGST="H"$  in the manual mode, current may flow to the internal pull-down resistors. In the manual mode, therefore, it is necessary to set  $REGST$  to "L" level and then, place the T6658A in the stand-by state.
- The T6658A is placed in the stand-by state asynchronous with the internal CPU operation. Therefore, in such as application where the T6658A is controlled by an external CPU, it is necessary to pay attention to the timing for placing the T6658A in the stand-by state.

## (2) Operation at time of releasing the T6658A from stand-by state

- If  $REGST="H"$  when  $STBY$  becomes "L", the T6658A performs the internal initialization. Therefore,  $BSY$  becomes "L" and it becomes possible to input commands. In this state, recognition outputs are all "0".
- If  $REGST="L"$  when  $STBY$  becomes "L", the T6658A performs the internal initialization and "0" is output for the recognition outputs ( $BLK_1$ ,  $BLK_2$ ,  $WD_1 \sim WD_2$ ). At this time,  $EOR$  is kept at "H". Therefore, it becomes possible to accept voice inputs. A time from the stand-by releasing to voice input is about 30ms.



## 5-6 Reset operation

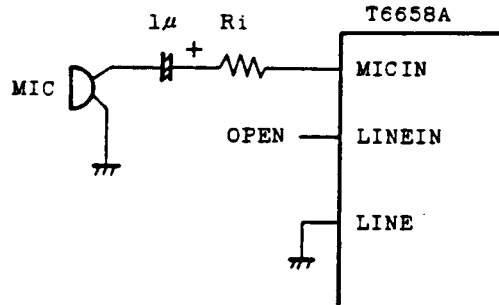
The  $\overline{ACL}$  terminal of the T6658 is the I/O terminal and when  $STBY="H"$ ,  $\overline{ACL}="L"$  is output. On the other hand, the T6658A can be reset by giving a "L" level signal to this terminal from the outside. The reset operation of the T6658A is explained in the following.

- When  $\overline{ACL}="L"$ , interrupting the processing of registration and recognition, the T6658A outputs  $BSY="H"$  signal. However, the check is not stopped.
- When  $\overline{ACL}="H"$ , the T6658A performs the internal initialization. The operation at this time is the same as that at time of standby release. Refer to 5-5 Standby Mode (2).
- The registered data stored in RAM remain unchanged regardless of the reset operation.

6. Description of External Circuit

6-1 Microphone input

The dynamic range (Maximum allowable input without distortion) of the MICIN terminal is 3.5 mVrms. By connecting a resistor to the MICIN terminal in series, it is possible to reduce gain of the on-chip microphone amplifier of the T6658A and expand this dynamic range.

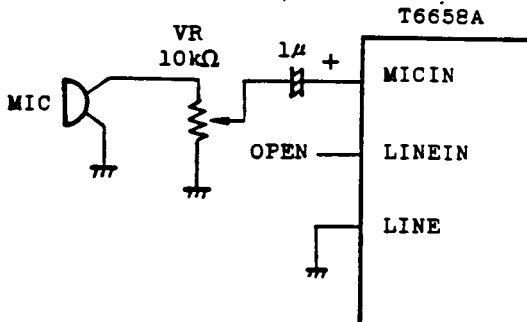


DYNAMIC RANGE

$$DR = \left(1 + \frac{R_i [k\Omega]}{25}\right) \times 3.5 [mvrms]$$

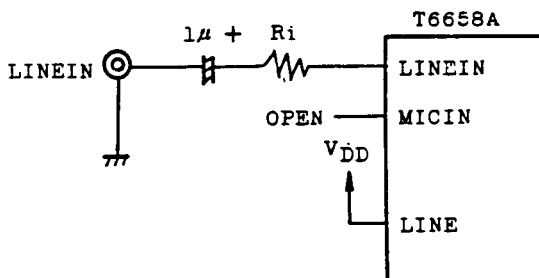
$$R_i = 0 \sim 50 [k\Omega]$$

If a value of Ri becomes excessively large, noise is easily picked up. Therefore, to further decrease the microphone input level, a variable resistor (VR) should be used as illustrated below.



6-2 Line input

The dynamic range of the LINEIN terminal is 550 mVrms, but it is possible to expand this dynamic range by connecting a resistor to this terminal in series.



DYNAMIC RANGE

$$DR = \left(1 + \frac{R_i [k\Omega]}{65}\right) \times 550 [mvrms]$$

$$R_i = 0 \sim 100 [k\Omega]$$

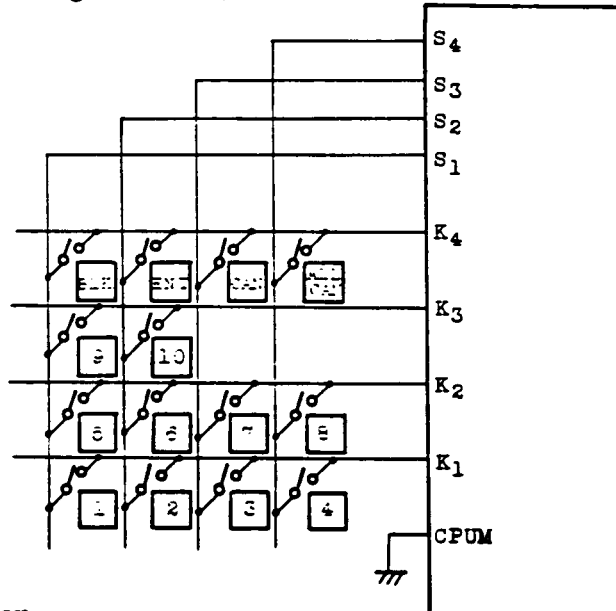
Note: Input level adjustment

To adjust levels at the MICIN and LINEIN terminals, it is a good method to observe output signal level from the MICOUT terminal of the T6658A. Instead of a microphone, etc., connect 1 kHz sine wave that has about the same level as the level that is obtained when spoken to a microphone in an ordinary loudness of voice. While observing signal at the MICOUT terminal by means of an oscilloscope, etc., adjust it with VR, etc. to obtain 250 ~ 300 mVpp.

6-3 Keyboard switches connection

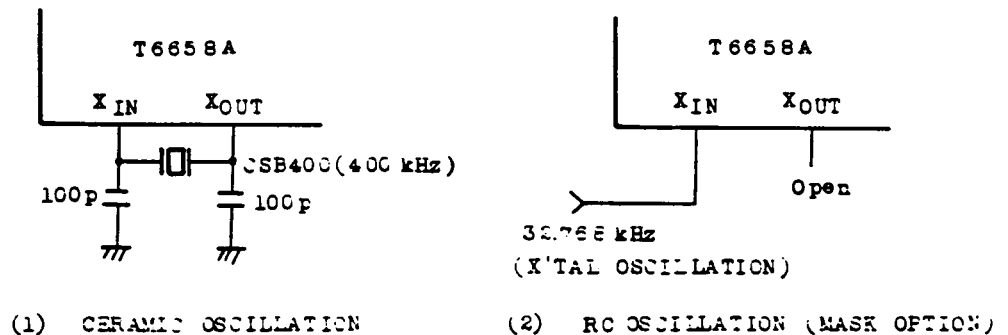
The keyboard switches connection under the manual mode is illustrated in the following figure. The switch should not be connected to those portions on the matrix without entry of the switch.

The chattering time must be less than 20mS. T6658A



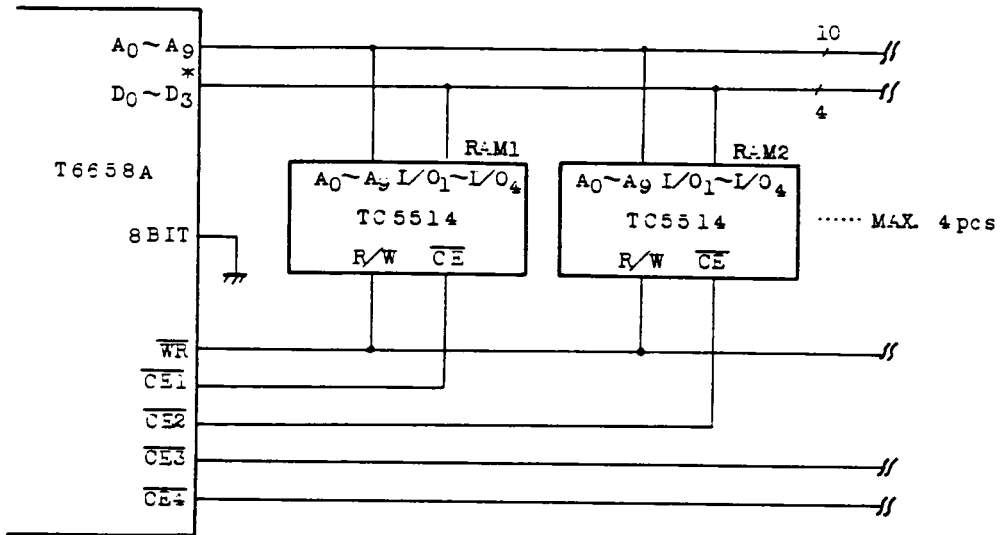
6-4 Clock generator

The T6658A has an on-chip RC oscillator circuit as a clock generator in addition to the ceramic oscillator circuit, and this circuit can be operated with a 32.768 kHz clock as the synchronizing signal from the outside. (Mask option)



6-5 External RAM connection

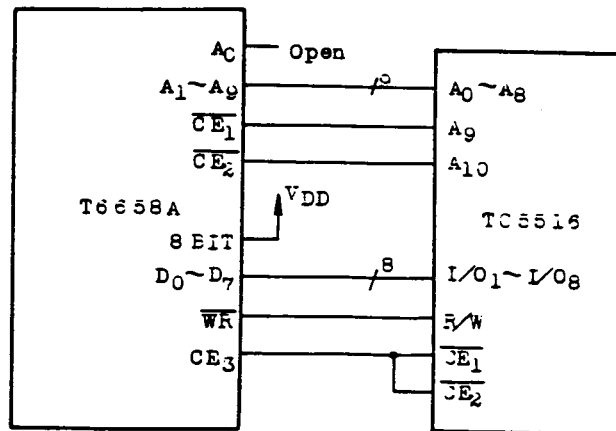
(1) Under using 1024 word by 4 bit RAM



\* D<sub>4</sub>~D<sub>7</sub> are not used. Leave open.

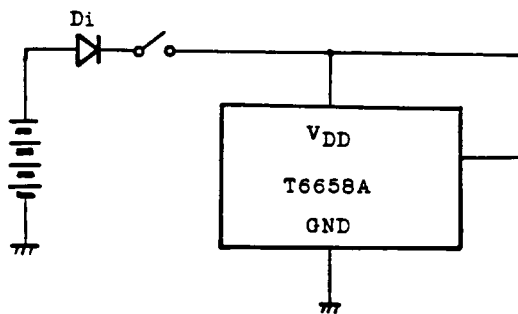
\* RAM<sub>1</sub>~RAM<sub>4</sub> are used for the registrations of block<sub>1</sub>~block<sub>4</sub> correspondently. The RAM<sub>1</sub> always must be connected.

(2) Under using 2048 word by 8 bit RAM



6-6 Precaution for use of dry battery

When four dry batteries are used as the power supply of the T6658A, voltage may exceed 6V and the absolute maximum rating at the early stage after started to operate. In this case, it is necessary to take some measures; e.g., to insert a diode into a power circuit in series.



Di : 1S1588, etc.

The terminal to be set at "H" level must always be connected to the power that has passed through a diode.



## 7. Pin Descriptions

### 7-1 MICIN (Analog Input)

The microphone connecting terminal. A microphone is connected to this terminal with a coupling capacitor.

### 7-2 LINEIN (Analog Input)

The line input terminal. Signal is input between this terminal and GND through a coupling capacitor.

### 7-3 LINE (Digital Input)

The microphone/line input selection terminal. When this terminal is placed at "L" level, the MICIN is selected, and at "H" level, the LINEIN is selected.

### 7-4 MICOUT, TRAI, TRAO, TRCI (Analog I/O)

A Customer can't use these terminals. Leave open.

### 7-5 $K_1 - K_4$ (Digital I/O)

The command input terminals at time of the registration mode. Under the CPU mode, commands are directly given from the CPU side. Under the manual mode, a keyboard is connected, at the same time the internal pull down registers are connected. The key chattering suppression time is about 20 ms. When  $\overline{RD}$  is at "L" level, the same value as contents of  $WD_1 - WD_4$  are output independently of the registration/recognition mode.

### 7-6 $S_1 - S_4$ (Digital Output)

The key scan signal output at the manual mode.



## 7-7 CPUM (Digital Input)

The Manual/CPU Mode selection terminal. When this terminal is at "L" level, the system is placed in the manual mode.

When this terminal is changed to "H" level, the system is placed in the CPU mode and commands for the registration are transferred directly to  $K_1 - K_4$  from CPU.

## 7-8 REGST (Digital Input)

The recognition/registration mode selection terminal. When this terminal is at "L" level, the system is placed in the recognition mode and performs the recognition for input voice. At "H" level, the system is placed in the registration mode and performs the registration for input voice. Under manual mode, the internal pull down register is connected.

7-9  $WD_1 - WD_4$ ,  $BLK_1$ ,  $BLK_2$  (Digital Outputs)

These are the output terminals of result of recognition. Block No. and Word No. of registered words, which are judged to be most similar to input voice, are output. These outputs are held until next voice input at recognition mode, and until next command input at registration mode. Immediately after system reset, these terminals are placed to "L" level.

## 7-10 EOR (Digital Output)

The EOR (End of Recognition) output terminal. Under both the recognition/registration modes, this terminal is placed at "L" level during voice input and becomes "H" level when the results are output to  $WD_1 - WD_4$ ,  $BLK_1$  and  $BLK_2$  after end of the recognition/registration process.

7-11  $\overline{RD}$  (Digital Input)

The  $K_1 - K_4$  I/O selection terminal. When this terminal is placed at "L" level, the same contents as those of  $WD_1 - WD_4$  are output to  $K_1 - K_4$ . Further, when this terminal is at "H" level,  $K_1 - K_4$  are changed to the input terminals, and bidirectional data transfer is possible for CPU.

7-12  $A_0 - A_9$  (Digital Outputs)

The address bus to be connected to an external RAM for registration. Either a 1024 word by 4 bit RAM or a 2048 word by 8 bit is used. (Refer to section 6 - 5 External RAM connection for details.)

7-13  $D_0 - D_7$  (Digital I/O)

The data bus for external RAM. Only  $D_0 - D_3$  are used by A 1024 word by 4 bit RAM.

7-14  $\overline{CE}_1 - \overline{CE}_4$  (Digital Outputs)

The chip enable outputs for external RAM. A 2048 word  $\times$  8 bit RAM uses  $\overline{CE}_1$  and  $\overline{CE}_2$  as  $A_9$  and  $A_{10}$  respectively, and connects  $\overline{CE}_3$  to the chip enable terminal of RAM. (Refer to 6 - 5 External RAM connection for details.)

7-15  $\overline{WR}$  (Digital Output)

The WRITE signal for external RAM.

## 7-16 8BIT (Digital Input)

The external RAM selection terminal. This terminal is placed at "L" level for a 1024 word  $\times$  4 bit RAM, and at "H" level for a 2048 word  $\times$  8 bit RAM.

7-17  $\overline{ACL}$  (Digital I/O)

The system reset terminal of the T6658A. At time of power ON and under stand-by state, "L" level signal is output. Normally, a capacitor is connected between this terminal and GND, but it is also possible to give signal externally.  $\overline{ACL}$  pulse width is 30 ms TYP. ( $C_{ACL}=1 \mu F$ ).

## 7-18 STBY (Digital Input)

The standby input terminal. When a "H" level signal is input to this terminal, the T6658A is placed in the stand-by mode.

## 7-19 BSY (Digital Output)

When the T6658A is processing a command under the registration mode, "H" level signal indicates next command cannot be accepted. Further, this terminal becomes "H" level when registering voice is being input. Under the recognition mode, "H" level signal is always output.

7-20 Vref, Csref, ADCAP, CAP<sub>1</sub>, CAP<sub>2</sub>

The decoupling capacitor connecting terminals of the reference voltage circuit inside the T6658A. A capacitor is connected between each of these terminals and GND.

7-21 X<sub>IN</sub>, X<sub>OUT</sub> (Digital I/O)

A ceramic oscillator (400 kHz) for the T6658A internal clock is connected to these terminals. When RC oscillation is selected by the mask option, 32.768 kHz clock is given to X<sub>IN</sub> from the outside as synchronizing signal.

At this time, X<sub>OUT</sub> should be kept open. (Refer to section 6 - 4 Clock generator for details.)

7-22 TS<sub>1</sub>, TS<sub>2</sub>, TIO<sub>1</sub>, TIO<sub>2</sub>

The test terminals. Connect TS<sub>1</sub> and TS<sub>2</sub> to GND and leave TIO<sub>1</sub> and TIO<sub>2</sub> open.

7-23 V<sub>DD</sub>, GND

The power supply terminals.

T6658A Table of Terminals

Name	Pin No.	I/O	Description	Remark
MICIN	64	Input	MIC Input	
LINEIN	66	Input	LINE Input	
LINE	65	Input	MIC/LINE input selection	
MICOUT	67	Output	MIC AMP Output	
TRAI	1	Input	For test	
TRAO	2	Output	For test	
TACI	3	Input	For test	
K1	40	I/O	Command input, recognition output (Word No.)	Pull down in the manual mode
K2	39	I/O	"	"
K3	38	I/O	"	"
K4	37	I/O	"	"
S1	44	Output	Key scan signal (in the manual mode)	
S2	43	Output	"	
S3	42	Output	"	
S4	41	Output	"	
CPUM	56	Input	Manual/CPU mode selection	
REGST	46	Input	Rrecognition/registratation mode selection.	Pull down in the manual mode
WD1	54	Output	Recognition output (Word No.)	
WD2	53	Output	"	
WD3	52	Output	"	
WD4	51	Output	"	
BLK1	50	Output	Recognition output (Block No.)	
BLK2	49	Output	"	
EOR	48	Output	Recognition end signal	
BSY	47	Output	BUSY signal	
$\overline{RD}$	45	Input	Read signal to K1 ~ K4	
A0	20	Output	Address for registratation RAM	
A1	21	Output	"	

**TOSHIBA** INTEGRATED CIRCUIT  
TECHNICAL DATA

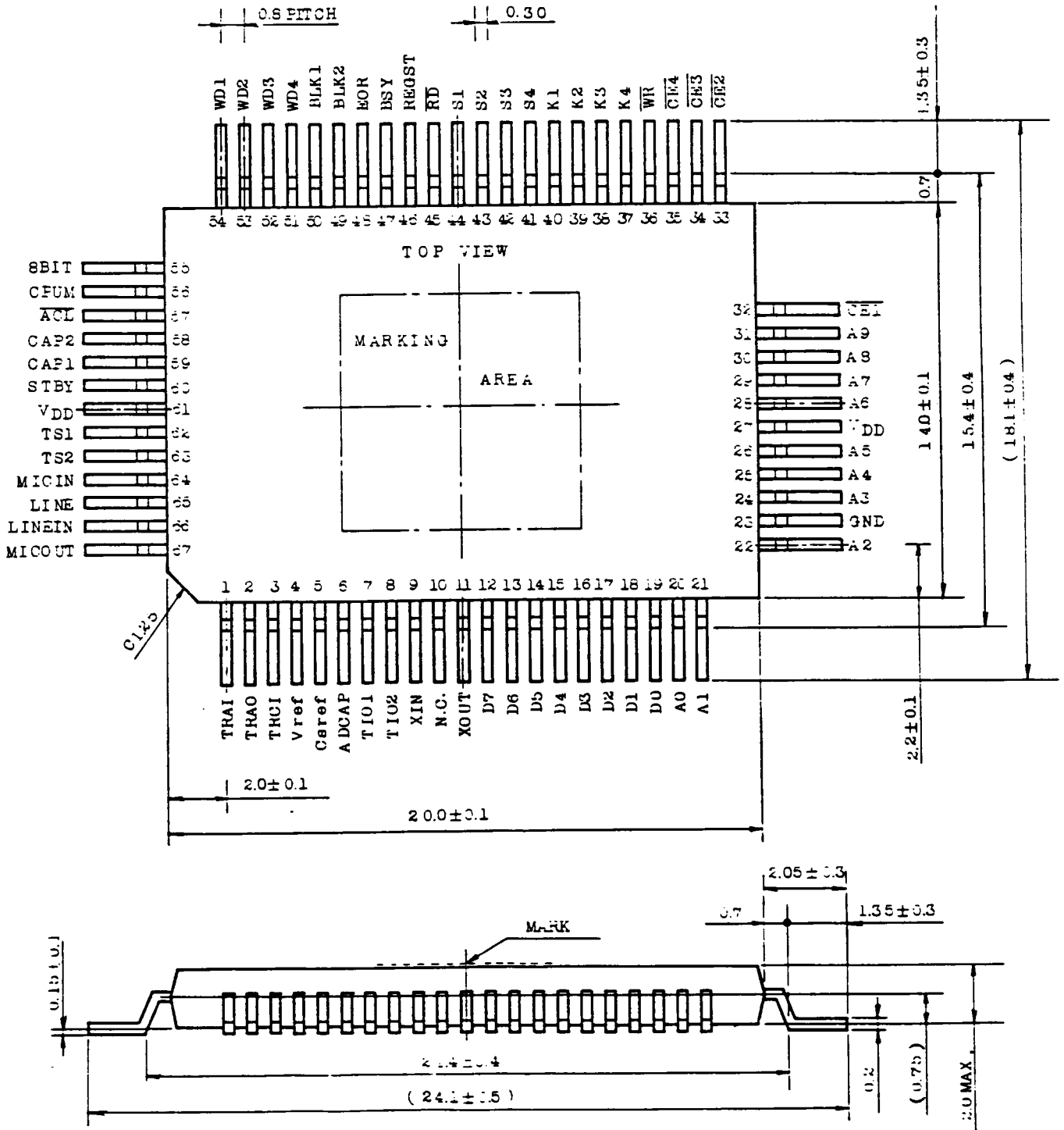
Name	Pin No.	I/O	Description	Remark
A2	22	Output	Address for registration RAM	
A3	24	Output	"	
A4	25	Output	"	
A5	26	Output	"	
A6	28	Output	"	
A7	29	Output	"	
A8	30	Output	"	
A9	31	Output	"	
D0	19	I/O	Data bus for registration RAM	Pull down at time of input
D1	18	I/O	"	"
D2	17	I/O	"	"
D3	16	I/O	"	"
D4	15	I/O	"	"
D5	14	I/O	"	"
D6	13	I/O	"	"
D7	12	I/C	"	"
$\overline{CE1}$	32	Output	Chip enable for registration RAM	
$\overline{CE2}$	33	Output	"	
$\overline{CE3}$	34	Output	"	
$\overline{CE4}$	35	Output	"	
$\overline{WR}$	36	Output	Write strobe for registration RAM	
8BIT	55	Input	4-bit/8-bit RAM selection	
STBY	60	Input	Stand-by signal	
$\overline{ACL}$	57	I/O	Reset signal	
Vref	4	-	Analog circuit reference voltage	
CSref	5	-	"	
ADCAP	6	-	"	
CAP1	59	-	"	
CAP2	58	-	"	

Name	Pin No.	I/O	Description	Remark
XIN	9	Input	Ceramic vibrator connecting terminal	
XOUT	11	Output	"	
TS1	62	Input	For test	Pull down
TS2	63	Input	"	"
TI01	7	I/O	"	
TI02	8	I/O	"	
VDD	27, 61	-	Power terminal	
GND	23	-	Ground	

8. Package outline T6658AF-BS

67 PIN FLAT PACKAGE (67-4-BS)

Unit in mm



2-31

### 9. Electrical Characteristics

#### 9-1 Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	-0.3 ~ +6.0	V
Input Voltage	V <sub>IN</sub>	-0.3 ~ V <sub>DD</sub> +0.3	V
Output Voltage	V <sub>OUT</sub>	-0.3 ~ V <sub>DD</sub> +0.3	V
Storage Temperature	T <sub>stg</sub>	-55 ~ +125	°C

#### 9-2 Recommended Operating Conditions

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	4.5 ~ 5.5	V
Input Voltage	V <sub>IN</sub>	0 ~ V <sub>DD</sub>	V
Output Voltage	V <sub>OUT</sub>	0 ~ V <sub>DD</sub>	V
Clock Frequency	f <sub>CLK</sub>	360 ~ 440	KHz
Operating Temperature	T <sub>opr</sub>	-10 ~ +70	°C

#### 9-3 DC Characteristics (V<sub>DD</sub>=+5.0V±10%, Ta=25°C)

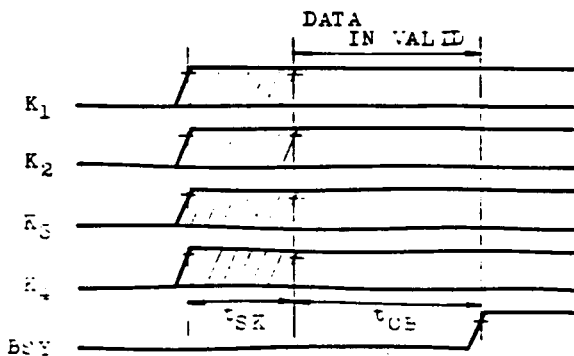
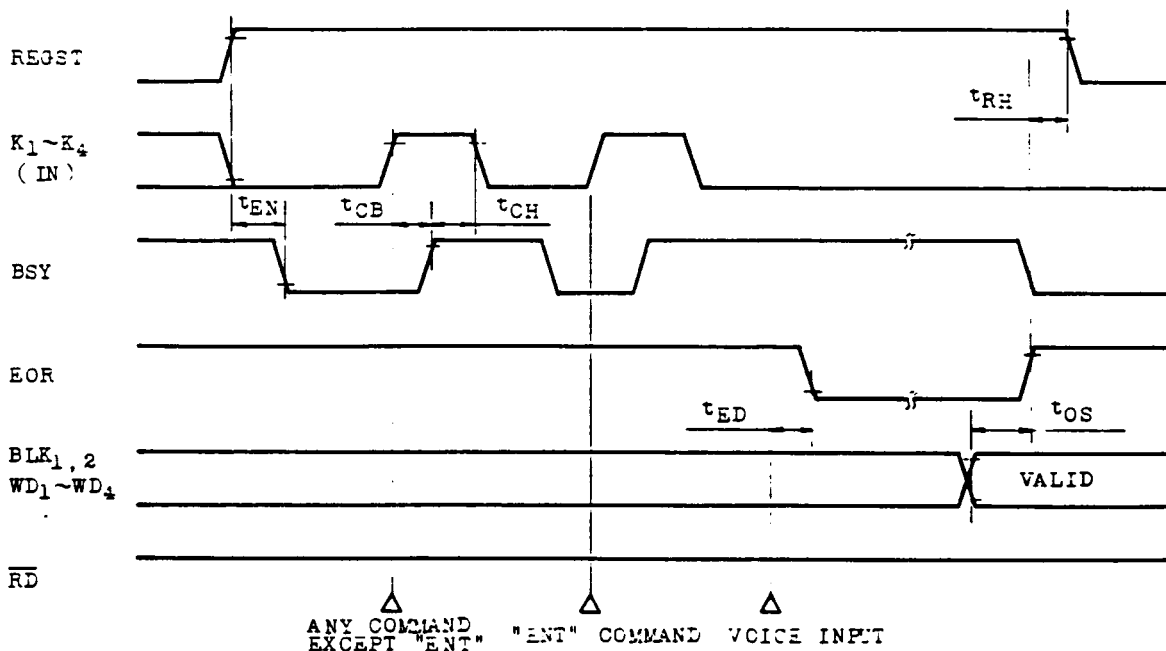
PARAMETER		SYMBOL	CONDITION	STANDBY VALUE			UNIT
				MIN	TYP	MAX	
Input Low Voltage		V <sub>IL</sub>		-	-	0.8	V
Input High Voltage	CPUM, 8 BIT ACL, XIN	V <sub>IH</sub>		V <sub>DD</sub> -0.8	-	-	V
	Except above		2.2	-	-		
Input Low Current		I <sub>IL</sub>	V <sub>IN</sub> =0V	-	-	-5	μA
Input High Current	K1~K4, REGST TS1, TS2	I <sub>IH</sub>	V <sub>IN</sub> =V <sub>DD</sub> , CPUM=V <sub>IL</sub>	-	100	250	μA
	DO ~ D7		V <sub>IN</sub> =V <sub>DD</sub>	-	50	125	
	Except above		V <sub>IN</sub> =V <sub>DD</sub>	-	-	5	
Output Low Current	S1 ~ S4	I <sub>OL</sub>	V <sub>OUT</sub> =0.8V	-	16	-	μA
	Except above		V <sub>OUT</sub> =0.4V	0.44	-	-	mA
Output High Current	S1 ~ S4	I <sub>OH</sub>	V <sub>OUT</sub> =V <sub>DD</sub> -2.0V	-	-0.36	-	mA
	Except above		V <sub>OUT</sub> =V <sub>DD</sub> -0.4V	-0.22	-	-	mA
Supply Current (1)		I <sub>DD</sub>	In case of voice	-	4.5	9.0	mA
Supply Current (2)		I <sub>STBY</sub>	STBY=V <sub>IH</sub>	-	-	3	μA



### 6-3 AC Characteristics ( $V_{DD}=5.0V\pm 10\%$ , $T_a=25^\circ C$ , $f_{CLK}=400KHz$ )

#### (1) Registration mode ( $CPUM=V_{IH}$ )

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
REGST $\rightarrow$ BSY Delay Time	$t_{EN}$		-	-	1.1	ms
Command $\rightarrow$ BSY Delay Time	$t_{CB}$		-	-	300	$\mu s$
Command Hold Time	$t_{CH}$		0	-	-	$\mu s$
Voice $\rightarrow$ EOR Delay Time	$t_{ED}$		-	-	1	ms
Data Set up Time (to EOR)	$t_{OS}$		40	-	-	$\mu s$
REGST Hold Time (from EOR)	$t_{RH}$		0	-	-	$\mu s$
Command bit Skew time *	$t_{SK}$		-	-	40	$\mu s$



Note: The  $t_{SK}$  means an allowance of skew of a rising edge about  $K_1 \sim K_4$  to give commands correctly.

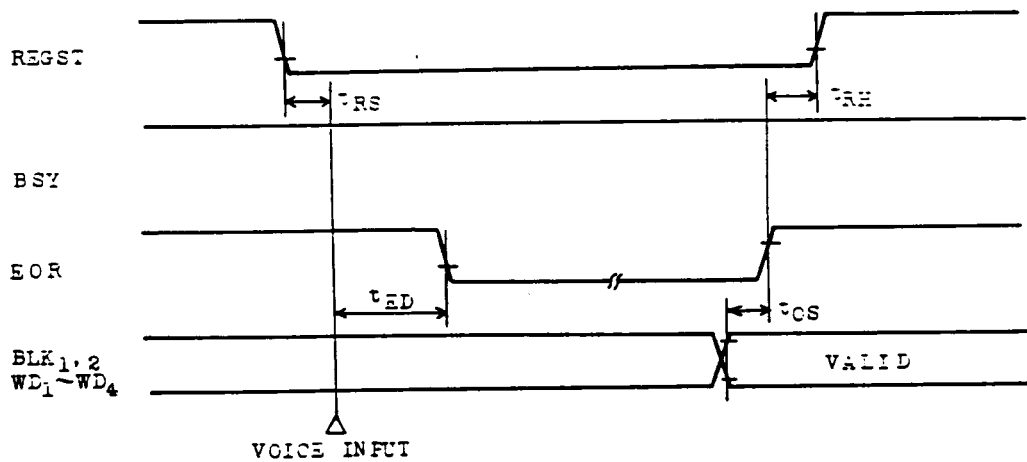
There is no limit about a falling.

# TOSHIBA INTEGRATED CIRCUIT

## TECHNICAL DATA

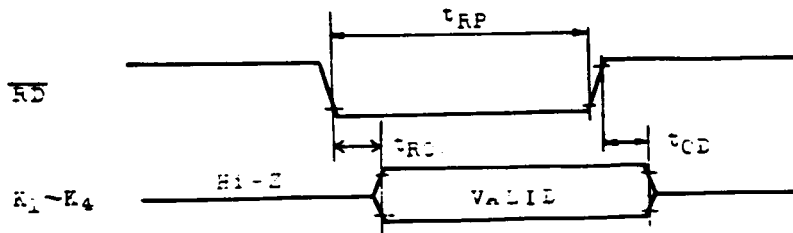
### (2) Recognition mode (CPUM = V<sub>IH</sub>)

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
REGST Set up Time (to voice input)	t <sub>RS</sub>		480	-	-	μs
Voice → EOR Delay Time	t <sub>ED</sub>		-	-	0.7	ms
Data Set up Time	t <sub>OS</sub>		40	-	-	μs
REGST Hold Time	t <sub>RH</sub>		0	-	-	μs



### (3) K<sub>1</sub> ~ K<sub>4</sub> Read cycle

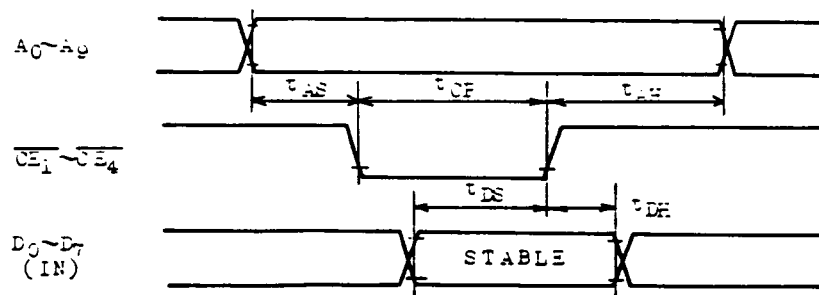
ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
$\overline{RD}$ Pulse Width	t <sub>RP</sub>		1000	-	-	ns
Output Delay Time	t <sub>RO</sub>		-	-	500	ns
Output Disable Time	t <sub>OD</sub>		-	-	500	ns



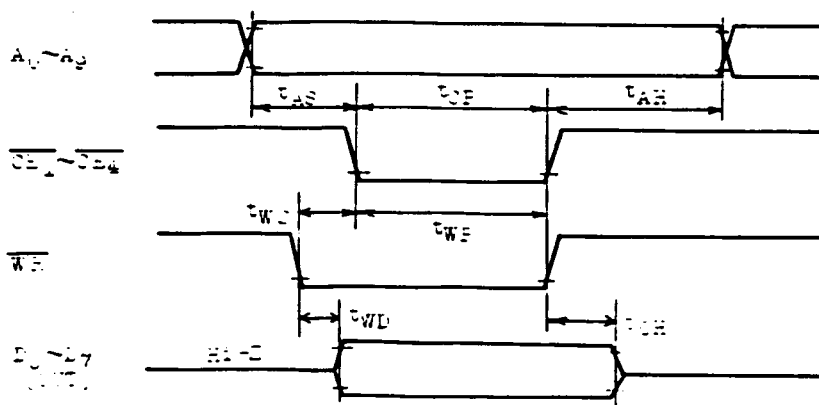
### (4) Memory read/write cycle

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Address Setup Time	$t_{AS}$		2.5	-	-	$\mu s$
Address Hold Time	$t_{AH}$		10	-	-	$\mu s$
$\overline{CE}$ Pulse Width	$t_{CP}$		-	7.5	-	$\mu s$
Data Setup Time	$t_{DS}$		5.0	-	-	$\mu s$
Data Hold Time	$t_{DH}$		0	-	-	$\mu s$
Write Pulse Setup Time	$t_{WS}$		-	2.5	-	$\mu s$
Write Pulse Width	$t_{WP}$		-	10	-	$\mu s$
Output Delay Time	$t_{WD}$		-	-	500	ns
Output Disable Time	$t_{OH}$		-	-	500	ns

#### MEMORY READ CYCLE



#### MEMORY WRITE CYCLE



**TOSHIBA** INTEGRATED CIRCUIT  
TECHNICAL DATA

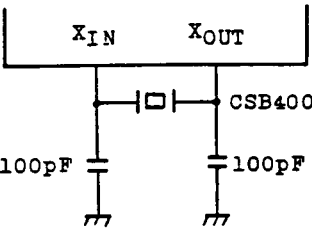
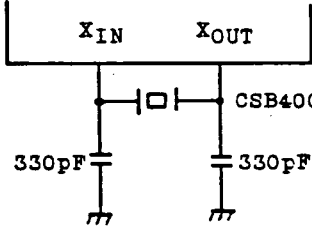
6-4 Analog input terminal ( $V_{DD} = +5.0 \text{ V} \pm 1\%$ ,  $T_a = 25^\circ\text{C}$ )

ITEM		SYMBOL	CONDITION	STANDARD VALUE			UNIT
				MIN.	TYP.	MAX.	
Allowable Input	MICIN	$V_{in}$	without generating a distortion	-	-	3.5	mVrms
	LINEIN			-	-	550	
Input Resistance	MICIN	$R_{in}$	$f = 1 \text{ KHz}$	-	25	-	$\text{K}\Omega$
	LINEIN			-	65	-	

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T6658A ERRATA

Page	Error	Correctness
<p>2 . 3 . 20</p>	 <p>The diagram shows two input/output terminals, X<sub>IN</sub> and X<sub>OUT</sub>, connected to a central component labeled CSB400. Each terminal is connected to the component through a 100pF capacitor, which is in turn connected to ground.</p>	 <p>The diagram shows two input/output terminals, X<sub>IN</sub> and X<sub>OUT</sub>, connected to a central component labeled CSB400. Each terminal is connected to the component through a 330pF capacitor, which is in turn connected to ground.</p>