

**TC74VHC374F, TC74VHC374FW, TC74VHC374FT**

**OCTAL D - TYPE FLIP - FLOP WITH 3 - STATE OUTPUT**

The TC74VHC374 is an advanced high speed CMOS OCTAL FLIP - FLOP with 3 - STATE OUTPUT fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8 - bit D - type flip - flop is controlled by a clock input (CK) and an output enable input ( $\overline{OE}$ ).




When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

**FEATURES :**

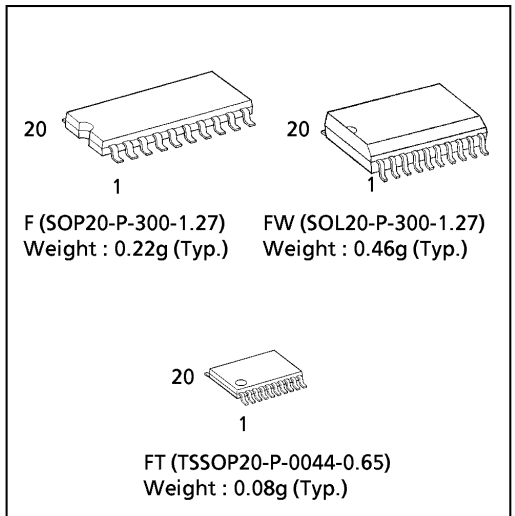
- High Speed..... $f_{MAX} = 185\text{MHz}(\text{typ.})$   
at  $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$  at  $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Low Noise..... $V_{OLP} = 0.9\text{V} (\text{Max.})$
- Pin and Function Compatible with 74ALS374

**TRUTH TABLE**

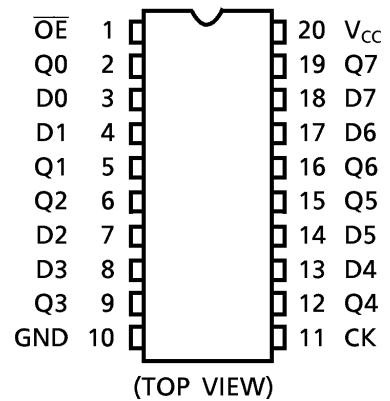
INPUTS			OUTPUT
$\overline{OE}$	CK	D	
H	X	X	Z
L		X	$Q_n$
L		L	L
L		H	H

X : Don't Care  
Z : High Impedance  
 $Q_n$  : No Change

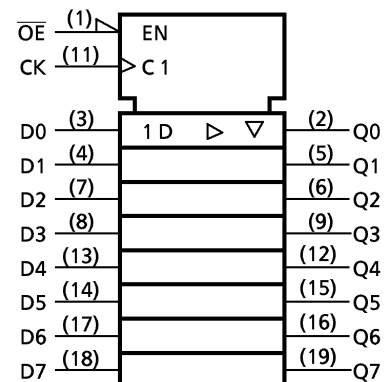
(Note) The JEDEC SOP (FW) is not available in Japan.



**PIN ASSIGNMENT**



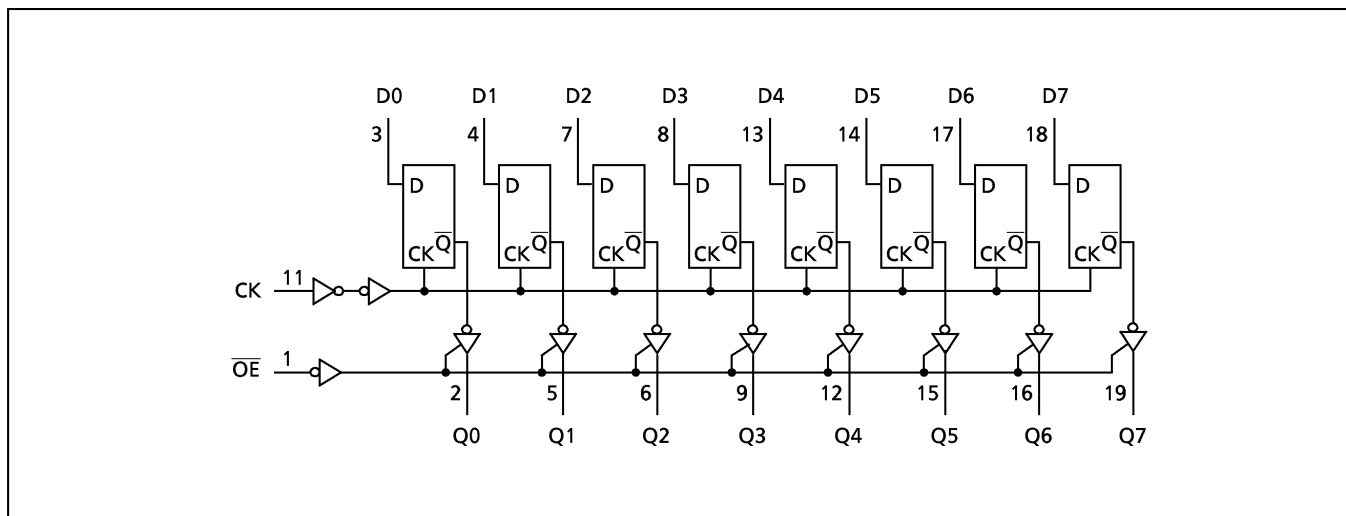
**IEC LOGIC SYMBOL**



980910EBA2

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## SYSTEM DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 75$	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65~150	$^{\circ}C$

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2.0~5.5	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	$^{\circ}C$
Input Rise and Fall Time	$dt/dv$	0~100 ( $V_{CC} = 3.3 \pm 0.3V$ ) 0~20 ( $V_{CC} = 5 \pm 0.5V$ )	ns/V

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**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V <sub>IH</sub>		2.0 3.0~ 5.5	1.50 V <sub>CC</sub> × 0.7	— —	— —	1.50 V <sub>CC</sub> × 0.7	—	V	
Low - Level Input Voltage	V <sub>IL</sub>		2.0 3.0~ 5.5	— —	— —	0.50 V <sub>CC</sub> × 0.3	— —	0.50 V <sub>CC</sub> × 0.3	V	
High - Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
			I <sub>OH</sub> = -4mA I <sub>OH</sub> = -8mA	4.5	4.4	4.5	—	4.4	—	
				3.0	2.58	—	—	2.48	—	
			I <sub>OH</sub> = -8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
			I <sub>OL</sub> = 4mA I <sub>OL</sub> = 8mA	4.5	—	0.0	0.1	—	0.1	
				3.0	—	—	0.36	—	0.44	
			4.5	—	—	0.36	—	0.44		
3 - State Output Off - State Current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.25	—	±2.50	μA	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5V or GND	0~5.5	—	—	±0.1	—	±1.0		
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	4.0	—	40.0		

**TIMING REQUIREMENTS ( Input t<sub>r</sub> = t<sub>f</sub> = 3ns )**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP .	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t <sub>W(H)</sub>		3.3 ± 0.3	—	5.0	5.5	ns
	t <sub>W(L)</sub>		5.0 ± 0.5	—	5.0	5.0	
Minimum Set - up Time	t <sub>s</sub>		3.3 ± 0.3	—	4.5	4.5	
			5.0 ± 0.5	—	3.0	3.0	
Minimum Hold Time	t <sub>h</sub>		3.3 ± 0.3	—	2.0	2.0	
			5.0 ± 0.5	—	2.0	2.0	

AC ELECTRICAL CHARACTERISTICS ( Input  $t_r = t_f = 3\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V <sub>CC</sub> (V)	CL (pF)	MIN.	TYP.	MAX.		MIN.
Propagation Delay Time (CK-Q)	$t_{pLH}$ $t_{pHL}$		$3.3 \pm 0.3$	15	—	8.1	12.7	1.0	15.0
				50	—	10.6	16.2	1.0	18.5
			$5.0 \pm 0.5$	15	—	5.4	8.1	1.0	9.5
				50	—	6.9	10.1	1.0	11.5
3-State Output Enable Time	$t_{pZL}$ $t_{pZH}$	RL = 1k $\Omega$	$3.3 \pm 0.3$	15	—	7.1	11.0	1.0	13.0
				50	—	9.6	14.5	1.0	16.5
			$5.0 \pm 0.5$	15	—	5.1	7.6	1.0	9.0
				50	—	6.6	9.6	1.0	11.0
3-State Output Disable Time	$t_{pLZ}$ $t_{pHZ}$	RL = 1k $\Omega$	$3.3 \pm 0.3$	50	—	10.2	14.0	1.0	16.0
			$5.0 \pm 0.5$	50	—	6.1	8.8	1.0	10.0
Maximum Clock Frequency	$f_{MAX}$		$3.3 \pm 0.3$	15	80	130	—	70	—
				50	55	85	—	50	—
			$5.0 \pm 0.5$	15	130	185	—	110	—
				50	85	120	—	75	—
Output to Output Skew	$t_{osLH}$ $t_{osHL}$	(Note 1)	$3.3 \pm 0.3$	50	—	—	1.5	—	1.5
			$5.0 \pm 0.5$	50	—	—	1.0	—	1.0
Input Capacitance	C <sub>IN</sub>			—	4	10	—	10	
Output Capacitance	C <sub>OUT</sub>			—	6	—	—	—	
Power Dissipation Capacitance	C <sub>PD</sub>	(Note 2)		—	32	—	—	—	

Note (1) Parameter guaranteed by design.  $t_{osLH} = |t_{pLHm} - t_{pLHn}|$ ,  $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

And the total C<sub>PD</sub> when n pcs. of Latch operate can be gained by the following equation :

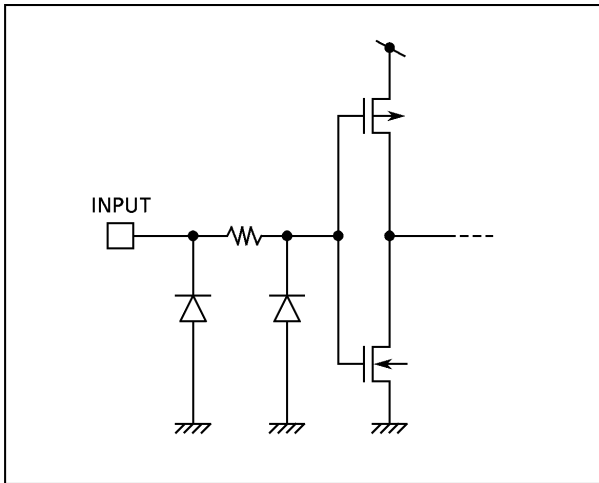
$$C_{PD} \text{ (total)} = 20 + 12 \cdot n$$

NOISE CHARACTERISTICS ( Input  $t_r = t_f = 3\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V <sub>CC</sub> (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50pF	5.0	0.5 (0.6)	0.8 (0.9)	V
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50pF	5.0	-0.5 (-0.6)	-0.8 (-0.9)	V
Minimum High Level Dynamic Input Voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50pF	5.0	—	1.5	V

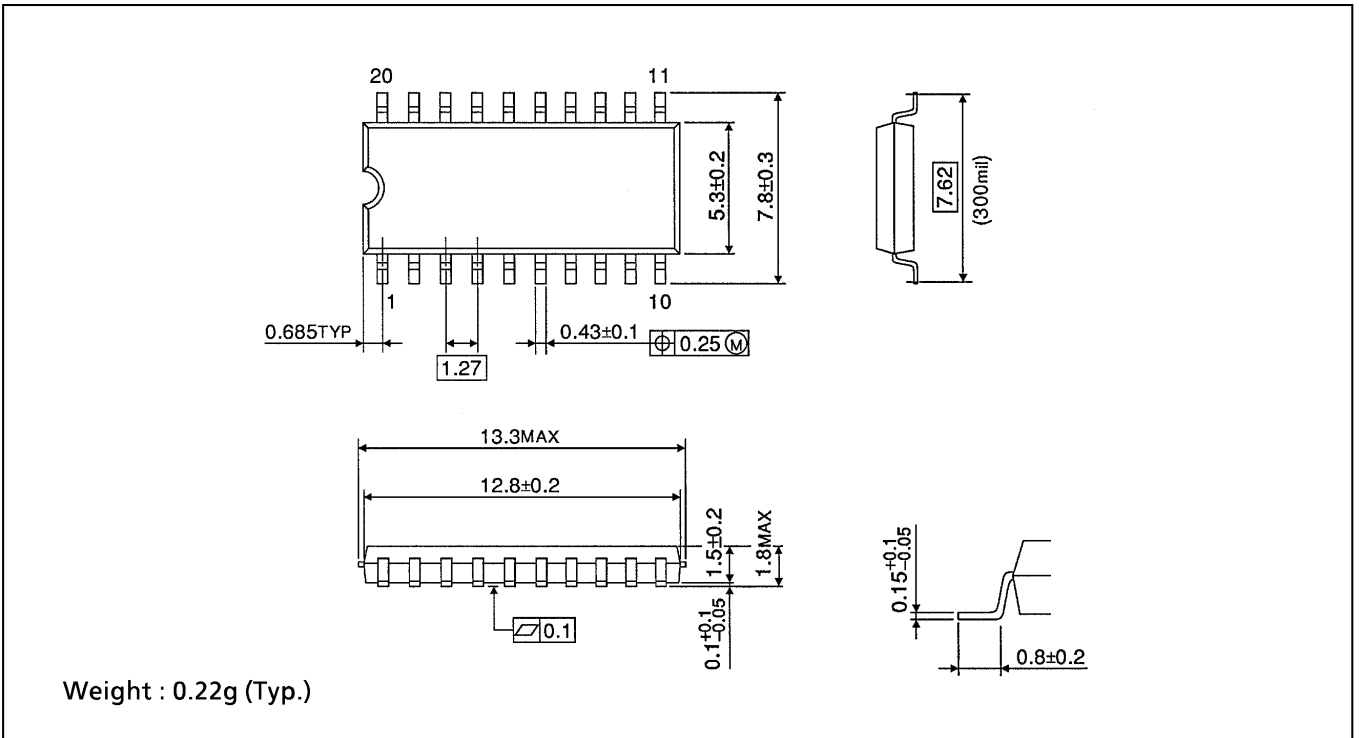
(Note) The value in ( ) only applies to JEDEC SOP (FW) devices.

INPUT EQUIVALENT CIRCUIT



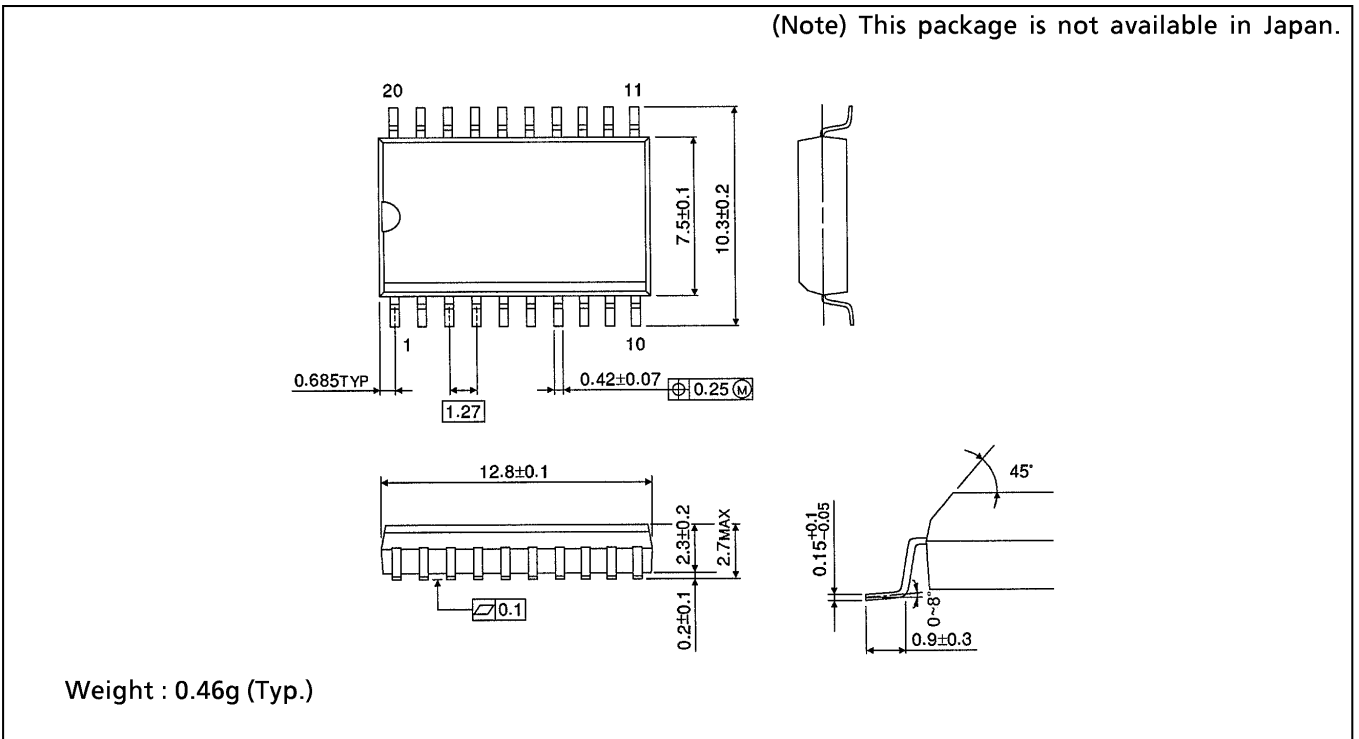
SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

Unit in mm



SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

Unit in mm



TSSOP 20PIN PACKAGE DIMENSIONS (TSSOP20-P-0044-0.65)

Unit in mm

