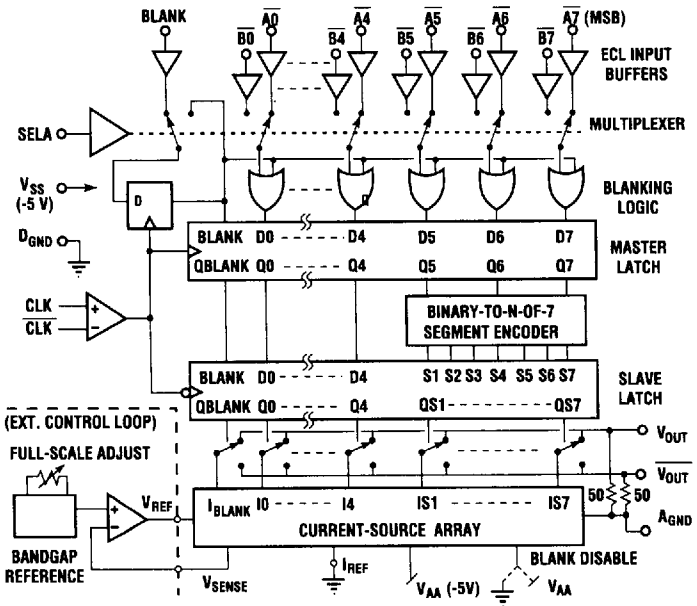
TQ6122

1 Gigasample/sec, 8-bit Digital-to-Analog Converter



TriQuint's TQ6122 GIGADAC™ is a monolithic, 8-bit digital-to-analog converter capable of conversion rates to at least 1000 Megasamples/second. The TQ6122 DAC may be used for display generation, waveform and signal synthesis, and video signal reconstruction. The TQ6122 features a 2:1 data MUX at the input for ease of interface and offers synchronous blanking capability for maximum ease of use in video applications. It drives complementary 1 V peak-to-peak swings into 50-ohm loads; on-chip 50-ohm reverse terminations provide extremely fast settling time.

Due to the inherently high speed of TriQuint's one-micron gate Enhancement / Depletion-mode gallium arsenide process, the TQ6122 offers guaranteed operation at clock rates of 1000 MHz, with typical room temperature conversion rates of 1.5 Gs/s without multiplexing and 1.3 Gs/s when using multiplexed inputs. The TQ6122 features output rise and fall times of 500 ps (10% – 90%), symmetric complementary output transitions, and glitch impulse values less than 10 pV/sec. When used for sine wave synthesis, typical spurious and harmonic free dynamic range is 45 dBc.

The TQ6122 may be retrofitted into designs which currently use TriQuint's TQ6111, 2, 3, 4M DACs with minimal changes to power supply levels and input and output connections. The part is available in a 44-pin ceramic package or as unpackaged die.

Features

- *1 Gs/s conversion rate*
- *8-bit resolution*
- *DC differential non-linearity $^1/_2$ LSB (0.2%)*
- *DC integral non-linearity 1 LSB (0.4%)*
- *Settling time 2 ns to 0.4% (est.)*
- *Spurious-free dynamic range (SFDR) 45 dBc typical*
- *ECL-compatible inputs*
- *Synchronous blanking input*
- *1.3 W power dissipation*
- *44-pin multilayer ceramic package or unpackaged die*

Applications

- *Display generation*
- *Waveform and signal synthesis*
- *Video signal reconstruction*

MIXED SIGNAL PRODUCTS

Specifications

Table 1. Absolute Maximum Ratings (1,2)

Symbol	Description	Min	Typ	Max	Units
A_{GND}, D_{GND}	Analog and digital ground	–2		+2	V
V_{SS}	Digital power	–7			V
V_{AA}	Analog power	–10			V
V_O, $\overline{V_O}$ (MAX)	Analog output (1 V F.S.)	–2.5		+2.5	V
V_I (MAX)	Digital input levels	V_{SS} –0.5		+0.5	V
I_I (MAX)	Digital input currents	–1		+1	mA
P_D	Power dissipation			3.0	W
T_C	Case backside temperature	–65		+135	°C
T_S	Storage temperature	–65		+150	°C

Notes: 1. Unless otherwise specified: $A_{GND} = D_{GND} = 0$ V, $V_{SS} = V_{AA} = -5$ V, $V_{FS} = 1$ V pk–pk, case temperature = 27 °C.
2. Exceeding the absolute maximum ratings may damage the device. The value shown for a particular parameter is determined with all other parameters at their nominal values.

Table 2. DC Characteristics (1)

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{AA}	Analog supply	Note 2	–5.25		–4.75	V
I_{AA}	V_{AA} current	V_{FS} = 1 V pk–pk	50	62	80	mA
V_{SS}	Digital supply	Note 2	–5.5		–4.5	V
I_{SS}	V_{SS} current		145	200	265	mA
P_D	Power dissipation		0.9	1.3	1.85	W
V_{ECLREF}	ECL reference level	Note 3, Figure 1	–1.5	–1.3	–1.1	V
I_{ECLREF}	ECL ref. input bias current	Note 3, Figure 1 $\Delta V_{ECLREF} = \pm 0.2$ V	–5	0	+5	mA
R_{ECLREF}	ECL ref. input resistance	Figure 1		50		
C_{ECLREF}	ECL ref. input capacitance			2		pF
$V_{IH(DC)}$	Data input HIGH (ECL)	DC value (V_{ECLREF} = –1.3 V)	–1100		–500	mV
$V_{IL(DC)}$	Data input LOW (ECL)	DC value (V_{ECLREF} = –1.3 V)	V_{TT}		–1500	mV
V_{CLKH} (DC), $\overline{V_{CLKH}}$ (DC)	Clock HIGH input	Differential clock, Note 4	V_{ECLREF} +0.3		–0.7	V
V_{CLKL} (DC), $\overline{V_{CLKL}}$ (DC)	Clock LOW input	Differential clock, Note 4	V_{TT}		V_{ECLREF} –0.3	V
I_{IN}	Data, clock input bias current	V_{IH} = –800 mV, V_{IL} = –1800 mV	–25		+25	uA
C_{IN}	Data, clock input capacitance	In multilayer ceramic package		0.5		pF
V_{OUT} (MAX), $\overline{V_{OUT}}$ (MAX)	Maximum absolute output level	Note 5			+1	V
V_{OUT} (MIN), $\overline{V_{OUT}}$ (MIN)	Minimum absolute output level	Note 5	–1.5			V

(Continued on next page)

Table 2. DC Characteristics [1] *(continued)*

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{FS}	Full-scale output swing	Data bits only, 0–0/1–1 input step R_L = 50 load	0	1	1.125	V pk–pk
V_{ZS}	Zero-scale offset	V_{FS} = 1 V, no external offset, $V_{BLANK\_DISABLE}$ = 0 V		–35		mV
D V_{BLANK}	Blanking interval	Blank input = 1, Notes 6, 7	9	10.4	12	%V_{FS}
$V_{BLANK\_DISABLE}$	Blank current disable control	Blank current ON Blank current OFF		–5 (V_{AA}) 0 (A_{GND})		V V
V_{REF}	V_{REF} input voltage	V_{FS} = 1 V peak-to-peak V_{FS} = 0 V peak-to-peak	V_{AA}+0.7 V_{AA}–1	V_{AA}+1.0	V_{AA}+1.4	V V
V_{SENSE}	V_{SENSE} output	V_{FS} = 1 V peak-to-peak		V_{AA}+0.8	V_{AA}+1.1	V
I_{VREF}	V_{REF} input current	V_{REF} = V_{AA} +0.65 V_{REF} = V_{AA} +1.1		10	 1	uA mA
I_{REF}	Ext. reference current output	V_{FS} = 1 V peak-to-peak	2	2.5	5	mA
V_{IREF}	I_{REF} terminal voltage		–1.5		+1	V
R_{OUT}, $\overline{R_{OUT}}$	V_{OUT}, $\overline{V_{OUT}}$ output resistance Matching of R_{OUT}, $\overline{R_{OUT}}$		44	50 0.2	57 2.5	 %
C_{OUT}	V_{OUT}, $\overline{V_{OUT}}$ output capacitance			0.3		pF
	Resolution				8	Bits
	Monotonicity		8			Bits
DNL	Differential non-linearity	(± $^1/_2$ LSB)			0.2	% F.S.
INL	Integral non-linearity	(± 1 LSB)			0.4	% F.S.
	Full-scale symmetry	V_{FS} = 1 V peak-to-peak, Note 8	–4		+4	mV
	V_{FS} temperature coefficient	Note 9				

Notes: 1. Unless otherwise specified: V_{AA} = –5V ± 5%, V_{SS} = –5 V ±10%, V_{TT} = –2V ± 5%, V_{FS} = 1 V pk–pk, T_{CASE} = 0 to +85 °C

2. See the "Power Supplies, Ground and Bypassing" section later in this datasheet for discussion of power supplies.

3. The ECL reference input establishes the switching point for the ECL line receivers used at the DATA, BLANK, and SELECT inputs. (See Figure 1.) I_{ECLREF} is the current required to change the internal ECLREF value by about ±200 mV.

4. Values shown are for differential clock drive, and apply to both CLOCK and $\overline{CLOCK}$ inputs. For single-ended drive, the HIGH level should be at least (V_{ECLREF} +0.5) volts, but must not exceed –700 mV. The LOW level should be (V_{ECLREF} –0.5) volts, but must not go below V_{TT}, where V_{TT} is the ECL termination voltage (nominal V_{TT} = –2 V).

5. $V_{OUT(MAX)}$, $\overline{V_{OUT(MAX)}}$, $V_{OUT(MIN)}$, $\overline{V_{OUT(MIN)}}$ represent the limits on the absolute output levels, including offset.

6. Blanking interval is the voltage change (as a percentage of the full-scale output swing) added to V_{FS} when BLANK is asserted.

7. The BLANK DISABLE input turns OFF the blank current (DV_{BLANK} = 0) when held at A_{GND}, and turns it ON when pulled to V_{AA}.

8. Full-scale symmetry is a measure of the balance between V_{OUT} and $\overline{V_{OUT}}$. For a full-scale input change (00000000 –> 1111111), the change in $\overline{V_{OUT}}$ will match the change in V_{OUT} to within ± 4 mV (1 LSB @ 1 V peak-to-peak).

9. The VFS temperature coefficient is determined primarily by the external reference and loop control op amp.

Table 3. AC Characteristics (1,2)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
F_{CLK} (MAX)	Maximum clock frequency	Unmuxed operation	1000	1500		MHz
		Muxed operation	1000	1300		MHz
$T_{RCLK,DATA}$	Clock, data input rise time	20% to 80%		300		ps
$T_{FCLK,DATA}$	Clock, data input fall time	20% to 80%		300		ps
T_{WH}	Duration of clock HIGH	Percentage of clock period	40	50	60	%
T_{WL}	Duration of clock LOW	Percentage of clock period	40	50	60	%
T_{SETUP}	Data, control setup time	See Figure 7				ps
T_{HOLD}	Data, control hold time	See Figure 7				ps
T_{ROUT}	Output rise time	10% to 90%		300		ps
T_{FOUT}	Output fall time	10% to 90%		300		ps
T_{SETTLE}	Output settling time	Within ±0.4% of final value		2		ns
	Glitch impulse				10	pV/sec

Notes: 1. Unless otherwise specified: V_{AA} = −5V ± 5%, V_{SS} = −5 V ± 10% , V_{FS} = 1 V p−p, T_{CASE} = 0 to +85 °C, V_{ECL} = −1.3 V, V_{IH} = −0.8 V, V_{IL} = −1.8 V
2. Applies to packaged parts only.

Figure 1. ECL Reference Input Equivalent Circuit

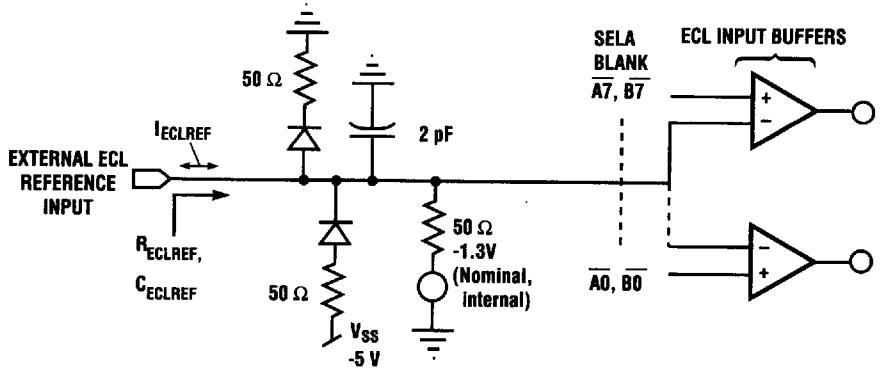


Figure 2. Definition of V_{IH}, V_{IL} for Data and BLANK Inputs

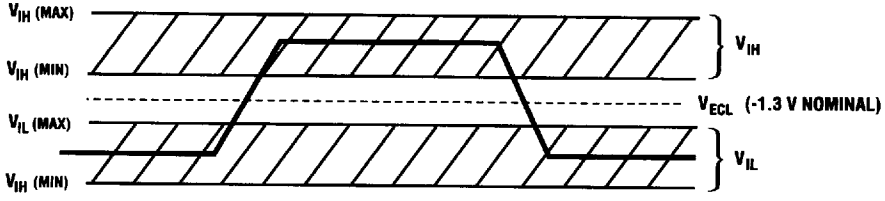


Figure 3. Typical Digital Input Circuit (Including CLOCK Inputs)

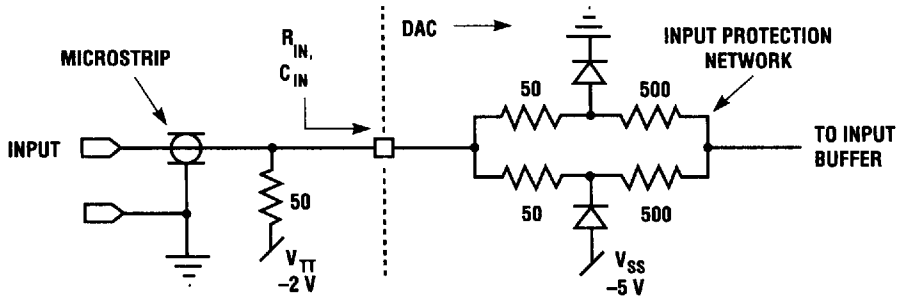


Figure 4. V_{OUT}, $\overline{V_{OUT}}$, and Input Code Relationships for (A) Typical Instrumentation and (B) Video Configurations

(A) TQ6122 Instrumentation DAC operation (1 V Full-Scale)

Blanking current is shunted to ground by tying BLANK DISABLE to A_{GND} and forcing BLANK = 0.

	Input Code	V_{OUT} (1)	$\overline{V_{OUT}}$ (1)
Full Scale	11111111	−0.996 V	0.000 V
Full Scale − 1 LSB	11111110	−0.992 V	−0.004 V
Half Scale + 1 LSB	10000001	−0.504 V	−0.492 V
Half Scale	10000000	−0.500 V	−0.496 V
Half Scale −1 LSB	01111111	−0.496 V	−0.500 V
Zero Scale + 1 LSB	00000001	−0.004 V	−0.992 V
Zero Scale	00000000	0.000 V	−0.996 V

(B) TQ6122 Video DAC Operation (0.679 V Full-Scale)

Blanking current is enabled by connecting BLANK DISABLE to V_{AA}.

	Input Code	V_{OUT} (1)	$\overline{V_{OUT}}$ (1)
Full Scale	11111111	−0.679 V	−0.071 V
Full Scale − 1 LSB	11111110	−0.676 V	−0.074 V
Half Scale + 1 LSB	10000001	−0.343 V	−0.407 V
Half Scale	10000000	−0.341 V	−0.409 V
Half Scale − 1 LSB	01111111	−0.338 V	−0.412 V
Zero Scale + 1 LSB	00000001	−0.003 V	−0.747 V
Zero Scale	00000000	0.000 V	−0.750 V
BLANK = HIGH	X X	−0.750 V	0.000 V

Notes: 1. All values shown for V_{OUT} and $\overline{V_{OUT}}$ assume identical load resistors (RL1 and RL2 in Figure 5), and no externally imposed output offset voltage (V_{OS} in Figure 5). Zero-scale offset is ignored.

Figure 5. Output Equivalent Circuit, Showing Terminated 50-ohm Transmission Line Loads

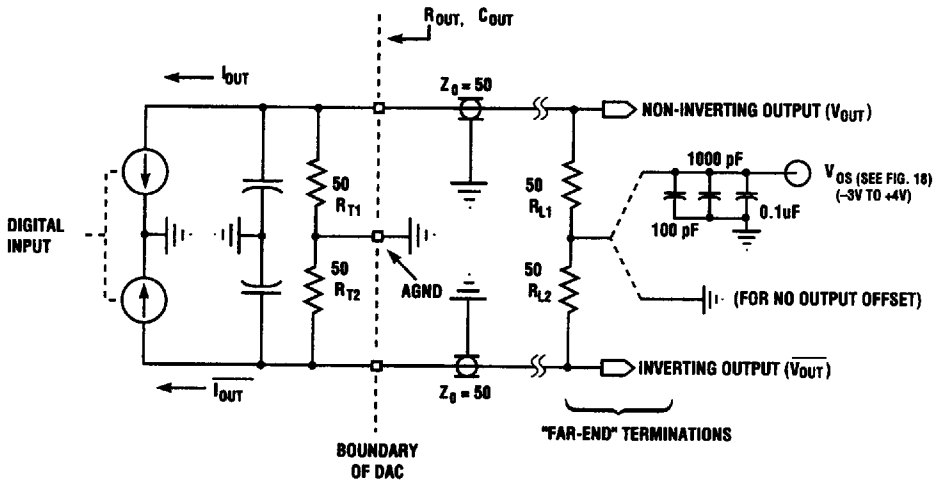


Figure 6. Definition of T_{WH} and T_{WL}

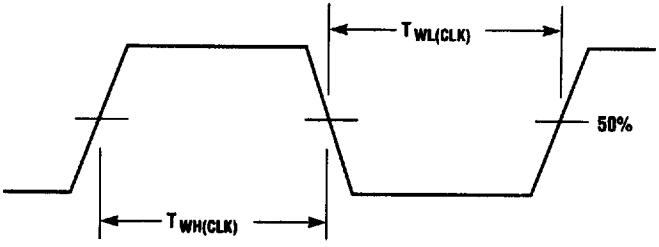
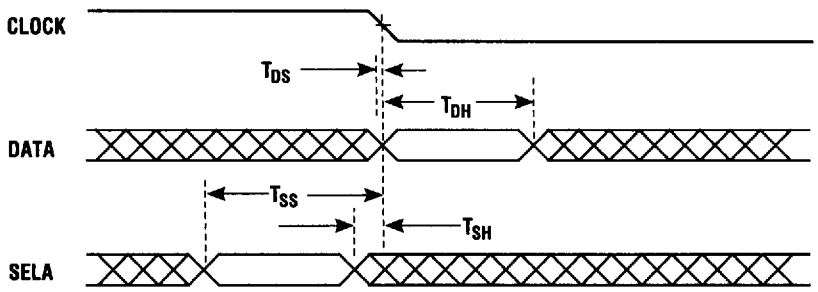


Figure 7. TQ6122 Data and Control Timing



Symbol	*Description*	*Typical @ 25 °C*	*Unit*
T_{DS}	Data setup time (1)	0	ps
T_{DH}	Data hold time (2)	+325	ps
T_{SS}	SELA setup time (1,3)	+350	ps
T_{SH}	SELA hold time (2,3)	–100	ps

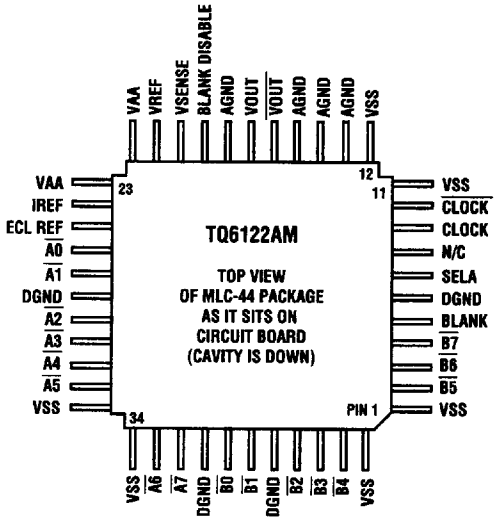
Notes: 1. Setup time is defined to be positive for data or control transitions occurring before the negative-going edge of the clock.
2. Hold time is defined to be positive for data or control transitions occurring after the negative-going edge of the clock.
3. While SELA does not strictly have a setup and hold time, it is convenient to express its allowed transition region limits in these terms.

Mechanical Characteristics

The TQ6122 DAC is packaged in a proprietary 44-pin multilayer ceramic package which provides high-speed, controlled-impedance interconnects and integral power supply bypassing. The leads are set on 0.050" centers, and are formed for gull-wing surface mounting. Figure 8 shows the pinout diagram of the packaged IC as seen from the top, opposite the cavity side; Figure 9 lists pin numbers, names and I/O levels. Figure 10 illustrates the pertinent dimensions of the package and Figure 11 shows the mounting footprint.

Since the TQ6122 dissipates on the order of 1.3 W, adequate heat sinking is essential for proper operation of the device. Figure 12 shows one possible heat sink arrangement based on a multi-finned "Top Hat" heat sink available from Thermalloy. An environment with a minimum of 100 fpm (feet per minute) of forced air cooling is assumed; >200 fpm is preferred.

Figure 8. TQ6122 Pinout



Notes: 1. A7, B7 = MSB inputs
2. N/C = no internal connection

Figure 9. TQ6122 Pin Descriptions

Pin	Signal	Interface Level (Typ.)
1, 11, 12, 33, 34, 44	V_{SS}	–5 V
2	$\overline{B5}$	600 mV pk–pk centered at –1.3 V @ DC
3	$\overline{B6}$	600 mV pk–pk centered at –1.3 V @ DC
4	$\overline{B7}$ (MSB)	600 mV pk–pk centered at –1.3 V @ DC
5	BLANK	600 mV pk–pk centered at –1.3 V @ DC
6, 28, 37, 40	D_{GND}	0 V
7	SELA	600 mV pk–pk centered at –1.3 V @ DC
8	—	No connection
9	CLOCK	1V pk–pk centered at –1.3 V @ AC
10	$\overline{CLOCK}$	1V pk–pk centered at –1.3 V @ AC
13–15, 18	A_{GND}	0 V
16	$\overline{V_{OUT}}$	0 V to –1 V
17	V_{OUT}	–1 V to 0 V
19	BLANK DISABLE	Enable = V_{AA} (I_{BLANK} = ON) Disable = A_{GND} (I_{BLANK} = OFF)
20	V_{SENSE}	V_{AA} + 0.8, for V_{FS} = 1 V pk–pk
21	V_{REF}	V_{AA} +1, for V_{FS} = 1V pk–pk
22, 23	V_{AA}	–5 V
24	I_{REF}	2.5 mA for V_{FS} = 1V pk–pk
25	ECL REF	–1.3 V
26	$\overline{A0}$ (LSB)	600 mV pk–pk centered at –1.3 V @ DC
27	$\overline{A1}$	600 mV pk–pk centered at –1.3 V @ DC
29	$\overline{A2}$	600 mV pk–pk centered at –1.3 V @ DC
30	$\overline{A3}$	600 mV pk–pk centered at –1.3 V @ DC
31	$\overline{A4}$	600 mV pk–pk centered at –1.3 V @ DC
32	$\overline{A5}$	600 mV pk–pk centered at –1.3 V @ DC
35	$\overline{A6}$	600 mV pk–pk centered at –1.3 V @ DC
36	$\overline{A7}$ (MSB)	600 mV pk–pk centered at –1.3 V @ DC
38	$\overline{B0}$ (LSB)	600 mV pk–pk centered at –1.3 V @ DC
39	$\overline{B1}$	600 mV pk–pk centered at –1.3 V @ DC
41	$\overline{B2}$	600 mV pk–pk centered at –1.3 V @ DC
42	$\overline{B3}$	600 mV pk–pk centered at –1.3 V @ DC
43	$\overline{B4}$	600 mV pk–pk centered at –1.3 V @ DC

Figure 10. Package Dimensions

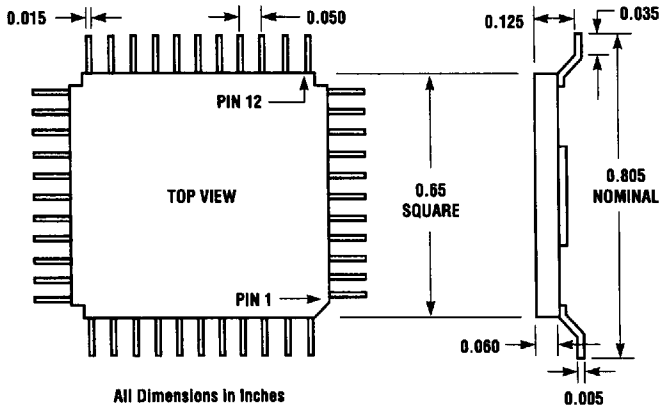


Figure 11. Mounting Footprint

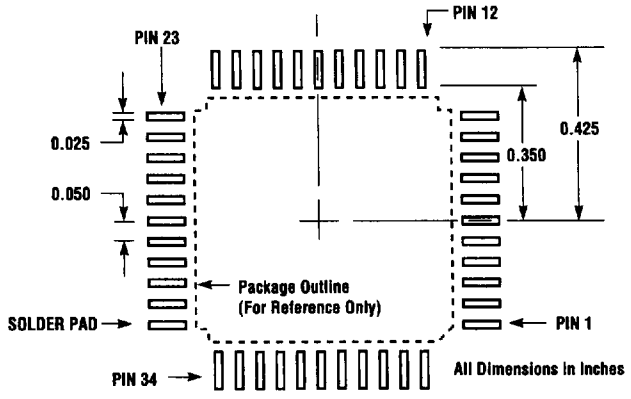
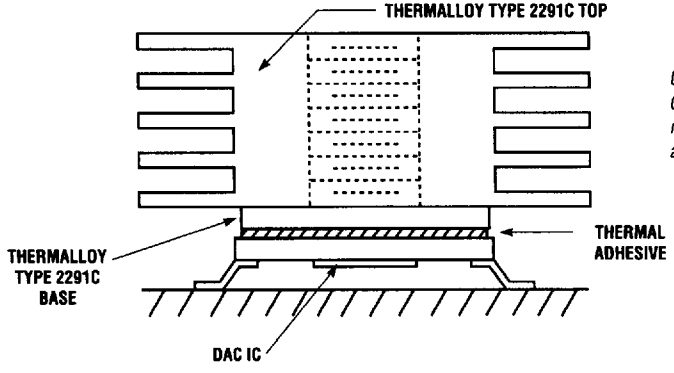


Figure 12. Heat-Sink Mounting Arrangement (heat sink not included)



Use Loctite "Output" Thermal Conductive Adhesive (Loctite item number 00241) or equivalent to attach heat sink base to IC.

Circuit Description

The TQ6122 DAC is based on a current-steering architecture in which weighted currents are switched by an array of differential-pair switches into either the V_{OUT} or $\overline{V_{OUT}}$ output, depending on the state of the input data and blanking bits. Essentially, the DAC is comprised of six circuit blocks: the input buffer, the data multiplexer, blanking logic, master/slave latch array with segment encode logic, differential-pair switches, and the current source array. (See figure on page 1.)

Input Buffers

The input buffers compare the ECL data and control input signals with the ECLREF level, amplify the difference, and translate this signal to the logic levels used within the IC. By default, the ECL reference is set by an internal generator; however, for best performance and maximum noise margin over temperature, power supply, and device-to-device variations, the user should provide an external level. For general-purpose applications, a simple resistive divider between D_{GND} and V_{TT} will suffice. For extreme environments or for maximum performance, the ECLREF level should be slaved to the centerpoint of the incoming data. Refer to the "Digital Inputs and Terminations" discussion later in this document for additional information.

Note that the data inputs are complemented to indicate that an increasing input value results in the V_{OUT} level moving more negative.

Data Multiplexer

The DAC makes provision for accepting data from either of two sources: from a single 8-bit-wide word at the full conversion rate, or from two 8-bit-wide half-speed words which are multiplexed together inside the DAC under the control of the SELA input. In use, the SELA input is set HIGH to select the A-Word data and LOW to select the B-Word. It is generally best to use the A-Word input when operating the DAC unmultiplexed, although the B-Word supports full-rate transfers.

Blanking Logic

A separate BLANK input is included to allow the DAC to be used in video display applications. When asserted LOW, the BLANK input has no effect on the operation of the DAC, and the state of the input data words controls the positions of the current switches. When BLANK is asserted HIGH, however, all internal data bits and the internal blanking bit are synchronously forced HIGH at the next negative-going clock transition, causing the V_{OUT} output to go to its most negative level. This level is the sum of the normal level associated with an input code of 11111111 plus the increment due to the blanking current being steered away from the $\overline{V_{OUT}}$ output to V_{OUT}. See Figure 4 (B).

In order to provide more latitude in the timing of the BLANK signal, the BLANK input is sampled only when the A-Word is selected. When the B-Word is selected, the state of the BLANK input at the time the SELA control line goes LOW is held stable until SELA again goes HIGH. In situations where blanking is not used, it is important that the BLANK input be tied to a solid logic LOW to prevent accidental assertion of BLANK = HIGH. Note also that when the DAC is used in the unmultiplexed mode, the data should be brought in on the A-Word inputs, since with SELA = LOW (as would be the case for B-Word operation), a transient HIGH level at the BLANK input would never be cleared and the DAC would lock up.

The BLANK_DISABLE pin is normally tied to the V_{AA} rail, allowing I_{BLANK} to flow to the differential-pair switch and then to the selected output. For applications which do not use blanking, however, the standing offset in the $\overline{V_{OUT}}$ output due to the unswitched

blanking current would be undesirable. For cases such as these, the blanking current may be completely turned off by connecting the BLANK_DISABLE pin to A_{GND}.

Master/Slave Latch With Encode Logic

A nine-wide master latch registers the data coming from the multiplexer and blanking logic. The latch outputs are then split into two groups. The top three bits are translated into a seven-level thermometer code by a binary-to-N-of-seven encoder, while the lower five data bits and the blanking bit are simply delayed. The seven encoder outputs and the six delayed data and blanking bits are re-registered in a slave latch to minimize skew, which, in turn, reduces the glitch impulse. Latch timing is set up such that the slave latch is in the "sample" mode when the input clock is LOW, meaning that the analog output is updated at the falling edge of the clock.

Current Switches

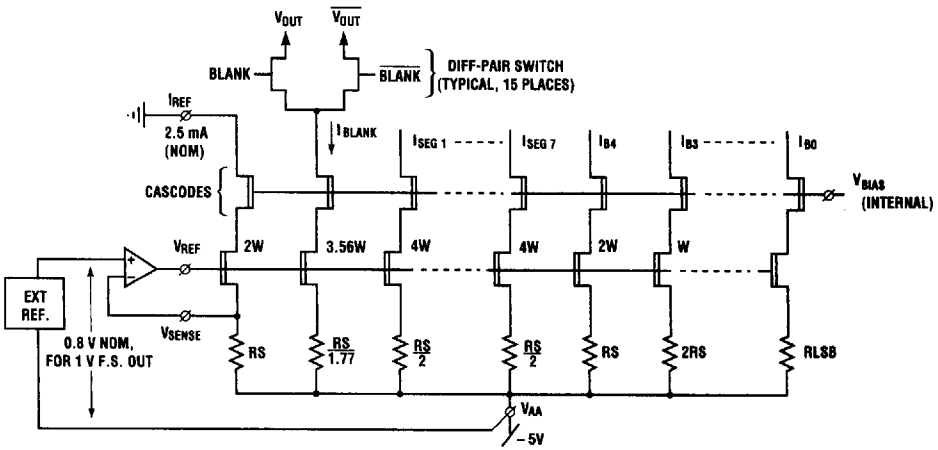
The thermometer code outputs of the slave latch array drive seven switches, each of which steers a current equal to 1/8 of the full-scale step amplitude. The five encoded data bits, on the other hand, switch currents with effective binary weightings from 1/16 of full scale down to 1/128 of full scale. The blanking bit steers a current which is nominally 10.4% of the full-scale amplitude.

Current-Source Array

The current-source array is the heart of the DAC from an analog standpoint, and is responsible for generating the segment, bit, and blanking currents. The maximum full-scale current I_{FS} (less I_{BLANK}) is about 45 mA, providing a 1.125 volt maximum swing into the 50-ohm external load. The blanking current is nominally 10.4% of I_{FS}, corresponding to a 10-unit IRE blanking interval of 71 mV when the full-scale output is set to 0.679 volt. The I_{REF} current tracks I_{FS}, with a nominal value of 2.5 mA for I_{FS} = 40 mA (i.e., 6.25% of I_{FS}).

Figure 13 (A) illustrates the basic circuit of the current-source array, which consists of a set of current sources ranging from the 5 mA segment currents to the binary-weighted current sources for the lower-order bits. The circuit design utilizes source degeneration, averaging, and linear gradient cancellation techniques to obtain matching consistent with up to 10-bit linearity.

Figure 13 (A). Current-Source Array Circuit — V_{SENSE}-Based Control Method

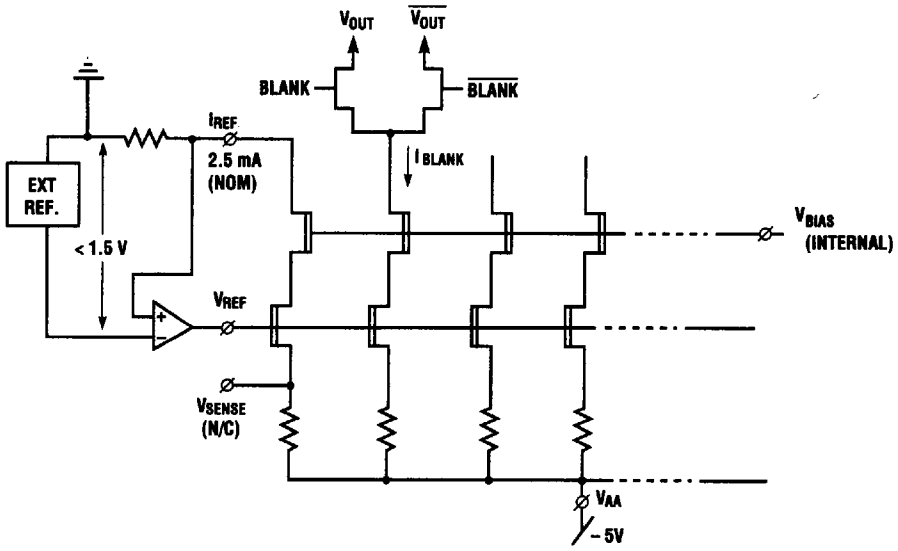


The absolute value of the current-source array output is determined using an off-chip (silicon) reference generator and op amp in a feedback-loop arrangement. In Figure 13 (A), the drop across the source degeneration resistors is compared with the level set by the external reference. Under conditions of 1 V peak-to-peak full-scale output swing, the voltage between the V_{SENSE} and V_{AA} pins of the DAC will be in the range of 0.8 V to 1.1 V, with V_{REF} being in the range of 0.7 V to 1.4 V (i.e., V_{REF} may lie above or below V_{SENSE} by several hundred millivolts). Note that, for this control method, the I_{REF} terminal must be connected to ground.

An alternative means of controlling the current-source array output is shown in Figure 13(B), with the advantage that now the reference current is being sensed *after* flowing through a path identical to that of the bit and segment currents. Thus, any error which may have occurred due to leakage will be directly corrected. Here, the V_{SENSE} pin is left disconnected and the I_{REF} current flows to ground through a stable resistor. The value of the resistor should be chosen to drop about 1 volt under the desired operating conditions, but under no circumstances should the voltage at the I_{REF} pin be allowed to drop below –1.5 V, or the linear relationship between I_{REF} and I_{FS} will be degraded.

The primary limitation on the maximum output current is the adjustment range of V_{SENSE}: if the value of $\{V_{SENSE} - V_{AA}\}$ exceeds about 1.2 V, the bottom current-source FETs begin to lose "headroom" by running up against the sources of the cascode transistors, causing the total current to begin limiting, as well as degrading, the linearity. If the designer is willing to accept somewhat degraded linearity and/or slightly higher power dissipation, V_{AA} may be taken down to –6 volts or so, allowing V_{REF} to be adjusted to give $\{V_{SENSE} - V_{AA}\}$ a maximum value of about 1.5 V. This translates to an output current of about 50 mA or 1.25 V peak-to-peak into the load. Note that under these conditions, the device will not sustain any damage, but full-spec operation of the DAC is not guaranteed.

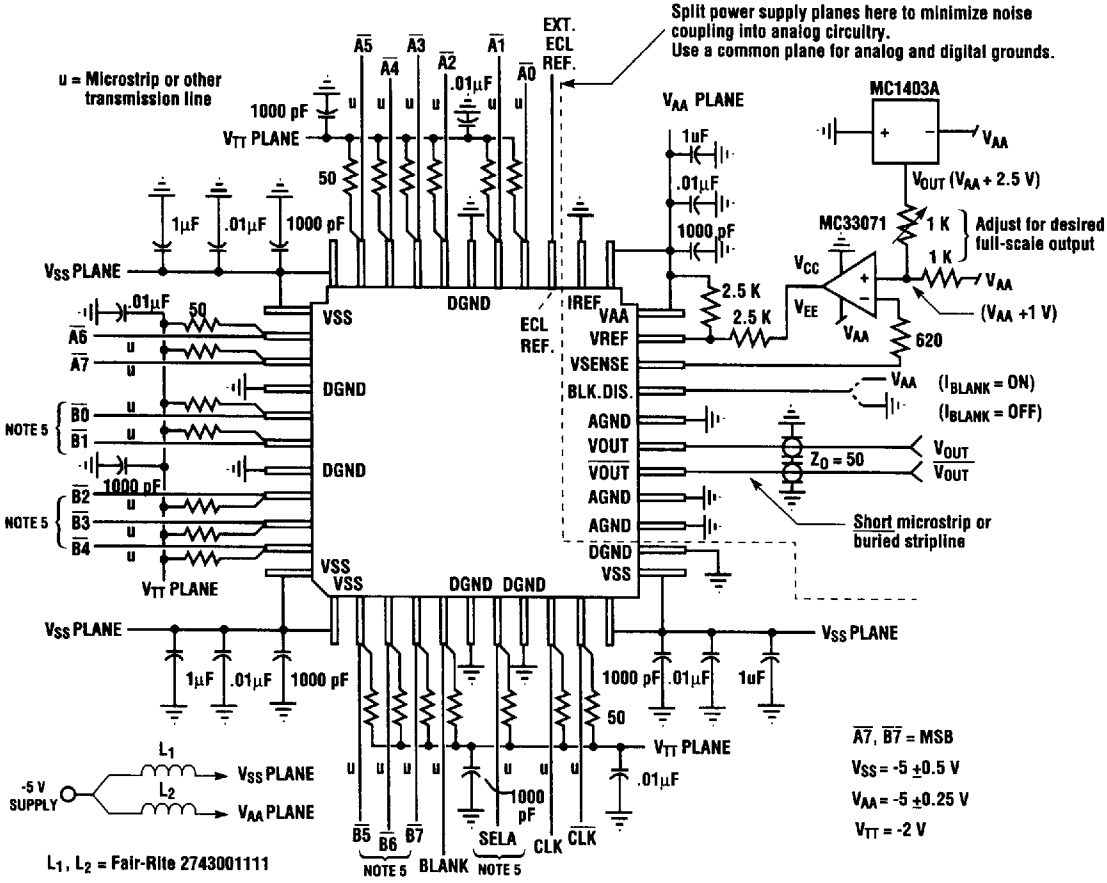
Figure 13 (B). Current-Source Array Circuit — I_{REF}-Based Control Method



Application Information

Figure 14 illustrates the basic connection of the DAC, showing details for power supplies, data and clock inputs, and outputs terminated in 50-ohm transmission line loads. Some issues relating to circuit board layout are also addressed.

Figure 14. Basic DAC Setup



Notes: 1. All resistors to V_{TT} are 50-ohm, 1/8 Watt, surface-mount, mounted as close to the IC as possible.

2. All V_{SS} and V_{TT} capacitors are rated 15 V. All V_{AA} capacitors are rated 25 V.

3. Use either surface-mount components or keep minimum-length leads on all resistors and capacitors.

4. For best noise isolation, the analog supply (V_{AA}) and digital supply (V_{SS}) should connect at only one point, via decoupling networks such as ferrite beads.

5. The input circuitry for $\overline{B0}$–$\overline{B7}$, BLANK, and SELA are the same as for $\overline{A0}$–$\overline{A7}$.

6. For questions regarding board layout, please contact the factory.

Power Supplies, Ground and Bypassing

To minimize noise coupling, the digital and analog power supplies should be returned to a single-point ground, and power supply buses to the IC should have minimum impedance (power planes are best).

The supplies themselves should be well bypassed at high and low frequencies, which requires the use of several different parallel capacitors as shown. The values are not particularly critical; however, due to the fact that a capacitor looks inductive above its self-resonant frequency, one needs to use several different values in parallel, ranging from microfarads to nanofarads, in order to provide adequate wideband bypassing.

For best results, use leadless ceramic chip capacitors for bypassing, although leaded components will work satisfactorily if higher noise can be tolerated. A common ground plane has been found to give the best performance.

For best results and minimum noise, the digital and analog supplies should be physically separated on the circuit board. When using a common –5 V feed, the V_{SS} and V_{AA} planes should be isolated by ferrite beads (Fair-Rite P/N 2743001111 or equivalent) as shown in Figure 14. Using separate LM337MT regulators downstream of the ferrite beads will provide better isolation.

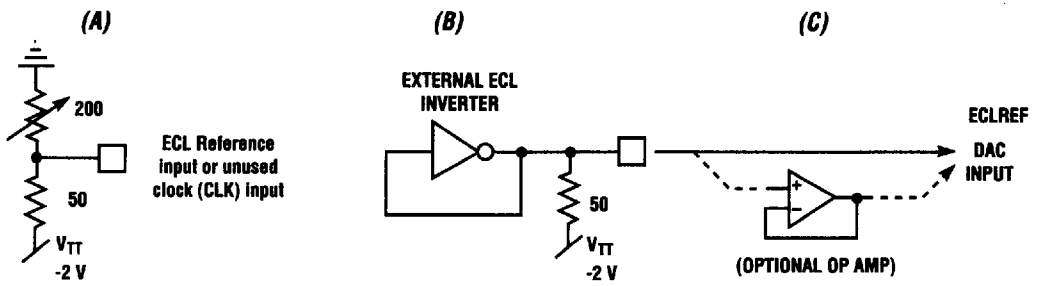
Digital Inputs and Terminations

The TQ6122 DAC is designed to accept ECL logic levels at all data and control inputs. All ECL inputs, with the exception of the clock (see below), are single-ended and are compared to the ECL threshold reference of –1.3 Volts (nominal) in the input buffers of the DAC.

The ECL reference input equivalent circuit is shown in Figure 1. Several options are available to the user for externally setting the ECL reference level. The simplest option is that of a voltage divider between D_{GND} and V_{TT}, setting the ECL termination voltage as shown in Figure 15 (A). The nominal value for ECLREF is –1.3 V; however, due to input offset variations among the input buffers or variations in V_{TT}, some adjustment above or below –1.3 V may give the best results.

A good way to settle ECLREF is to slave the ECL reference level to the center (switching) point of the input data signal. This may be accomplished in two ways: either use the V_{BB} generator output of the device which is generating the ECL signals supplied to the DAC, or use an inverter with input and output connected together to generate a level equal to the switching threshold. See Figure 15 (B). Note that the ECLREF generator should be able to source and sink up to approximately 5 mA, since the input resistance is about 50 ohms, against an internal –1.3 V (nominal) voltage source. An additional op amp may be used to give more flexibility or more robust drive. See Figure 15 (C).

Figure 15. External ECL Reference Generator



Clock Input

In order to realize the full speed potential of the DAC, a clock with an input swing of at least 1 V peak-to-peak, nominally centered on –1.3 V, is required. The clock may be applied in either single-ended or differential fashion. Because a differential clock provides maximum speed and best control of the relationship between clock and output transitions, as well as minimum noise, it is the preferred solution. For single-ended clock drive, the customer must drive the unused CLOCK input with an external ECL reference level, which may be generated using a resistive divider or, for best results, an external inverter tied back on itself. See Figure 15.

Input Line Termination

As shown in Figure 14, data, control, and clock inputs should be terminated in 50 ohms to V_{TT}, consistent with good ECL practice. For best results, keep terminations physically small — surface-mount "chip" resistors work very well — and locate them as close to the IC as possible. The V_{TT} bus should also be locally bypassed to digital ground, using chip capacitors placed close to the terminations. The DAC offers good performance for $-2.5\ V \le V_{TT} \le -2\ V$, where the use of $V_{TT} < -2$ V may allow the designer to eke out the last bit of performance in a noisy or marginal drive-level environment.

Current-Source Control Loop

As illustrated previously in Figure 13, and shown in detail in Figure 16, the bit current sources are controlled by placing them in a feedback loop which compares the drop across a current-sensing resistor with a stable reference. For nominal 1 Volt full-scale output swing, the V_{REF}-to-V_{AA} voltage will be in the 0.8 to 1 V range, and may be derived from a zener or, better still, a bandgap reference such as the 2.5 V Motorola MC1403A. The output of the bandgap reference will have to be divided down before being applied to the control op amp, and some means should be provided to trim the output to compensate for V_{OUT} load resistor variations.

The op amp must have input common-mode and output drive ranges which extend down to within at least 0.5 Volt of the negative rail for maximum control range. For best noise immunity, both the reference generator and the op amp should share a point connection to the V_{AA} rail, close to the DAC. The Motorola MC33071 op amp is suitable for this application. Standard linear design techniques should be used to minimize thermal drift and offset. Note that the temperature coefficient of the nichrome resistors used in the DAC is on the order of +6 ppm/°C. Figure 16 shows a typical reference control loop circuit.

Fig. 16. Typical External Current-Source Control Loop

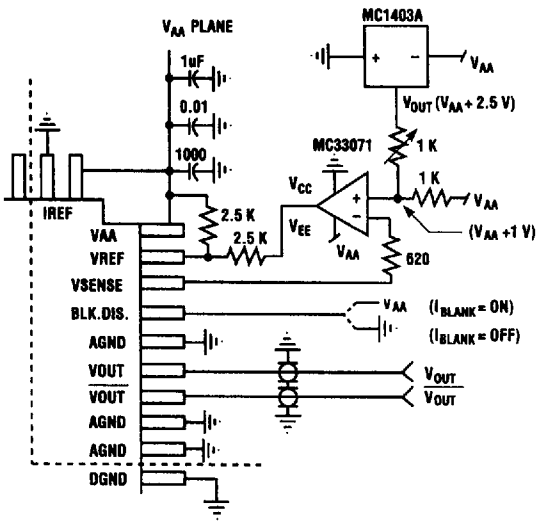
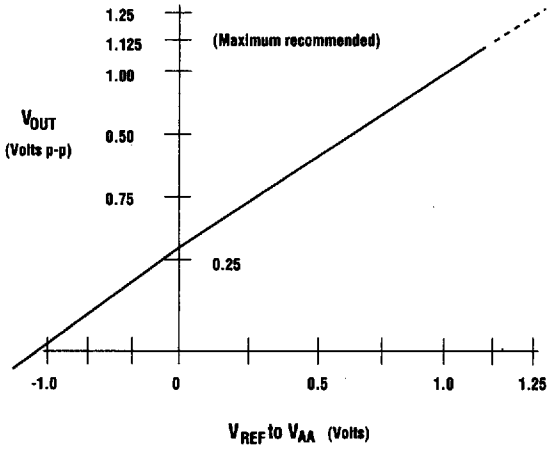


Figure 17 illustrates the relationship between control input V_{REF} and the full-scale output swing. Note that the full-scale swing may be reduced below 0.25 V peak-to-peak by pulling V_{REF} below V_{AA}. However, this necessitates a separate negative supply for the control

op amp and reference generator, which may decrease the V_{AA} supply rejection. In circuits which use different negative rails for the DAC V_{AA} supply and the op amp, V_{REF} should be clamped to no more than two diode drops below V_{AA}, and a current-limiting resistor should be included at either the op amp output or between its negative supply input and supply input. In the event of turn-on transients and large excursions in the op amp supply before V_{AA} has settled out, these precautions will help prevent breakdown of circuitry within the DAC.

Figure 17. Typical V_{REF}-to-V_{AA} Transfer Characteristics



Full-Scale Output Adjust

The procedure for setting the full-scale output range is quite straightforward, and involves monitoring the output level(s) using a DVM. With the DAC connected to its actual V_{OUT} and $\overline{V_{OUT}}$ load(s), the output is alternately switched between steady state zero- and full-scale levels, and the reference is adjusted until the desired full-scale transition amplitude is obtained. The clock must be running and the BLANK input set to "0". Alternatively, for a DDS application, a spectrum analyzer or a power meter may be used to monitor the full-scale output power.

Blanking Current Programming

The blanking current (I_{BLANK} in Figure 13) is turned off by connecting the BLANK_DISABLE pin to A_{GND} to divert the current away from the blank switch and the output of the DAC, and turned on by connecting BLANK_DISABLE to V_{AA}.

Output Equivalent Circuit

Figure 5 illustrates the equivalent circuit of the two DAC outputs. Each of the bit current sources is switched into either the V_{OUT} or the $\overline{V_{OUT}}$ output, depending on the data stored in the slave latches. A pair of internal 50-ohm resistors are connected from V_{OUT} and $\overline{V_{OUT}}$ to analog ground (A_{GND}), and provide reverse termination for the analog output transmission lines. Although in principle there is no restriction on the load impedance applied at the outputs, in practice, the best performance will be obtained when driving a 50-ohm terminated transmission line. This is very important from a settling standpoint, since reflections from non-50-ohm loads will superimpose with new transitions and interfere with settling. The general rule for terminating the outputs is "the cleaner, the better."

Output Zero-Scale Adjust

The output baseline, or "zero-scale" level, may be adjusted by returning the far-end termination resistors to a well-bypassed supply level other than ground. For this general situation, reference Figure 5, the instantaneous output voltages V_{OUT} and $\overline{V_{OUT}}$ are given by:

$$V_{OUT} = V_{OS}\left(\frac{R_{T1}}{R_{L1} + R_{T1}}\right) - |\, I_{OUT} \,|\, (R_{L1} \,||\, R_{T1})$$

$$\overline{V_{OUT}} = V_{OS}\left(\frac{R_{T2}}{R_{L2} + R_{T2}}\right) - |\, \overline{I_{OUT}} \,|\, (R_{L2} \,||\, R_{T2})$$

$$I_{OUT} = \left(\frac{\text{Digital Input}}{255}\right) I_{FS}$$

$$\overline{I_{OUT}} = \left(1 - \frac{\text{Digital Input}}{255}\right) I_{FS}$$

I_{FS} = Summation of all individual bit currents
Digital Input = Decimal equivalent of the binary input word

For the case of $R_{L1} = R_{L2} = R_{T1} = R_{T2} = 50$ ohms, V_{OS} is attenuated by 50%. An overriding factor in setting the output offset is the requirement that V_{OUT} and $\overline{V_{OUT}}$ always remain within the device's output compliance range of –1.5 V to +1 V. Note also that in the case of the video application of the DAC, the value of the blanking current I_{BLANK} and the state of the BLANK input must be included in the expressions for V_{OUT} and $\overline{V_{OUT}}$.

An alternative method of offsetting the output involves injecting an offset current at the output. This may be done using a current source in the form of either a resistor or a transistor as shown in Figure 18(A). The resistor has the advantage of minimizing perturbation of the transmission line impedance, with the disadvantage of requiring a large supply voltage. In general, a 1/8 to 1/4 W carbon-composition resistor with a value of 500 to 1000 ohms will give good performance. Keep the lead lengths short when attaching to the circuit board and bypass the driven terminal of the resistors with a 1000 pF to 0.01 µF SMT (surface-mount) capacitor network to the ground plane.

A transistor current source, on the other hand, requires much less power supply overhead, but adds more capacitance to the transmission line. If a transistor is used, it should be a high-F_T device with low C_{CB} or C_{DG} (0.5 pF , if possible) and installed with short leads.

Capacitive coupling provides a means of obtaining an output centered on 0 volts. However, simply adding a coupling capacitor at one (or both) of the outputs will cause the DC output level to exceed the –1.5 V output compliance limit. The way to circumvent this problem is to add an offset current between the DAC output and the coupling capacitor (as discussed above), or to add a low-loss 50-ohm pad between the DAC and the capacitor, as shown in Figure 18(B). A "T" or "π" attenuator topology is acceptable, having 1 dB to 3 dB of attenuation. The characteristic impedance must be consistent with the overall system impedance, typically 50 ohms. This approach works, although the lower limit on the output level tends to be very close to the –1.5 V compliance limit for 1 V full-scale output swings, so some care and verification will be required.

Figure 18(A). Alternate Output Offset Current Generators

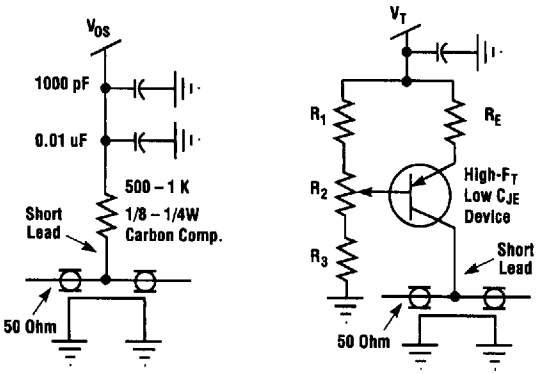
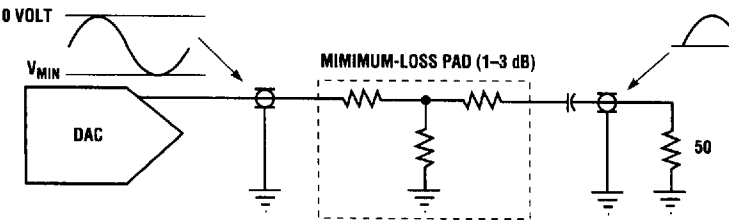


Figure 18(B). AC Coupling of Outputs



Note: V_{MIN} must not exceed the lower output compliance limit of –1.5 V for proper operation. If $V_{MIN} < -1.5$ V, decrease the DAC output swing by adjusting the V_{REF} drive to the control op amp.

Typical AC Performance

Figures 19 through 23 show typical AC performance of the TQ6122. Figures 19A and 19B illustrate the response of the DAC to an unmultiplexed counter input at 1 Gs/s and 1.5 Gs/s, respectively. Blanking is enabled in both cases.

The small glitches appearing at 1/8 of full-scale intervals are shown in more detail in Figure 22.

Figure 19 (A). Unmuxed Ramp at 1000 Ms/s with Blanking *(Guaranteed, 0 to +85 °C)*

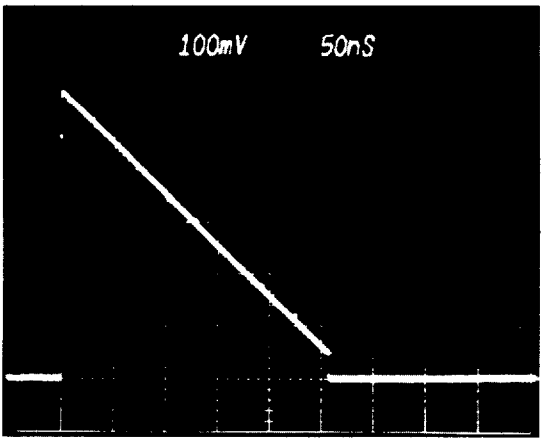
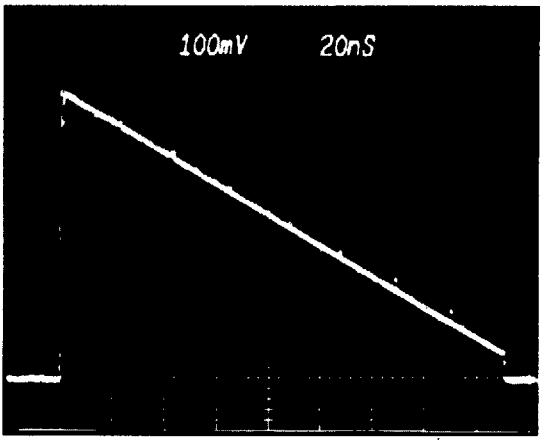


Figure 19(B). Unmuxed Ramp at 1500 Ms/s with Blanking *(Typical, +25 °C)*



Multiplexed behavior is shown in Figure 20A and 20B, with a counter input muxed against fixed levels at 1000 Ms/s and at 1350 Ms/s, respectively.

In Figure 20A, the ramp is muxed against a steady state mid-scale value, while in Figure 20B, the steady state input is 11111111. The apparent droop in the top level in Figure 20B is an artifact of the sampler.

Figures 19A, 19B, and 20A show the effects of blanking, while in Figure 20B, the BLANK input is held LOW, demonstrating the repetitive nature of the waveform.

Note: In Figure 20(A), A0–A7 are switched, B0–B6 are LOW, B7is HIGH and BLANK is switched. In Figure 20(B), A0–A7 are switched, B0–B7 are HIGH, and BLANK is LOW.

Figure 20(A). Muxed Ramp at 1000 Ms/s with Blanking

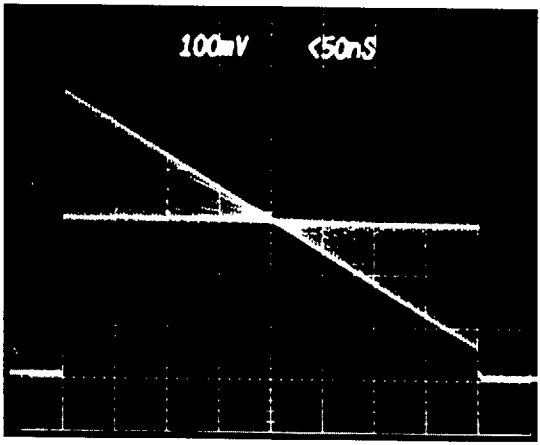


Figure 20(B). Muxed Ramp at 1350 Ms/s with Blanking Disabled

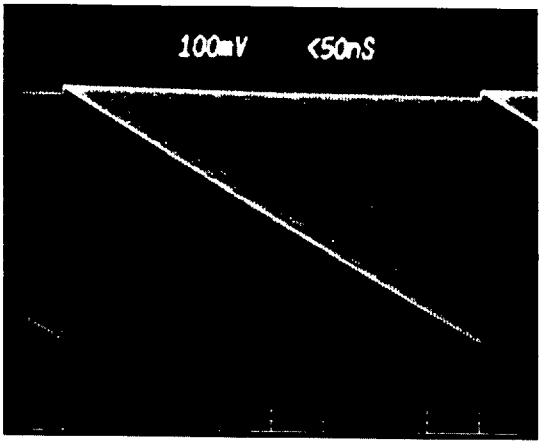


Figure 21 illustrates the symmetry of complementary full-scale transitions at V_{OUT} and $\overline{V_{OUT}}$, while Figure 22 depicts a typical worst-case glitch of 6 pV/sec.

Figure 21. Typical Full-Scale Transitions at V_{OUT} and $\overline{V_{OUT}}$ (f_{CLK} = 1000 MHz)

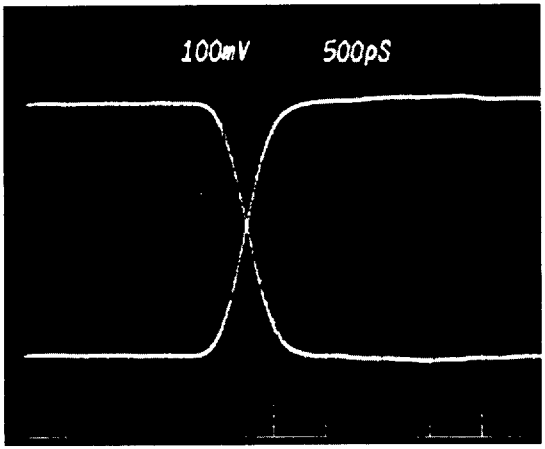


Figure 22. Typical Worst-Case Glitch Impulse (f_{CLK} = 1000 MHz)

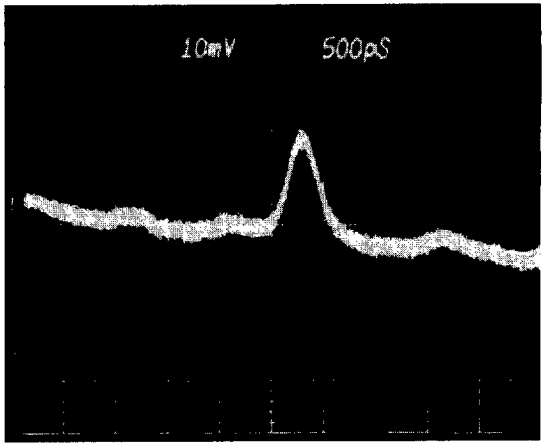


Figure 23(A). Synthesized Sine Wave Output

Figure 23(A) shows a 1 Gs/s, 58.6 MHz sine wave, and Figure 23B shows its corresponding spectrum. The spurious-free dynamic range is 46 dBc, a typical value for the device.

In Figure 23(B), the DAC output is attenuated by 6 dB going into a spectrum analyzer.

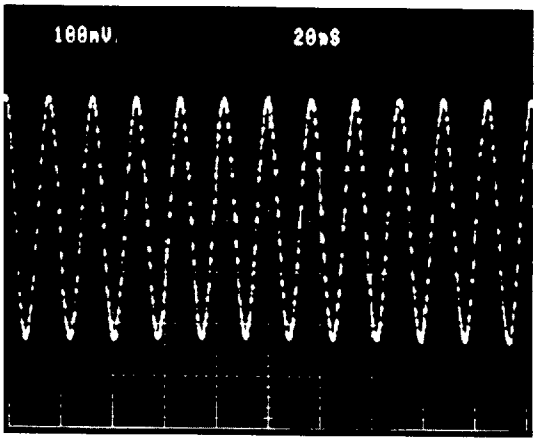


Figure 23(B). Spectrum of a 58.5 MHz Sine Wave at 1 Gs/s

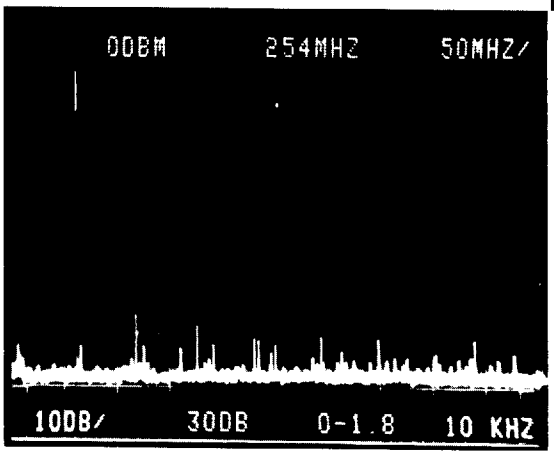


Figure 24 shows a modulated sine wave as an example of a more complex waveform.

Figure 24. Complex Modulated Sine Wave Pattern at 1000 Mb/s

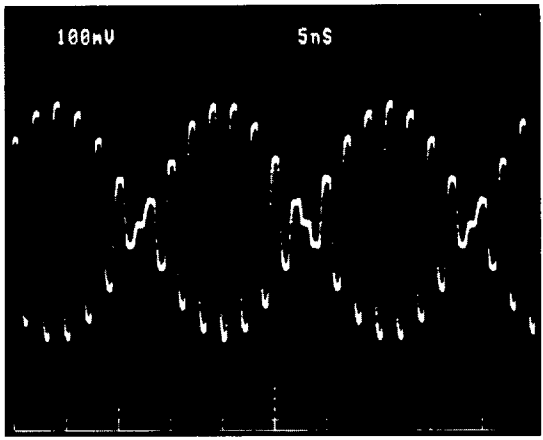
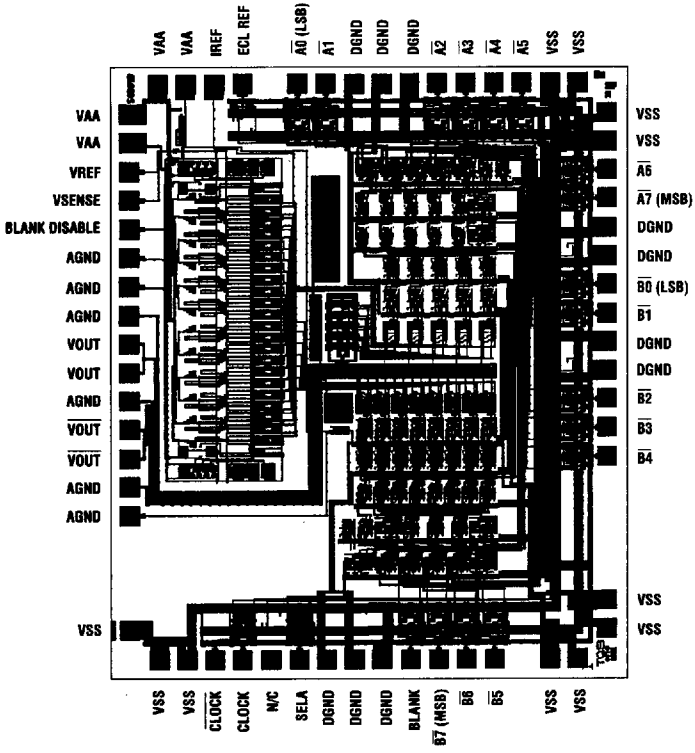


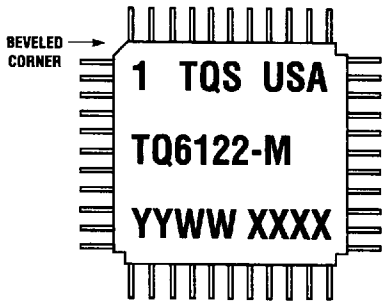
Figure 25. Chip Dimensions, Topography, and Padout



DIE SIZE: 129 Mils x 111 Mils (3110 µM x 2660 µM)

Notes: *1. Dimensional limits unless otherwise specified: ±2 mils (±51 µM).*
2. Pins labeled N/C are not connected internally.

Figure 26. Package Labelling (44-pin packaged version)
See Figures 10, 11 and 12 for package dimensions and heat-sink mounting information.



Component	*Material*
Lead	Kovar
Lead Plating	Lead/tin alloy

YYWW – Date Code

XXXX - Lot Number

Ordering Information

TQ6122-M	*8-bit, 1 Gs/s DAC in 44-pin package*
TQ6122-D	*8-bit, 1 Gs/s DAC, die only*
ETF6122	*Engineering Test Fixture with 6122 device*

MIXED SIGNAL PRODUCTS

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Revision 1.0.A October 1997