Structure	Silicon monolithic IC
Product series	Digital surround / echo processor for audio application
Type	**BU9262AFS**
Features	・Digital delay time : 9.2msec-192msec variable (8step)
	・Build-in input/output mixing amp.

◇ Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage	VCC	0.3 ~ 7.0	V
Terminal voltage	VIN	VSS -0.3 ~ VCC + 0.3	V
Storage temperature range	TSTG	-55 ~ +125	°C
Power dissipation	PD	800	mW

* In the case of exceeding Ta=25°C, 8.0mW should be redacted per 1°C.
* The radiation-resistance design is not carried out.
* Operation is not guaranteed.

◇ Operating Conditions (Ta= -10°C ~ +70°C)

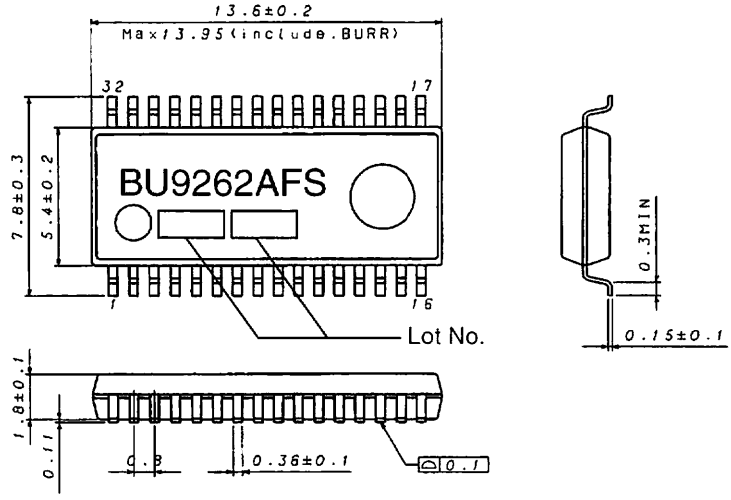
Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VCC	4.5	5.0	5.5	V
Operating frequency	fC	-	2	-	MHz

◇Electrical Characteristics

(Unless otherwise specified, Ta = 25°C、VCC = 5V、VIN = 200mVrms、fin = 1kHz、fC = 2MHz、Rg = 600Ω)

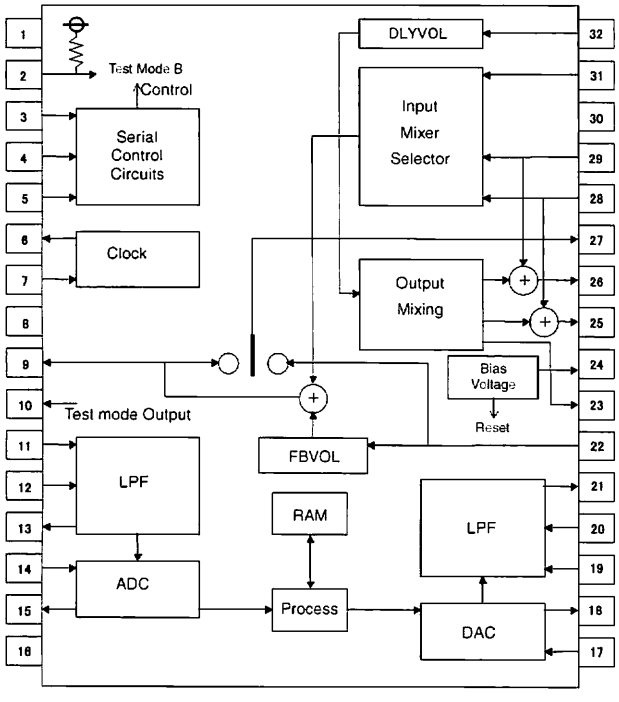
Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Circuit Current	ICC	—	20	40	mA	No signal
<Digital Delay>						
Input/Output Gain	AV1	−3	0	3	dB	
Output Distortion	THD1	—	0.6	1.2	%	tDL = ~48ms、30kHz LPF
	THD2	—	1.0	2.0	%	tDL = 96ms、30kHz LPF
	THD3	—	1.2	2.4	%	tDL = 144ms、30kHz LPF
	THD4	—	1.5	3.0	%	tDL = 192ms、30kHz LPF
Output Noise Voltage	VNO1	—	−90	−75	dBV	tDL = ~48ms、DIN−AUDIO
	VNO2	—	−87	−72	dBV	tDL = 96ms、DIN−AUDIO
	VNO3	—	−85	−70	dBV	tDL = 144ms、DIN−AUDIO
	VNO4	—	−83	−68	dBV	tDL = 192ms、DIN−AUDIO
Maximum Output Voltage	VMX1	0.7	1.0	—	Vrms	THD = 10%、30kHz LPF
<Delay Volume "DS1G" Output>						
Input/Output Gain	AV5	0	3	6	dB	DLYVOL = MAX.
Output Distortion	THD5	—	0.17	0.34	%	30kHz LPF
Output Noise Voltage	VNO5	—	−100	−90	dBV	DELAY OFF、DIN−AUDIO
Maximum Attenuation	VMX5	1.1	1.4	—	Vrms	THD = 10%、30kHz LPF
Maximum Attenuation	ATT5	—	−90	−60	dB	DLYVOL = MIN. DIN−AUDIO
<Feedback Volume>						
Input/Output Gain	AV6	−6	−3	0	dB	FBVOL = MAX.
Maximum Attenuation	ATT6	—	−90	−60	dB	FBVOL = MIN. DIN−AUDIO
<Line Amp>						
Input/Output Gain	AV7	−3	0	3	dB	
Output Distortion	THD6	—	0.01	0.03	%	30kHz LPF
Output Noise Voltage	VNO6	—	−100	−90	dBV	DELAY OFF、DIN−AUDIO
Maximum Output Voltage	VMX6	1.2	1.8	—	Vrms	THD = 10%、30kHz LPF
Channel Separation	AVCS	—	−90	−65	dB	f = 400Hz、DIN−AUDIO
Input Impedance	ZI	24	35	—	kΩ	
<Digital Section>						
Input "H" Voltage	VIH	3.8	—	—	V	
Input "L" Voltage	VIL	—	—	1.2	V	
Pull-up Resistance	Rd	12	25	50	kΩ	

◇Package Outline



SSOP-A32(Unit : mm)

◇Block Diagram



◇Terminal Function

Terminal No.	Terminal name	Function
1	NC	No Connection
2	TESTB	Test B Input Pin (normally set to "H" Input)
3	SCK	Serial Clock Input
4	SLT	Serial Latch Input
5	SI	Serial Data Input
6	CLKO	Oscillation Output Terminal
7	CLKI	Oscillation Input Terminal
8	NC	No Connection
9	DSOUT	Delay Source Output
10	TESTOUT	Test Output Pin (normally set to "L" Input)
11	LPF1I1	LPF External Capacitor terminal
12	LPF1I2	
13	LPF1O	
14	ADI	ADC Capacitor Connection Terminal
15	ADO	
16	GND	Ground Terminal
17	DAI	DAC Capacitor Connection Terminal
18	DAO	
19	LPF2I1	LPF External Capacitor terminal
20	LPF2I2	
21	LPF2O	
22	VOIN	Delayed Signal Volume Input
23	DSIG	Delayed Signal Output
24	VREF	Analog Bias Voltage
25	RCOUT	Rch Output
26	LCOUT	Lch Output
27	FBOUT	Power Supply Terminal
28	RCIN	Rch Input
29	LCIN	Lch Input
30	VCC	Power Supply Terminal
31	MICIN	Mic In (Connect with Mic Amp Output)
32	MIXIN	Mix Signal Input

◇ Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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As of 18th. April 2005