



6 Channel EMI Filter Array with ESD Protection

Features

- Six channels of EMI filtering for data ports
- Pi-style EMI filters in a capacitor-resistor-capacitor (C-R-C) network
- 40dB absolute attenuation (typical) at 1 GHz
- 35dB attenuation (typical) at 1 GHz relative to pass band
- $\pm 15\text{kV}$ ESD protection on each channel (IEC 61000-4-2 Level 4, contact discharge)
- $\pm 30\text{kV}$ ESD protection on each channel (HBM)
- 15-bump, 2.960mm X 1.330mm footprint Chip Scale Package (CSP)
- Chip Scale Package features extremely low lead inductance for optimum filter and ESD performance

Applications

- EMI filtering and ESD protection for both data and I/O ports
- Wireless Handsets
- Handheld PCs / PDAs
- MP3 Players
- Notebooks
- Desktop PCs

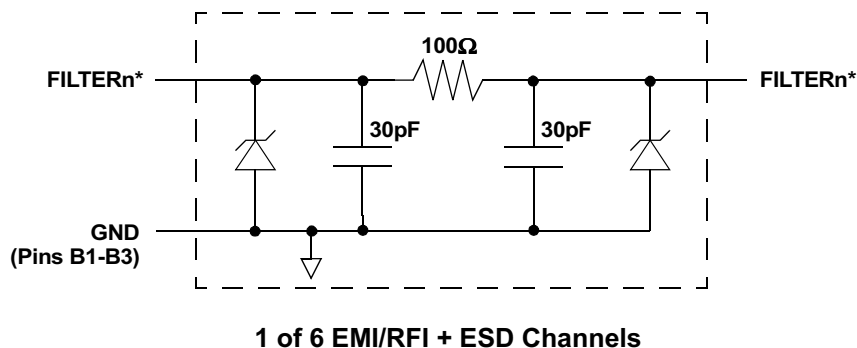
Product Description

The CSPEMI306A is a six channel low-pass filter array that reduces EMI/RFI emissions while at the same time providing ESD protection. It is used on data ports on mobile devices. To reduce EMI/RFI emissions, the CSPEMI306A integrates a pi-style filter (C-R-C) for each of the 6 channels. Each high quality filter provides greater than 30dB attenuation in the 800-2700 MHz range relative to the pass band attenuation. These pi-style filters also support bidirectional filtering, controlling EMI both to and from a data port connector.

In addition, the CSPEMI306A provides a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge (ESD). The input pins are designed and characterized to safely dissipate ESD strikes of 15kV, exceeding the maximum requirement of the IEC 61000-4-2 international standard. Using the MIL-STD-883 (Method 3015) specification for Human Body Model (HBM) ESD, the device provides protection for contact discharges to greater than 30kV.

The CSPEMI306A is particularly well suited for portable electronics (e.g., cellular telephones, PDAs, notebook computers) because of its small package footprint and low weight. This device is available in a space-saving, low-profile Chip Scale Package, and is fabricated with California Micro Devices' semiconductor processes for reliability equalling today's IC devices.

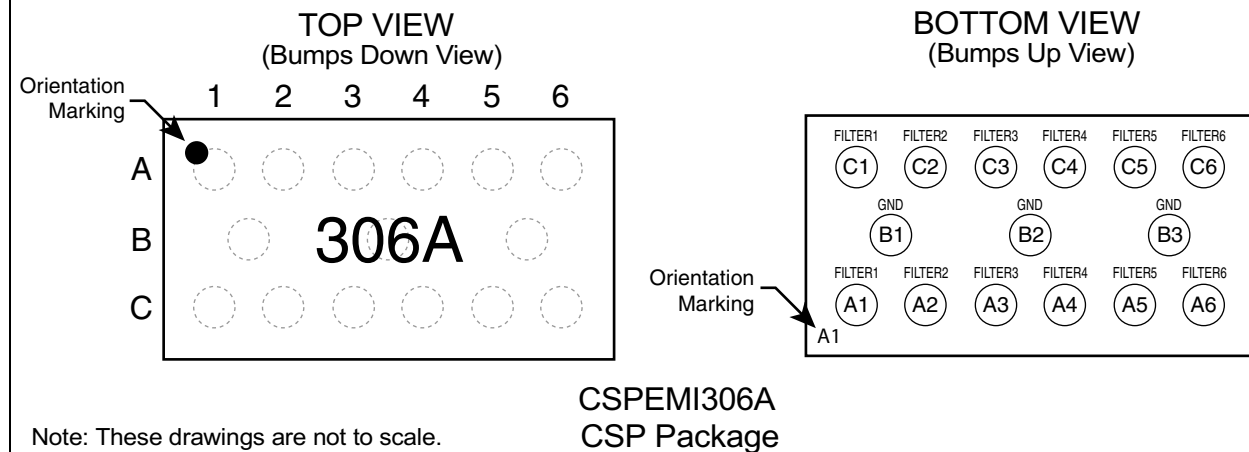
Electrical Schematic



* See Package/Pinout Diagram for expanded pin information.



PACKAGE / PINOUT DIAGRAMS



PIN DESCRIPTIONS

PIN(s)	NAME	DESCRIPTION
A1	FILTER1	Filter Channel 1
A2	FILTER2	Filter Channel 2
A3	FILTER3	Filter Channel 3
A4	FILTER4	Filter Channel 4
A5	FILTER5	Filter Channel 5
A6	FILTER6	Filter Channel 6
B1-B3	GND	Device Ground
C1	FILTER1	Filter Channel 1
C2	FILTER2	Filter Channel 2
C3	FILTER3	Filter Channel 3
C4	FILTER4	Filter Channel 4
C5	FILTER5	Filter Channel 5
C6	FILTER6	Filter Channel 6

Ordering Information

PART NUMBERING INFORMATION

Pins	Package	Ordering Part Number ¹	Part Marking
15	CSP	CSPEMI306A	306A

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Storage Temperature Range	-65 to +150	°C
DC Power per Resistor	100	mW
DC Package Power Rating	600	mW

STANDARD OPERATING CONDITIONS

PARAMETER	RATING	UNITS
Operating Temperature Range	-40 to +85	°C

ELECTRICAL OPERATING CHARACTERISTICS¹

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
R	Resistance		80	100	120	Ω
C	Capacitance	At 2.5V DC	24	30	36	pF
TCR	Temperature Coefficient of Resistance			1200		ppm/°C
TCC	Temperature Coefficient of Capacitance	At 2.5V DC		-300		ppm/°C
V _{DIODE}	Diode Voltage (reverse bias)	I _{DIODE} =10μA	5.5			V
I _{LEAK}	Diode Leakage Current (reverse bias)	V _{DIODE} =3.3V			100	nA
V _{SIG}	Signal Voltage Positive Clamp Negative Clamp	I _{LOAD} = 10mA	5.6 -0.4	6.8 -0.8	9.0 -1.5	V V
V _{ESD}	In-system ESD Withstand Voltage a) Human Body Model, MIL-STD-883, Method 3015 b) Contact Discharge per IEC 61000-4-2 Level 4	Notes 2,4 and 5	±30 ±15			kV kV
V _{CL}	Clamping Voltage during ESD Discharge MIL-STD-883 (Method 3015), 8kV Positive Transients Negative Transients	Notes 2,3,4 and 5		+10 -5		V V

Note 1: T_A=25°C unless otherwise specified.

Note 2: ESD applied to input and output pins with respect to GND, one at a time.

Note 3: Clamping voltage is measured at the opposite side of the EMI filter to the ESD pin. For example, if ESD is applied to Pin A1, then clamping voltage is measured at Pin C1.

Note 4: Unused pins are left open

Note 5: These parameters are guaranteed by design and characterization.



Performance Information

Typical Filter Performance ($T_A=25^\circ\text{C}$, DC Bias=0V, 50 Ohm Environment)

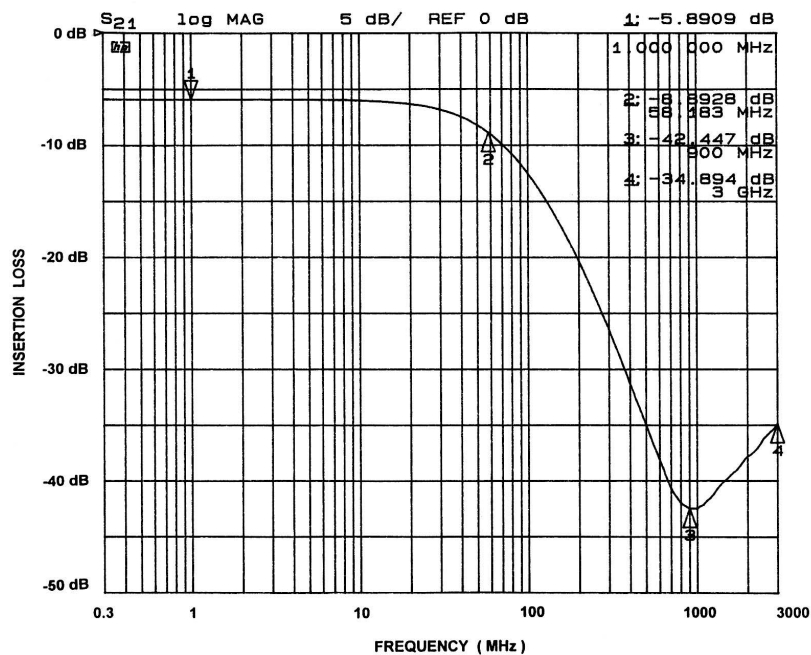


Figure 1. Insertion Loss VS. Frequency (A1-C1 to GND B2)

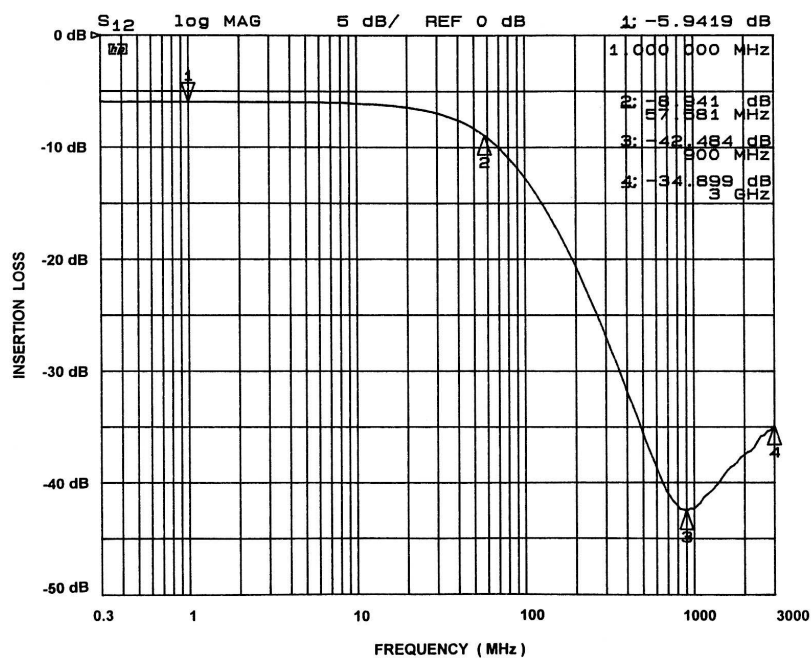


Figure 2. Insertion Loss VS. Frequency (A2-C2 to GND B2)



Performance Information (cont'd)

Typical Filter Performance ($T_A=25^\circ\text{C}$, DC Bias=0V, 50 Ohm Environment)

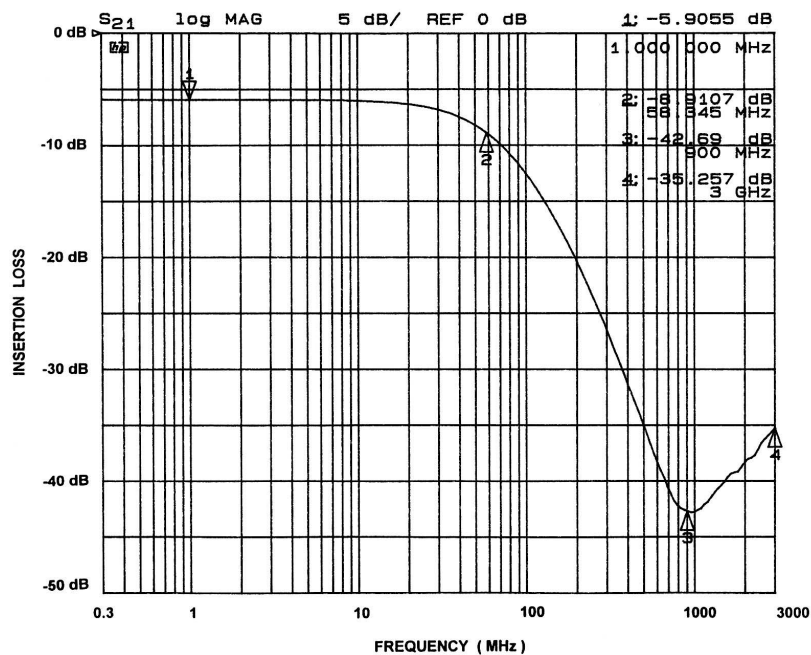


Figure 3. Insertion Loss VS. Frequency (A3-C3 to GND B2)

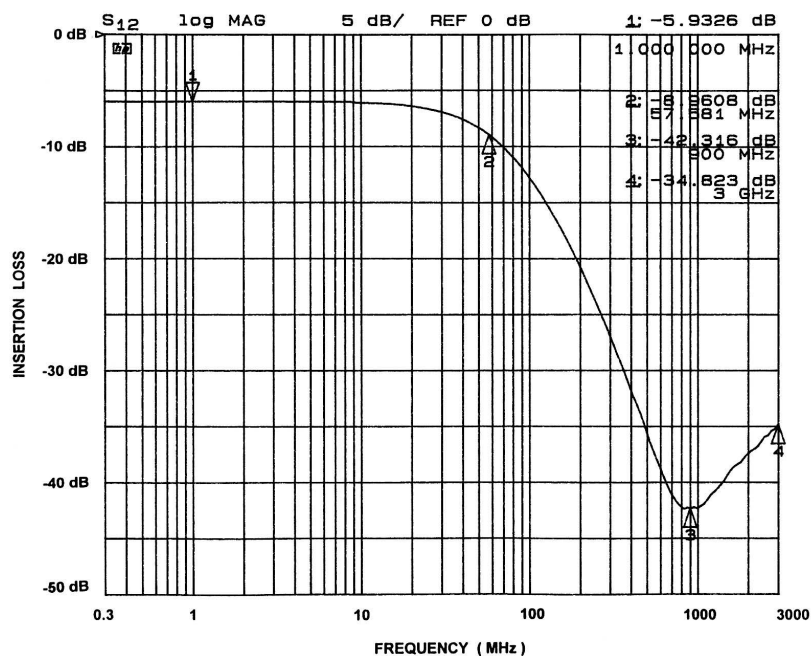


Figure 4. Insertion Loss VS. Frequency (A4-C4 to GND B2)



Performance Information (cont'd)

Typical Filter Performance ($T_A=25^\circ\text{C}$, DC Bias=0V, 50 Ohm Environment)

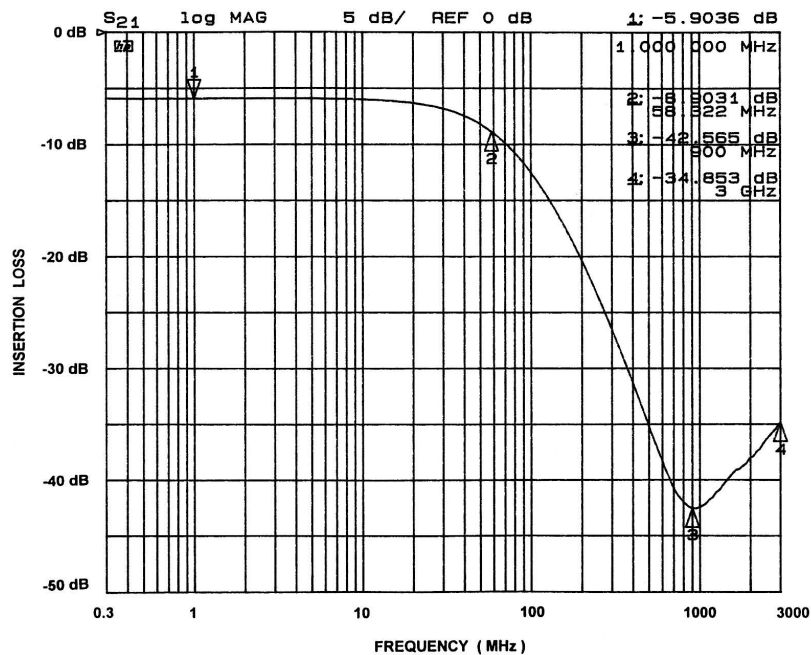


Figure 5. Insertion Loss VS. Frequency (A5-C5 to GND B2)

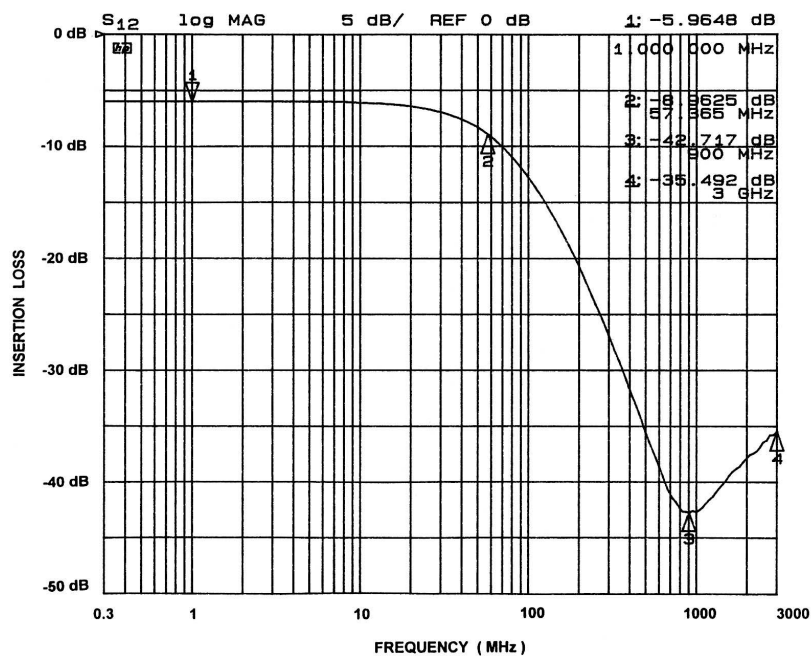


Figure 6. Insertion Loss VS. Frequency (A6-C6 to GND B2)



Performance Information (cont'd)

Typical Filter Performance ($T_A=25^\circ\text{C}$, DC Bias=0V, 50 Ohm Environment)

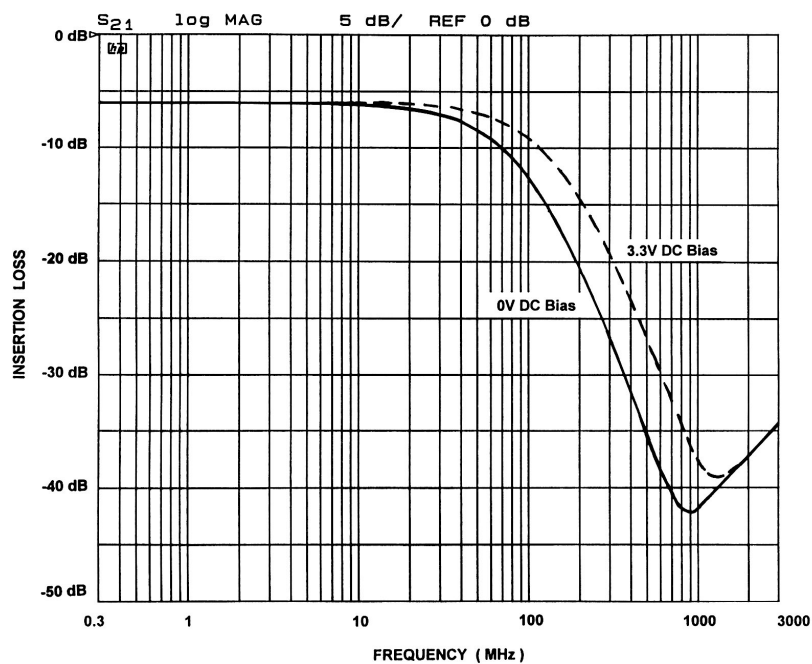


Figure 7. Comparison of Filter Response Curves for CSPEMI306A VS. DC Bias



Performance Information (cont'd)

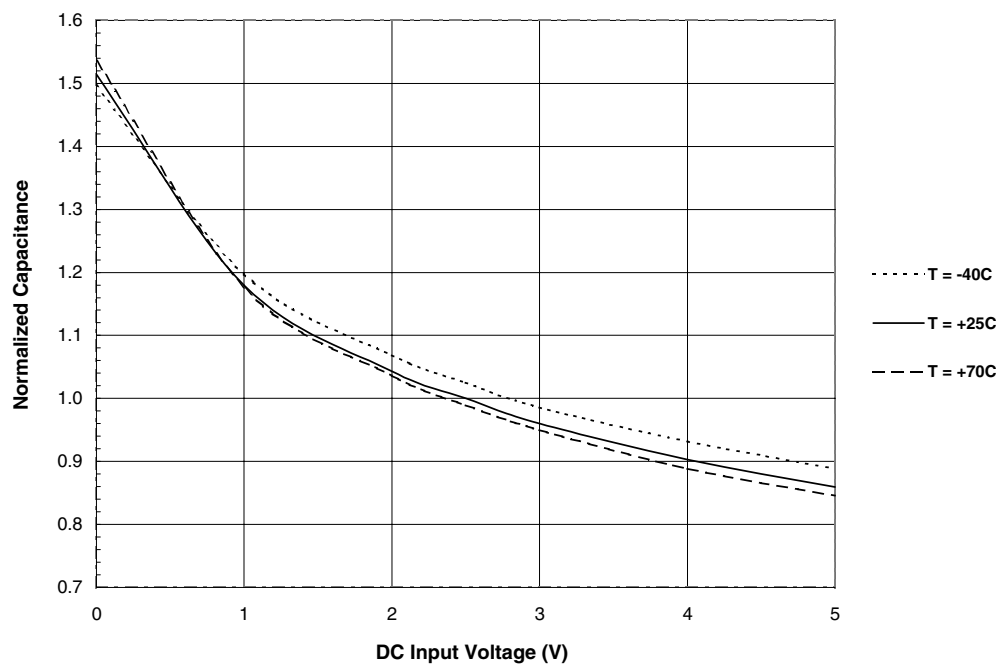


Figure 8. Filter Capacitance vs. Input Voltage over Temperature
(normalized to capacitance at 2.5VDC and 25°C)

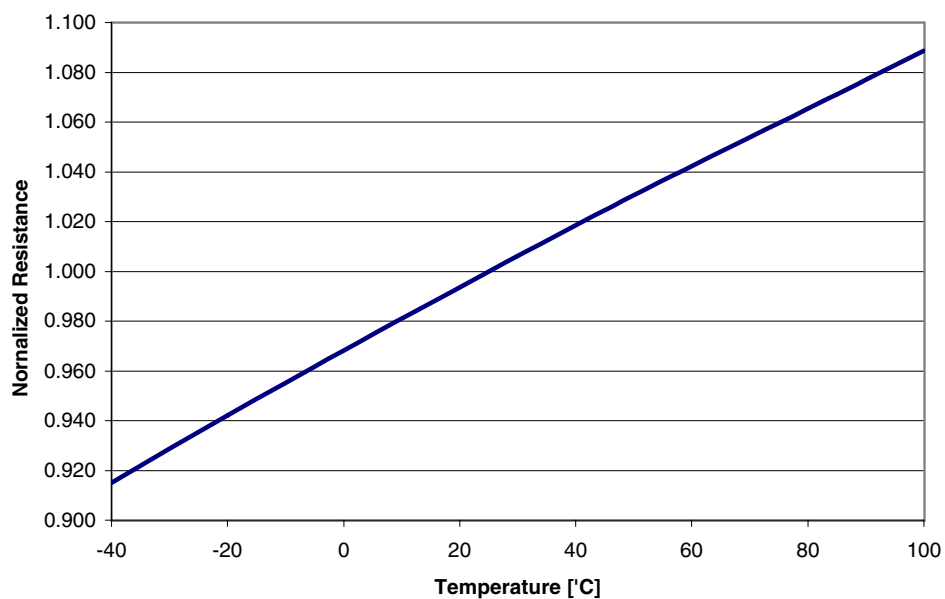


Figure 9. Resistance vs. Temperature
(normalized to resistance at 25°C)

Application Information

Refer to Application Note AP-217, "The Chip Scale Package", for a detailed description of Chip Scale Packages offered by California Micro Devices.

PRINTED CIRCUIT BOARD RECOMMENDATIONS

PARAMETER	VALUE
Pad Size on PCB	0.275mm
Pad Shape	Round
Pad Definition	Non-Solder Mask defined pads
Solder Mask Opening	0.325mm Round
Solder Stencil Thickness	0.150mm
Solder Stencil Aperture Opening (laser cut, 5% tapered walls)	0.330mm Round
Solder Flux Ratio	50/50 by volume
Solder Paste Type	No Clean
Pad Protective Finish	OSP (Entek Cu Plus 106A)
Tolerance — Edge To Corner Ball	$\pm 50\mu\text{m}$
Solder Ball Side Coplanarity	$\pm 20\mu\text{m}$
Maximum Dwell Time Above Liquidous (183°C)	60 seconds
Soldering Maximum Temperature	240°C

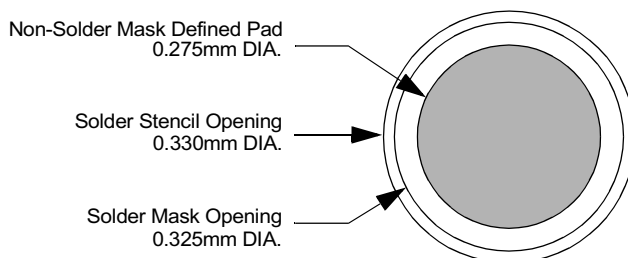


Figure 10. Recommended Non-Solder Mask Defined Pad Illustration

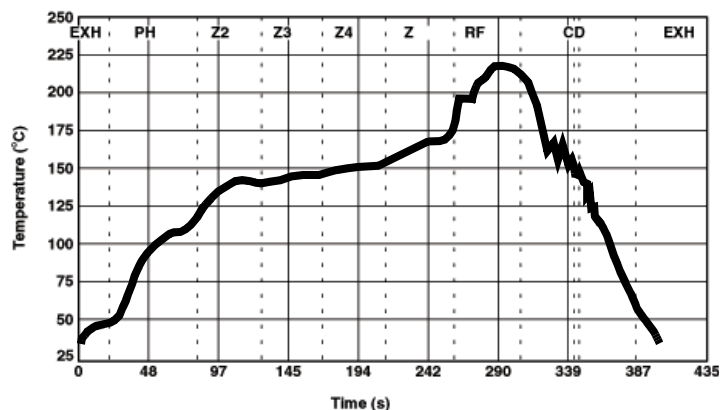


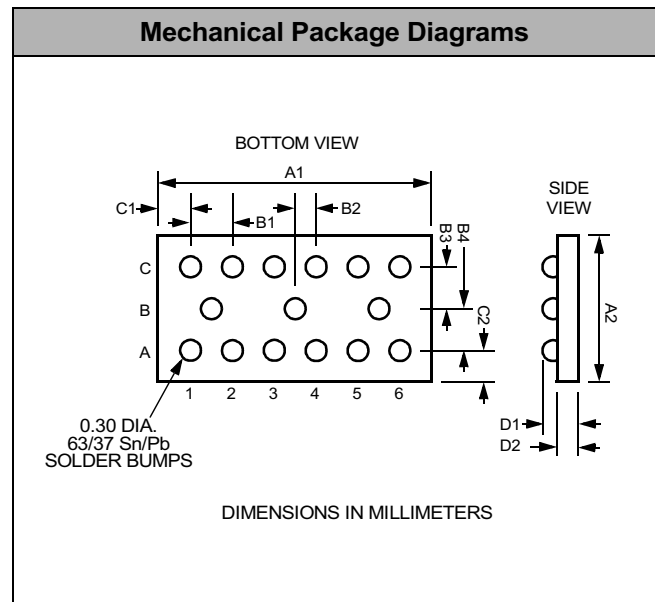
Figure 11. Solder Reflow Profile

Mechanical Details

CSP Mechanical Specifications

CSPEMI306A devices are packaged in a custom Chip Scale Package (CSP). Dimensions are presented below. For complete information on CSP packaging, see the California Micro Devices CSP Package Information document.

PACKAGE DIMENSIONS						
Package		Custom CSP				
Bumps		15				
Dim	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A1	2.915	2.960	3.005	0.1148	0.1165	0.1183
A2	1.285	1.330	1.375	0.0506	0.0524	0.0541
B1	0.495	0.500	0.505	0.0195	0.0197	0.0199
B2	0.245	0.250	0.255	0.0096	0.0098	0.0100
B3	0.430	0.435	0.440	0.0169	0.0171	0.0173
B4	0.430	0.435	0.440	0.0169	0.0171	0.0173
C1	0.180	0.230	0.280	0.0071	0.0091	0.0110
C2	0.180	0.230	0.280	0.0071	0.0091	0.0110
D1	0.561	0.605	0.649	0.0221	0.0238	0.0255
D2	0.355	0.380	0.405	0.0140	0.0150	0.0159
# per tape and reel		3500 pieces				
Controlling dimension: millimeters						



**Package Dimensions for
CSPEMI306A Chip Scale Package**

CSP Tape and Reel Specifications

PART NUMBER	CHIP SIZE (mm)	POCKET SIZE (mm) $B_0 \times A_0 \times K_0$	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P_0	P_1
CSPEMI306A	2.96 X 1.33 X 0.6	3.18 X 1.52 X 0.76	8mm	178mm (7")	3500	4mm	4mm

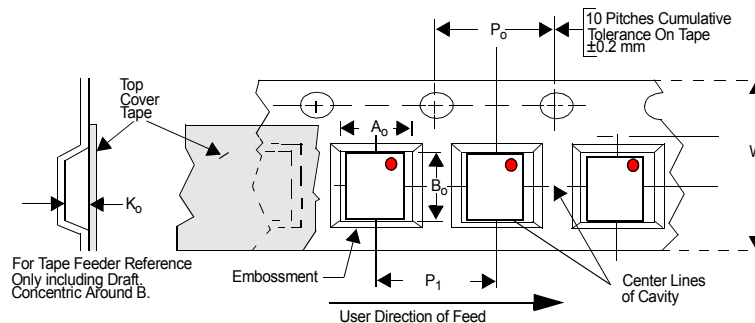


Figure 12. Tape and Reel Mechanical Data