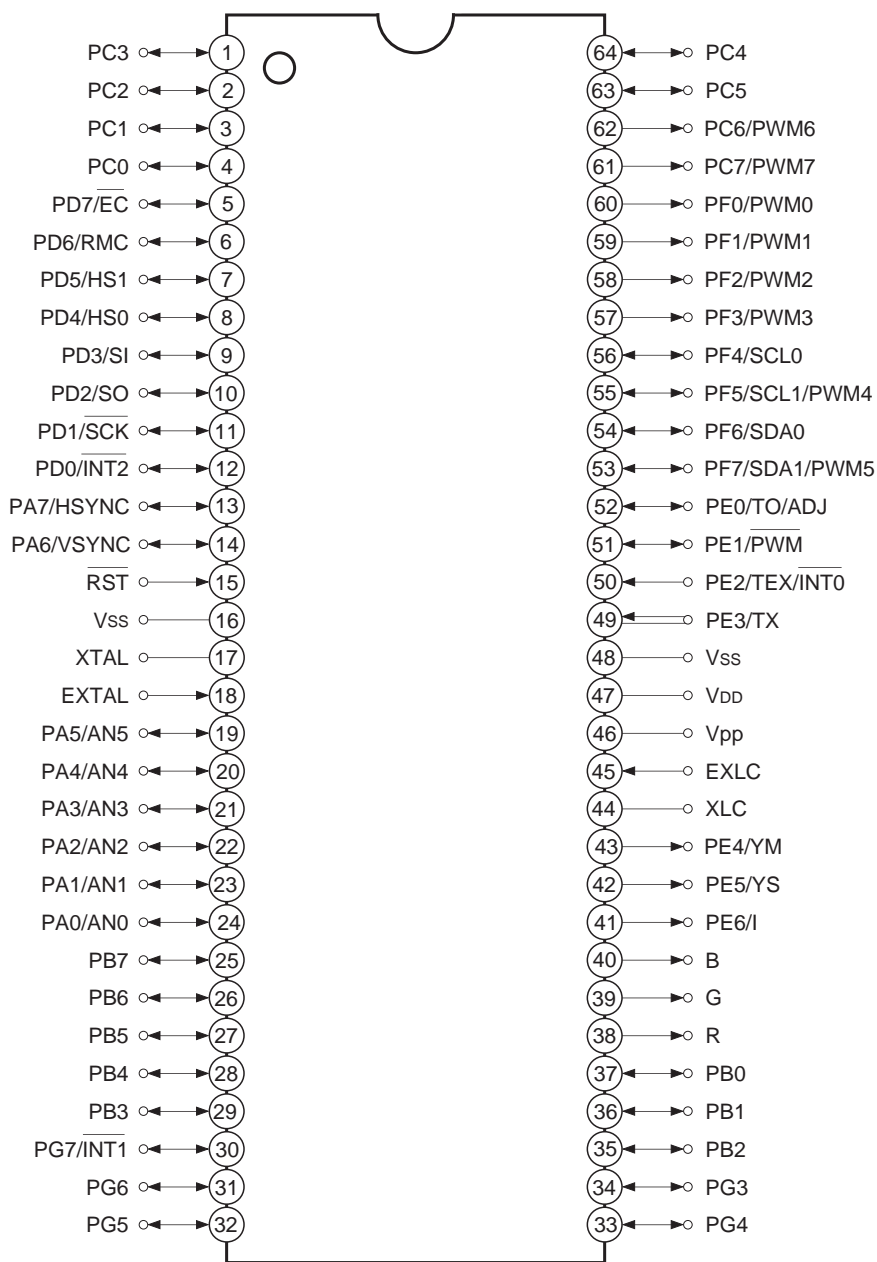


\* Not incorporated for 52-pin package.  
 Parentheses indicate configurations for 52-pin package.

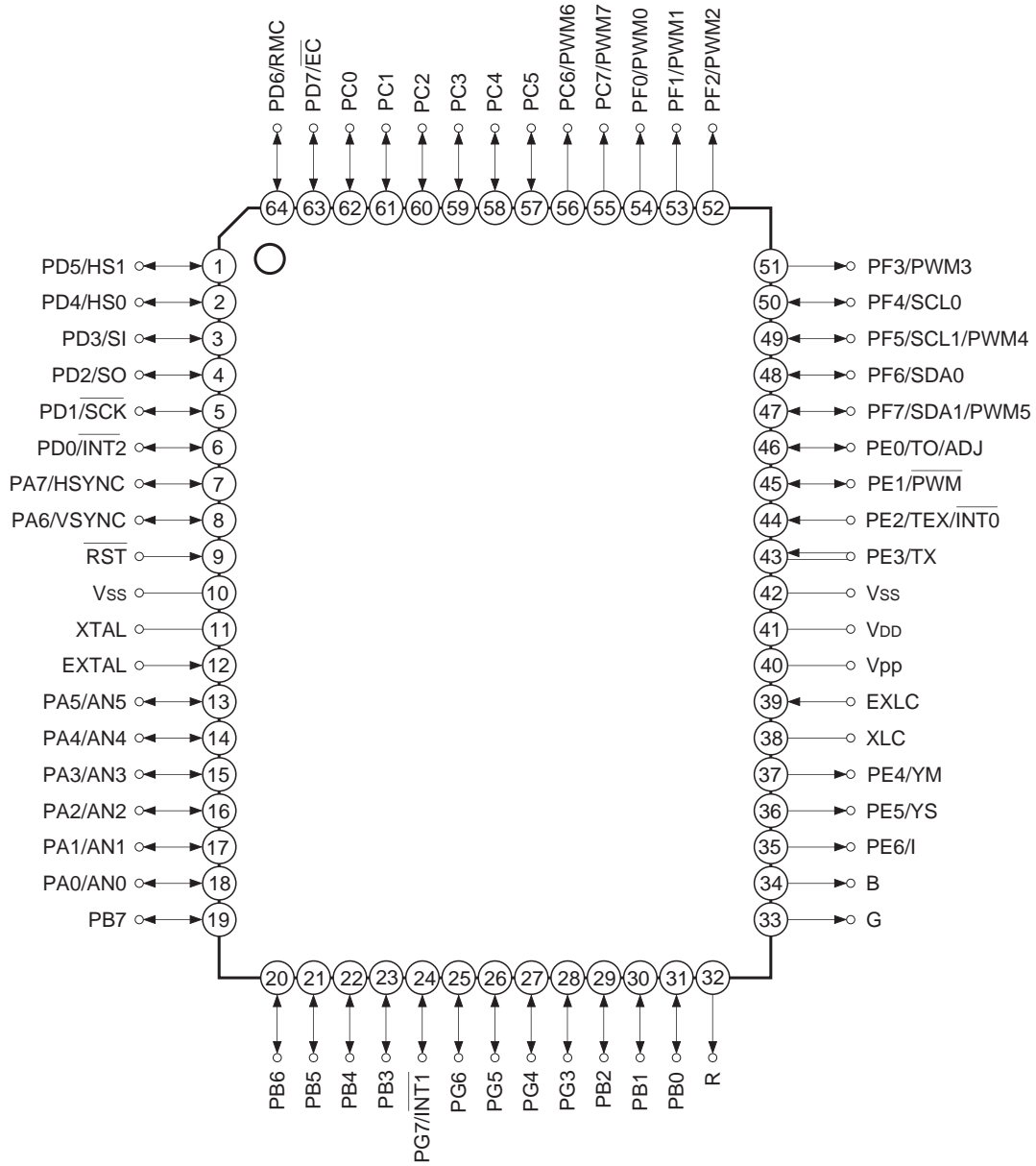
Pin Assignment (Top View) 64-pin SDIP



**Note)**

1. Vpp (Pin 46) is left open.
2. Vss (Pins 16 and 48) are both connected to GND.

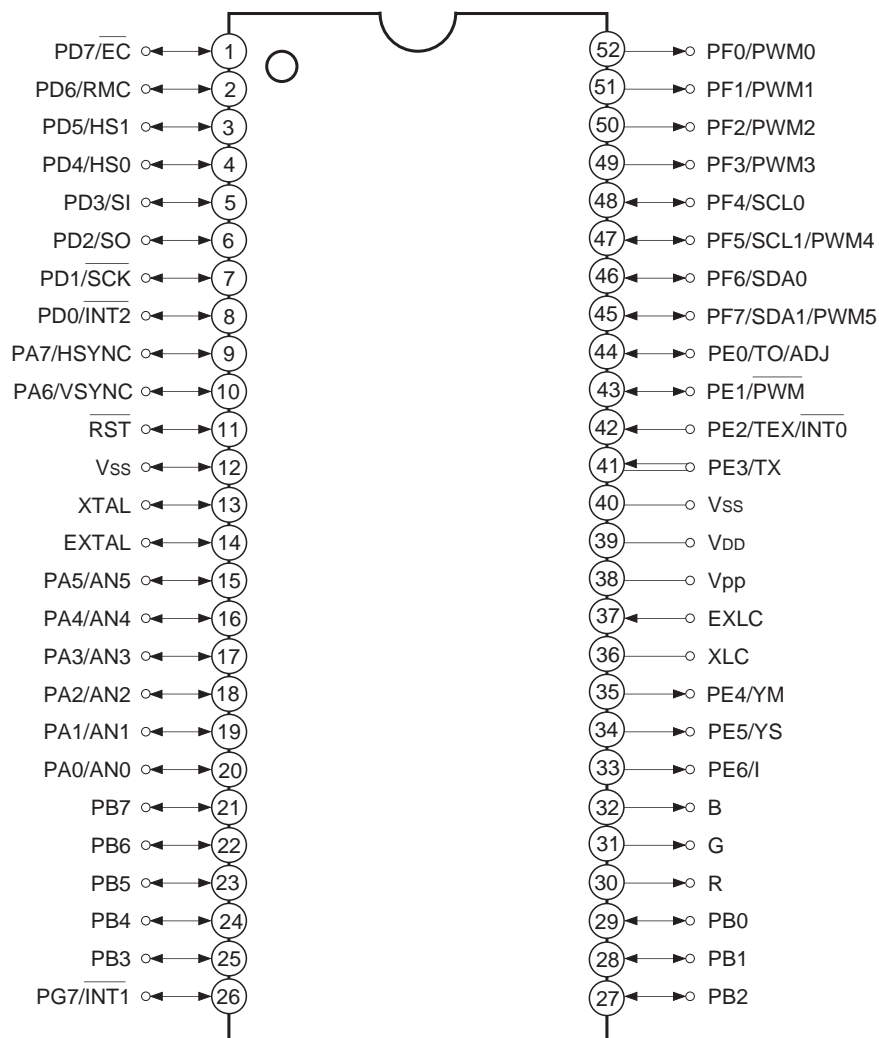
Pin Assignment (Top View) 64-pin QFP



**Note)**

1. Vpp (Pin 40) is left open.
2. Vss (Pins 10 and 42) are both connected to GND.

Pin Assignment (Top View) 52-pin SDIP



**Note)**

1. Vpp (Pin 38) is left open.
2. Vss (Pins 12 and 40) are both connected to GND.

Pin Description

Symbol	I/O	Description		
PA0/AN0 to PA5/AN5	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Analog inputs to A/D converter. (6 pins)	
PA6/VSYNC	I/O/Input		OSD display vertical sync signal input.	
PA7/HSYNC	I/O/Input		OSD display horizontal sync signal input.	
PB0 to PB7	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)		
PC0 to PC5*	I/O	(Port C) Lower 6 bits are I/O ports; I/O can be set in a unit of single bits. Upper 2 bits are output port and large current (12mA) N-channel open drain output. Upper 2 bits are medium drive voltage (12V); lower 6 bits are 5V drive. (8 pins)		
PC6/PWM6* to PC7/PWM7*	Output/Output		8-bit PWM output. (2 pins)	
PD0/ $\overline{\text{INT2}}$	I/O/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sink current. (8 pins)	External interruption request input. Active at the falling edge.	
PD1/ $\overline{\text{SCK}}$	I/O/I/O		Serial clock I/O.	
PD2/SO	I/O/Output		Serial data output.	
PD3/SI	I/O/Input		Serial data input.	
PD4/HS0	I/O/Input		HSYNC counter (CH0) input.	
PD5/HS1	I/O/Input		HSYNC counter (CH1) input.	
PD6/RMC	I/O/Input		Remote control reception circuit input.	
PD7/ $\overline{\text{EC}}$	I/O/Input		External event input for timer/counter.	
PE0/TO/ADJ	I/O/Output/ Output			Rectangular wave output for 8-bit timer/counter.   TEX oscillation frequency dividing output.
PE1/ $\overline{\text{PWM}}$	I/O/Output		14-bit PWM output.	
PE2/TEX/ $\overline{\text{INT0}}$	Input/Input/ Input	(Port E) Bits 0 and 1 are I/O port; I/O can be set in a unit of single bits. Bits 2 and 3 are input port. Bits 4, 5 and 6 are output port. (7 pins)	Connects a crystal for 32kHz timer/counter clock oscillation. When used as an event counter, input to TEX pin and leave TX pin open.   External interruption request input. Active at the falling edge.	
PE3/TX	Input			
PE4/YM	Output/Output			
PE5/YS	Output/Output			
PE6/I	Output/Output			
B	Output			OSD display 6-bit output. (6 pins)
G	Output			
R	Output			

\* Not incorporated for 52-pin package.

Symbol	I/O	Description	
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port and large current (12mA) N-channel open drain output. Lower 4 bits are medium drive voltage (12V); upper 4 bits are 5V drive. (8 pins)	8-bit PWM output. (4 pins)
PF4/SCL0	Output/I/O		I <sup>2</sup> C bus interface transfer clock I/O. (2 pins)
PF5/SCL1/PWM4	Output/I/O/Output		
PF6/SDA0	Output/I/O		I <sup>2</sup> C bus interface transfer data I/O. (2 pins)
PF7/SDA1/PWM5	Output/I/O/Output		
PG3 to PG6*	I/O	(Port G) 5-bit I/O port. I/O can be set in a unit of single bits. (5 pins)	
PG7/ $\overline{\text{INT1}}$	I/O/Input	External interruption request input. Active at the falling edge.	
EXTAL	Input	Connects a crystal for system clock oscillation. When a clock is supplied externally, input to EXTAL pin and input a reversed phase clock to XTAL pin.	
XTAL			
$\overline{\text{RST}}$	Input	System reset; active at Low level.	
EXLC	Input	OSD display clock oscillation I/O. Oscillation frequency is determined by the external L and C.	
XLC			
V <sub>pp</sub>		Positive power supply for incorporated PROM writing. Leave this pin open during normal operation.	
V <sub>DD</sub>		Positive power supply.	
V <sub>SS</sub>		GND. Connect two V <sub>SS</sub> pins to GND.	

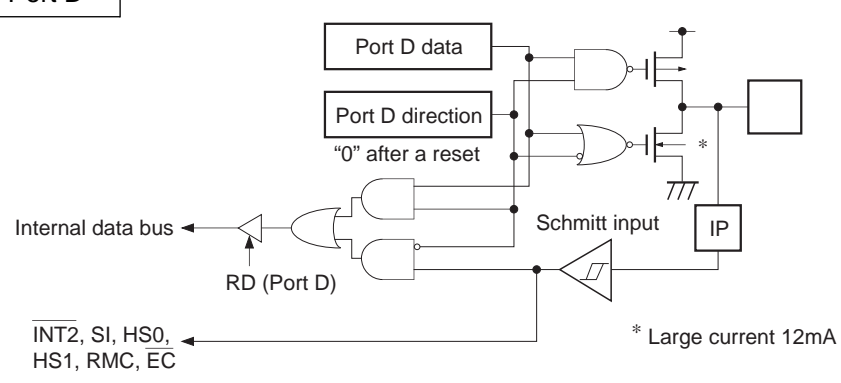
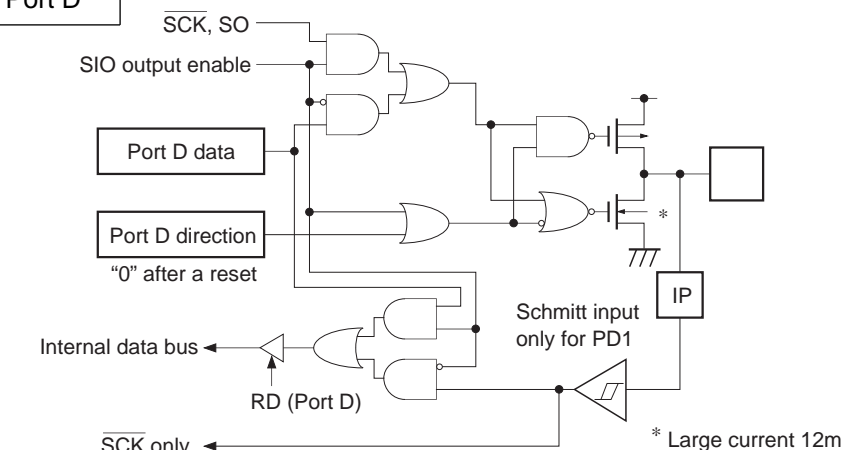
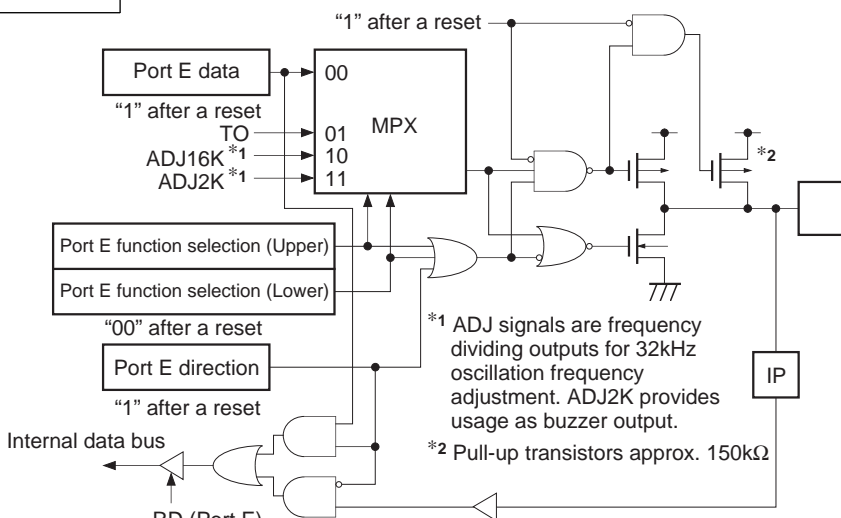
\* Not incorporated for 52-pin package.

Input/Output Circuit Formats for Pins

Pin	Circuit format	After a reset
<p>PA0/AN0 to PA5/AN5</p> <p>6 pins</p>	<p>Port A</p>	<p>Hi-Z</p>
<p>PA6/VSYNC PA7/HSYNC</p> <p>2 pins</p>	<p>Port A</p>	<p>Hi-Z</p>
<p>PB0 to PB7 PC0 to PC5* PG3 to PG6* PG7/INT1</p> <p>19 pins</p>	<p>Port B Port C Port G</p>	<p>Hi-Z</p>
<p>PC6/PWM6* PC7/PWM7* PF0/PWM0 to PF3/PWM3</p> <p>6 pins</p>	<p>Port C Port F</p> <p>* 12V drive voltage Large current 12mA</p>	<p>Hi-Z</p>

\* Not incorporated for 52-pin package.



Pin	Circuit format	After a reset
<p>PD0/<math>\overline{\text{INT2}}</math>                      PD3/<math>\overline{\text{SI}}</math>                      PD4/<math>\overline{\text{HS0}}</math>                      PD5/<math>\overline{\text{HS1}}</math>                      PD6/<math>\overline{\text{RMC}}</math>                      PD7/<math>\overline{\text{EC}}</math></p> <p>6 pins</p>	<p>Port D</p>  <p>Internal data bus ← RD (Port D)</p> <p><math>\overline{\text{INT2}}</math>, <math>\overline{\text{SI}}</math>, <math>\overline{\text{HS0}}</math>, <math>\overline{\text{HS1}}</math>, <math>\overline{\text{RMC}}</math>, <math>\overline{\text{EC}}</math></p> <p>* Large current 12mA</p>	<p>Hi-Z</p>
<p>PD1/<math>\overline{\text{SCK}}</math>                      PD2/<math>\overline{\text{SO}}</math></p> <p>2 pins</p>	<p>Port D</p>  <p>Internal data bus ← RD (Port D)</p> <p><math>\overline{\text{SCK}}</math> only</p> <p>* Large current 12mA</p>	<p>Hi-Z</p>
<p>PE0/<math>\overline{\text{TO}}</math>/<math>\overline{\text{ADJ}}</math></p> <p>1 pin</p>	<p>Port E</p>  <p>Internal data bus ← RD (Port E)</p> <p>*1 ADJ signals are frequency dividing outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.</p> <p>*2 Pull-up transistors approx. 150k<math>\Omega</math></p>	<p>High level                      (H level at ON                      resistance of                      pull-up                      transistor                      during a reset)</p>

Pin	Circuit format	After a reset
<p>PE1/PWM</p> <p>1 pin</p>	<p>Port E</p> <p>Internal data bus</p> <p>RD (Port E)</p> <p>IP</p>	<p>High level</p>
<p>PE2/TEX/INT0 PE3/TX</p> <p>2 pins</p>	<p>Port E</p> <p>TEX oscillation circuit control</p> <p>“1” after a reset Schmitt input</p> <p>INT0</p> <p>Intrnal data bus</p> <p>RD (Port E)</p> <p>PE2/ TEX/ INT0</p> <p>IP</p> <p>PE3/ TX</p> <p>Schmitt input</p> <p>Clock input</p> <p>RD (Port E)</p>	<p>Oscillation stop Port input</p>
<p>PE4/YM PE5/YS PE6/I</p> <p>3 pins</p>	<p>Port E</p> <p>YM, YS, I</p> <p>Output polarity</p> <p>“0” after a reset</p> <p>Port E function selection</p> <p>“1” after a reset</p> <p>Port E data</p> <p>Internal data bus</p> <p>RD (Port E)</p> <p>IP</p> <p>Writing data to output polarity register or port data register brings output to activate.</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PF4/SCL0 PF5/SCL1/PWM4 PF6/SDA0 PF7/SDA1/PWM5</p> <p>4 pins</p>	<p>Port F</p> <p>SCL, SDA</p> <p>I<sup>2</sup>C bus enable</p> <p>PWM4, PWM5</p> <p>Port F function selection "0" after a reset</p> <p>Port F data "1" after a reset</p> <p>Internal data bus</p> <p>RD (Port F) Schmitt input</p> <p>SCL, SDA (I<sup>2</sup>C bus circuit)</p> <p>* Large current 12mA</p> <p>BUS SW To internal I<sup>2</sup>C pins (SCL1 for SCL0)</p>	<p>Hi-Z</p>
<p>R G B</p> <p>3 pins</p>	<p>R, G, B</p> <p>Output polarity "0" after a reset</p> <p>Writing data to output polarity register brings output to activate.</p>	<p>Hi-Z</p>
<p>EXLC XLC</p> <p>2 pins</p>	<p>Oscillation control</p> <p>EXLC</p> <p>XLC</p> <p>OSD display clock</p>	<p>Oscillation stop</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	<p>EXTAL</p> <p>XTAL</p> <ul style="list-style-type: none"> <li>• Diagram shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed and XTAL is driven at "H" level during stop. (This device does not enter the stop mode.)</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>	<p>Pull-up resistor</p> <p>Schmitt input</p>	<p>Low level (during a reset)</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	V <sub>pp</sub>	-0.3 to +13.0	V	Incorporated PROM
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Medium drive output voltage	V <sub>OUTP</sub>	-0.3 to +15.0	V	
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	∑I <sub>OH</sub>	-50	mA	Total of all output pins
Low level output current	I <sub>OL</sub>	15	mA	Pins excluding large current output (value per pin)
	I <sub>OLC</sub>	20	mA	Large current output pins* <sup>2</sup> (value per pin)
Low level total output current	∑I <sub>OL</sub>	130	mA	Total of all output pins
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	1000	mW	SDIP-64P-01
		600	mW	QFP-64P-L01
		875	mW	SDIP-52P-01

\*<sup>1</sup> V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*<sup>2</sup> The large current drive transistor is Port C (PC6, PC7), Port D (PD) and Port F (PF).

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing modes
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing mode or sleep
		2.7	5.5	V	Guaranteed operation range for TEX mode
		—	—	V	Guaranteed data hold range for stop <sup>*5</sup>
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*1
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	*2
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin <sup>*3</sup> , TEX pin <sup>*4</sup>
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*1
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	*2
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin <sup>*3</sup> , TEX pin <sup>*4</sup>
Operating temperature	T <sub>opr</sub>	-20	+75	°C	

\*1 PA0 to PA5, PB3 to PB7, PC0 to PC5, PD2, PE0, PE1, PE3, PG3 to PG6, SCL0, SCL1, SDA0, SDA1 pins

\*2 VSYNC, HSYNC, INT2, SCK, SI, HS0, HS1, RMC, EC, INT0, INT1, RST, PB0 to PB2 pins

\*3 Specifies only during external clock input.

\*4 Specifies only during external event count input.

\*5 This device does not enter the stop mode.

**Electrical Characteristics**

**DC characteristics**

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA, PB, PC0 to PC5, PD, PE0 to PE1, PE4 to PE6, PG, R, G, B	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output voltage	VOL	PA to PD, PE0 to PE1, PE4 to PE6, PF0 to PF3, PG, R, G, B	VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
		PC6, PC7, PD, PF PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	VDD = 4.5V, IOL = 12.0mA			1.5	V
			VDD = 4.5V, IOL = 3.0mA			0.4	V
			VDD = 4.5V, IOL = 4.0mA			0.6	V
Input current	IiHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
	IiLE		VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IiHT	TEX	VDD = 5.5V, VIH = 5.5V	0.1		10	μA
	IiLT		VDD = 5.5V, VIL = 0.4V	-0.1		-10	μA
	IiLR	RST*1	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA
I/O leakage current	IIZ	PA, PB, PC0 to PC5, PD, PE, PG, R, G, B, RST*1	VDD = 5.5V, VI = 0, 5.5V			±10	μA
Open drain I/O leakage current (in N-ch Tr off state)	ILOH	PC6, PC7, PF0 to PF3	VDD = 5.5V, VOH = 12.0V			50	μA
		PF4 to PF7	VDD = 5.5V, VOH = 5.5V			10	μA
I <sup>2</sup> C bus switch connection impedance (in output Tr off state)	RBS	SCL0: SCL1 SDA0: SDA1	VDD = 4.5V VSCL0 = VSCL1 = 2.25V VSDA0 = VSDA1 = 2.25V			120	Ω
Supply current*2	IDD1	VDD	1/2 frequency dividing mode		27	42	mA
			VDD = 5.5V, 16MHz crystal oscillation (C1 = C2 = 15pF)				
			VDD = 5.5V, 24MHz crystal oscillation	40	63		
	IDD2		VDD = 3.3V, 32kHz crystal oscillation (C1 = C2 = 47pF)	40	95	μA	
	IDDS1		Sleep mode		2.2	3.9	mA
			VDD = 5.5V, 24MHz crystal oscillation (C1 = C2 = 15pF)				
	IDDS2		VDD = 3.3V, 32kHz crystal oscillation (C1 = C2 = 47pF)	17	45	μA	
IDDS3	Stop mode*3 VDD = 5.5V, termination of 24MHz and 32kHz oscillation	—	—	—	μA		

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	PA, PB, PC0 to PC5, PD, PE0 to PE3, PF4 to PF7, PG, EXTAL, EXLC, $\overline{\text{RST}}$	Clock 1MHz 0V other than the measured pins		10	20	pF

\*1 For  $\overline{\text{RST}}$  pin, specifies the input current when pull-up resistance is selected, and specifies the leakage current when non-resistor is selected.

\*2 When all output pins are left open. Specifies only when the OSD oscillation is stopped.

\*3 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig.2	8		24	MHz
System clock input pulse width	t <sub>XL</sub> , t <sub>XH</sub>	EXTAL	Fig. 1, Fig.2 External clock drive	17			ns
System clock input rise and fall times	t <sub>CR</sub> , t <sub>CF</sub>	EXTAL	Fig. 1, Fig.2 External clock drive			200	ns
Event count input clock pulse width	t <sub>EH</sub> , t <sub>EL</sub>	$\overline{EC}$	Fig. 3	4t <sub>sys</sub> *1			ns
Event count input clock rise and fall times	t <sub>ER</sub> , t <sub>EF</sub>	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	fc	TEX TX	V <sub>DD</sub> = 2.7 to 5.5V Fig. 2 (32kHz clock applied conditions)		32.768		kHz
Event count input clock input pulse width	t <sub>TL</sub> , t <sub>TH</sub>	TEX	Fig. 3	10			μs
Event count input clock rise and fall times	t <sub>TR</sub> , t <sub>TF</sub>	TEX	Fig. 3			20	ms

\*1 Indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

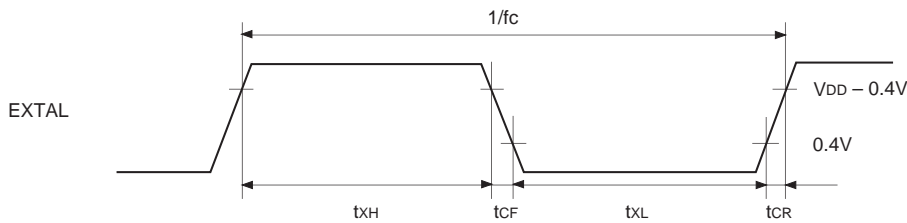


Fig. 1. Clock timing

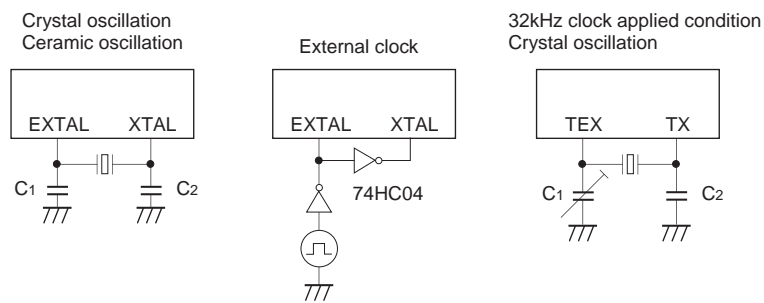


Fig.2. Clock applied conditions

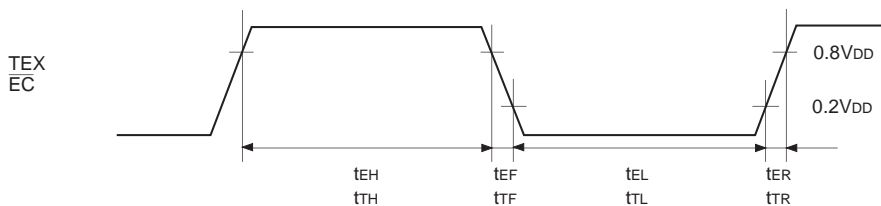


Fig. 3. Event count clock timing



(2) Serial transfer

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ High and Low level width	$t_{\text{KH}}$	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$ input mode	400		ns
	$t_{\text{KL}}$		$\overline{\text{SCK}}$ output mode	4000/fc - 50		ns
SI input setup time (for $\overline{\text{SCK}} \uparrow$ )	$t_{\text{SIK}}$	SI	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI hold time (for $\overline{\text{SCK}} \uparrow$ )	$t_{\text{KSI}}$	SI	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	$t_{\text{KSO}}$	SO	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

**Note)** The load of  $\overline{\text{SCK}}$  output mode and SO output delay time is  $50\text{pF} + 1\text{TTL}$ .

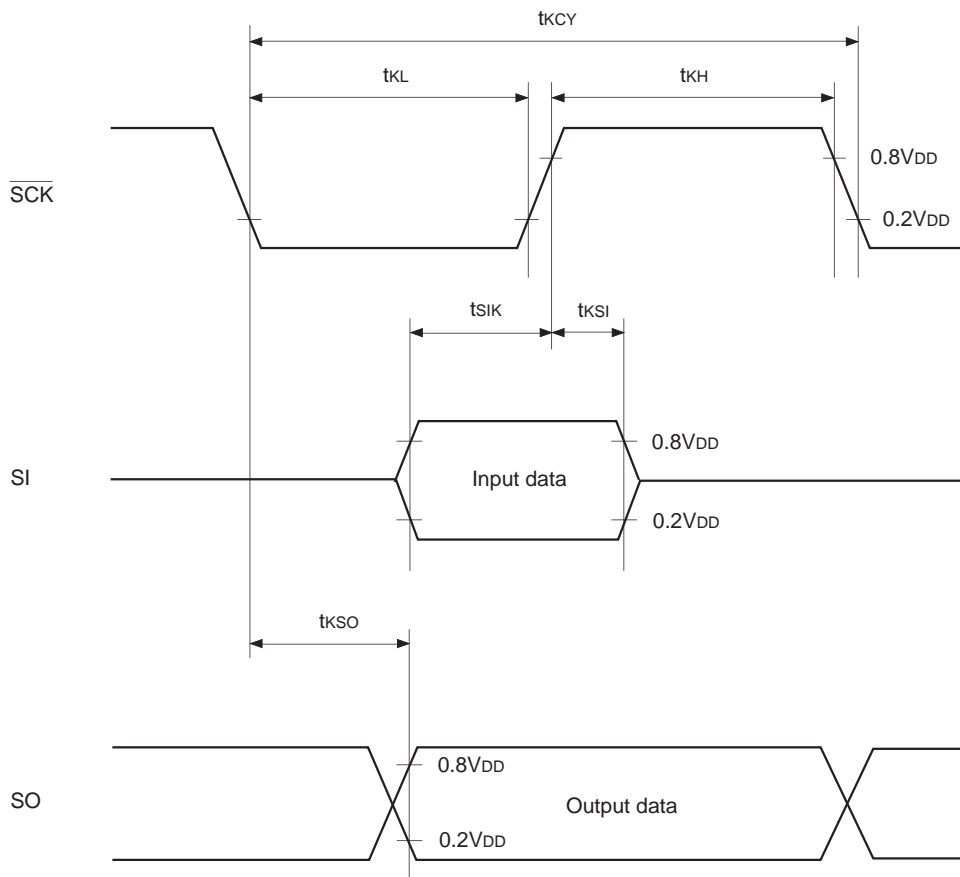
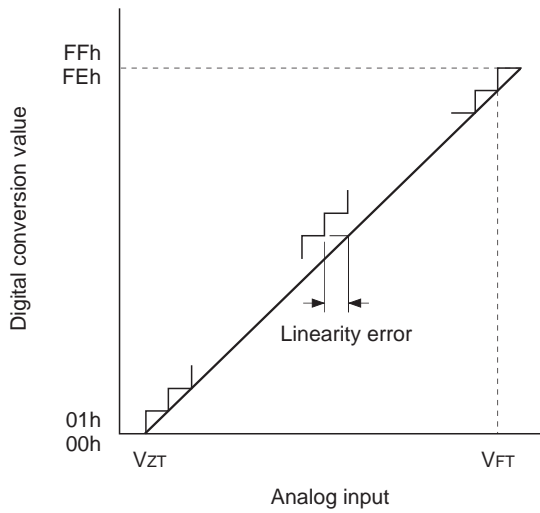


Fig. 4. Serial transfer timing

(3) A/D converter

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C VDD = 5.0V Vss = 0V			±3	LSB
Zero transition voltage	VZT*1			-10	10	70	mV
Full-scale transition voltage	VFT*2			4910	4970	5030	mV
Conversion time	tCONV			26/fADC*3			µs
Sampling time	tSAMP			6/fADC*3			µs
Analog input voltage	VIAN	AN0 to AN5		0		VDD	V

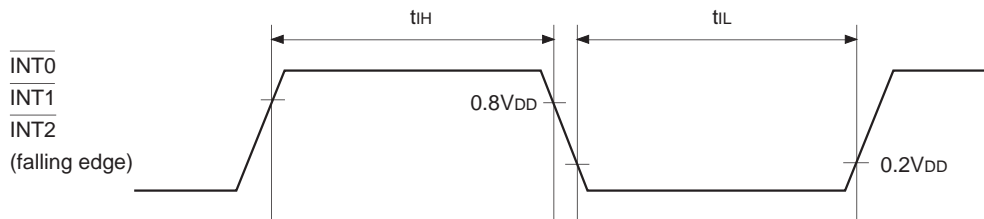


- \*1 VZT: Value at which the digital conversion value changes from 00h to 01h and vice versa.
- \*2 VFT: Value at which the digital conversion value changes from FEh to FFh and vice versa.
- \*3 fADC indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 000F6h):  
 $f_{ADC} = f_c$  (CKS = "0"),  $f_c/2$  (CKS = "1")

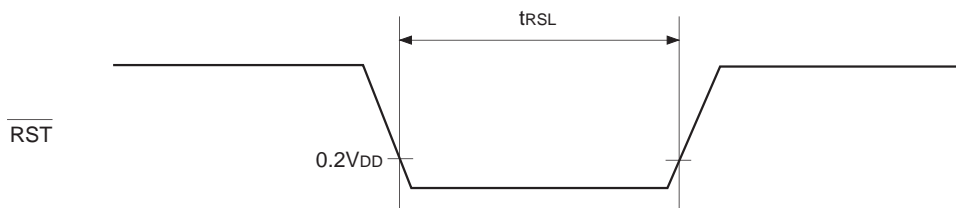
Fig. 5. Definitions for A/D converter terms

**(4) Interruption, reset input** ( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High, Low level width	$t_{IH}$ $t_{iL}$	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$		1		$\mu\text{s}$
Reset input Low level width	$t_{RSL}$	$\overline{\text{RST}}$		$32/f_c$		$\mu\text{s}$



**Fig. 6. Interruption input timing**



**Fig. 7.  $\overline{\text{RST}}$  input timing**

(5) I<sup>2</sup>C bus timing

(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCL clock frequency	f <sub>SCL</sub>	SCL		0	100	kHz
Bus-free time before starting transfer	t <sub>BUF</sub>	SDA, SCL		4.7		µs
Hold time for starting transfer	t <sub>HD; STA</sub>	SDA, SCL		4.0		µs
Clock Low level width	t <sub>LOW</sub>	SCL		4.7		µs
Clock High level width	t <sub>HIGH</sub>	SCL		4.0		µs
Setup time for repeated transfers	t <sub>SU; STA</sub>	SDA, SCL		4.7		µs
Data hold time	t <sub>HD; DAT</sub>	SDA, SCL		0*1		µs
Data setup time	t <sub>SU; DAT</sub>	SDA, SCL		250		ns
SDA, SCL rise time	t <sub>R</sub>	SDA, SCL			1	µs
SDA, SCL fall time	t <sub>F</sub>	SDA, SCL			300	ns
Setup time for transfer completion	t <sub>SU; STO</sub>	SDA, SCL		4.7		µs

\*1 The data hold time should be 300ns or more because the SCL rise time (300ns Max.) is not included in it.

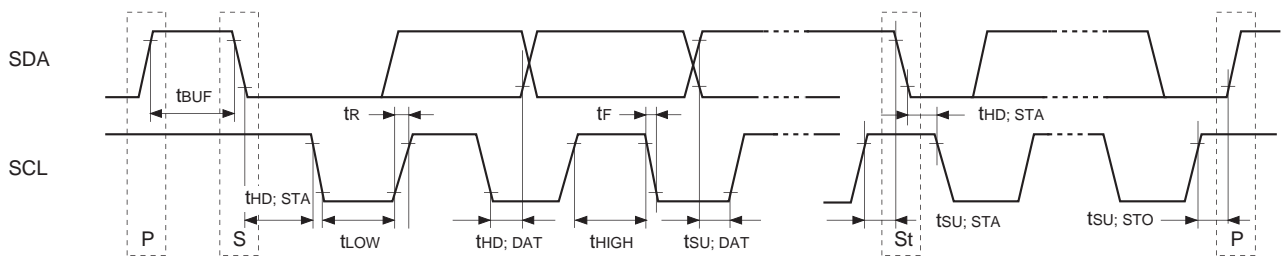


Fig. 8. I<sup>2</sup>C bus transfer timing

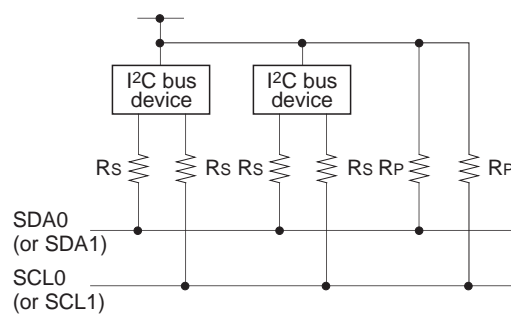


Fig. 9. I<sup>2</sup>C bus device recommended circuit

- A pull-up resistor (Rp) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce the spike noise caused by CRT flashover.

(6) OSD timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
OSD clock frequency	fosc*1	EXLC XLC	Fig. 11	4	40.8	MHz
HSYNC pulse width	tHWD	HSYNC	Fig. 10	30/fc		µs
VSYNC pulse width	tvWD	VSYNC	Fig. 10	1		H*2
HSYNC afterwrite rise and fall times	tHCG	HSYNC	Fig. 10		200	ns
VSYNC beforewrite rise and fall times	tvCG	VSYNC	Fig. 10		1.0	µs

\*1 The maximum value of fosc is specified with the following equation.

$$fosc [max] \leq fc \times 1.7$$

\*2 H indicates 1HSYNC period.

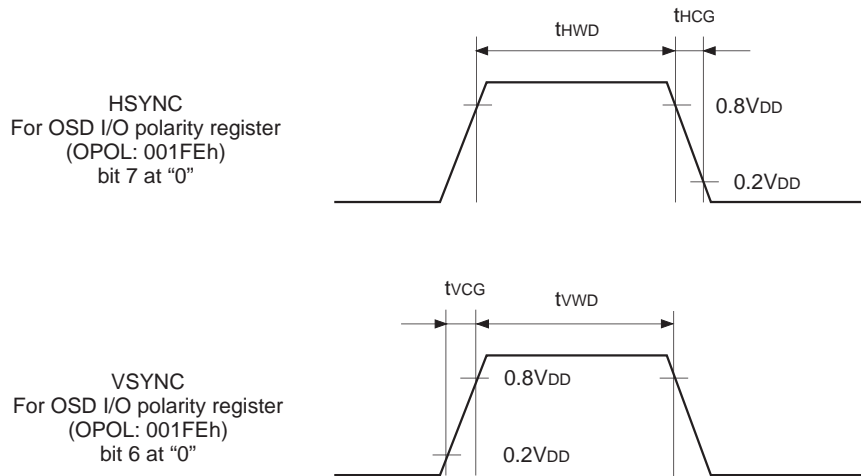


Fig. 10. OSD timing

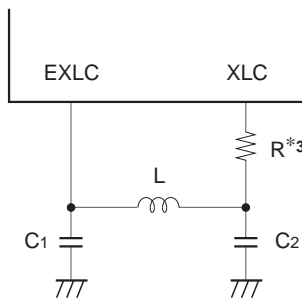


Fig. 11. LC oscillation circuit connection

\*3 The series resistor for XLC (R = 1kΩ or less) can reduce the frequency of occurrence of the undesired radiation.

Appendix

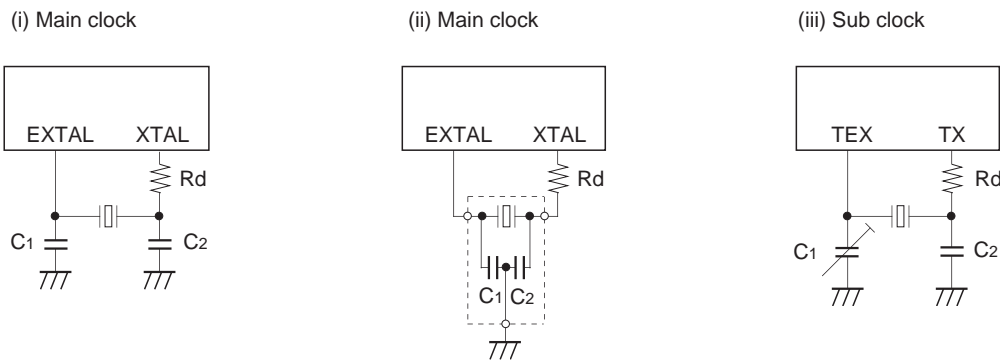


Fig. 12. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example	Remarks
MURATA MFG CO., LTD.	CSA10.0MTZ	10.0	30	30	0*1	(i)	
	CSA12.0MTZ	12.0					
	CSA16.00MXZ040	16.0	5	5			
	CSA24.00MXZ040	24.0	OPEN	OPEN			
	CST10.0MTW*	10.0	30	30		(ii)	
	CST12.0MTW*	12.0					
	CST16.00MXW0C1*	16.0	5	5			
RIVER ELETEC CORPORATION	HC-49/U03	8.0	18	18	330*1	(i)	
		12.0	12	12			
		16.0	10	10			
KINSEKI LTD.	HC-49/U (-S)	8.0	10	10	0*1	(i)	
		12.0	5	5			
		16.0	OPEN	OPEN			
		24.0	3	3			
	P3	32.768kHz	33	30	120k	(iii)	
Seiko Instruments Inc.	VTC-200 SP-T	32.768kHz	18	18	330k	(iii)	CL = 12.5pF

\* Models with an asterisk (\*) have the built-in ground capacitance (C1, C2).

\*1 The series resistor for XTAL (Rd = 500Ω or less) can reduce the effect of the noise caused by the electrostatic discharge.

Mask Option Table

Item	Mask ROM	CXP7500P10-1-□□□	CXP7500P11-2-□□□
Package	64-pin plastic SDIP/QFP 52-pin plastic SDIP	64-pin plastic SDIP/QFP	52-pin plastic SDIP
ROM capacitance	96K/120K byte	PROM 120K byte	PROM 120K byte
Reset pin pull-up resistor	Existent/Non-existent	Existent	Existent

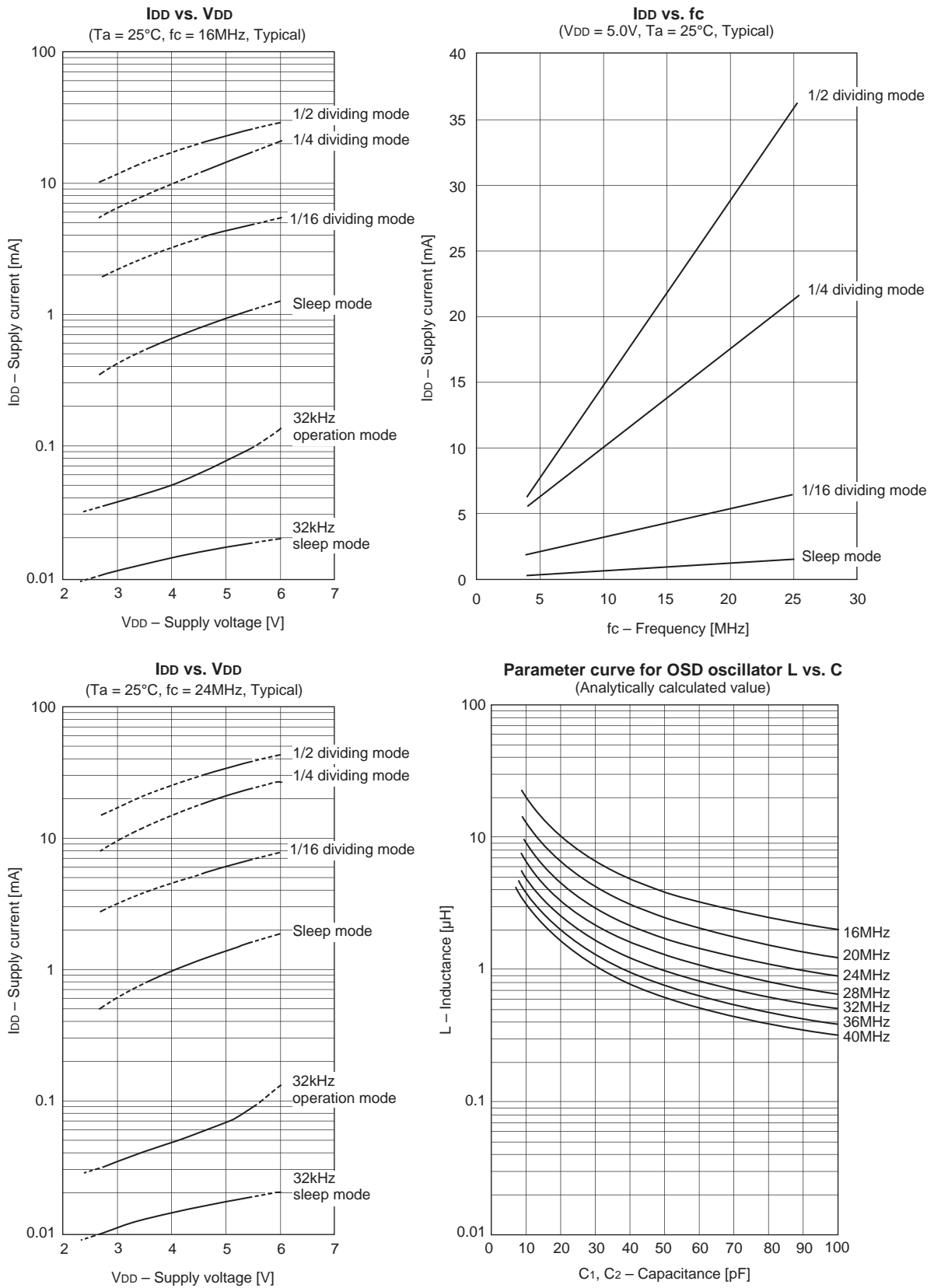
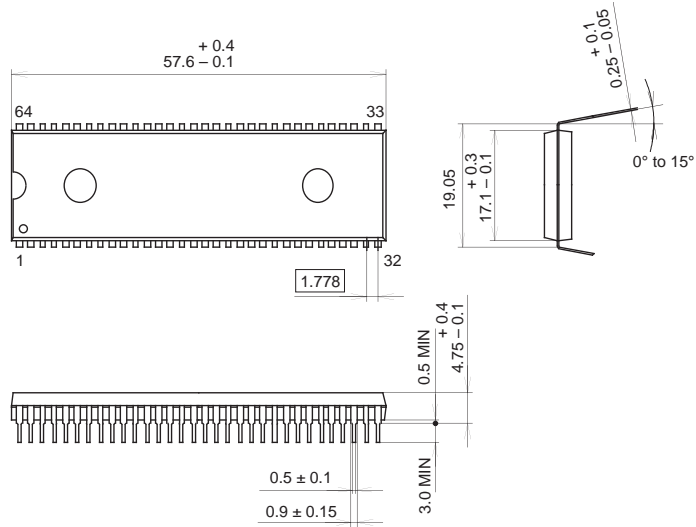


Fig. 13. Characteristic curves

Package Outline

Unit: mm

64PIN SDIP (PLASTIC)

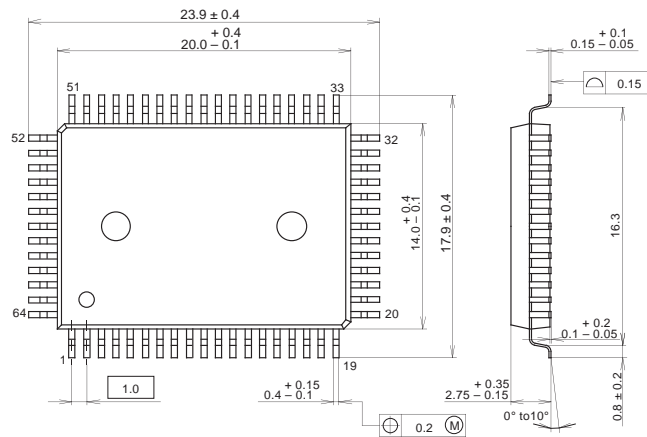


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	SDIP064-P-0750
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	8.6g

64PIN QFP(PLASTIC)



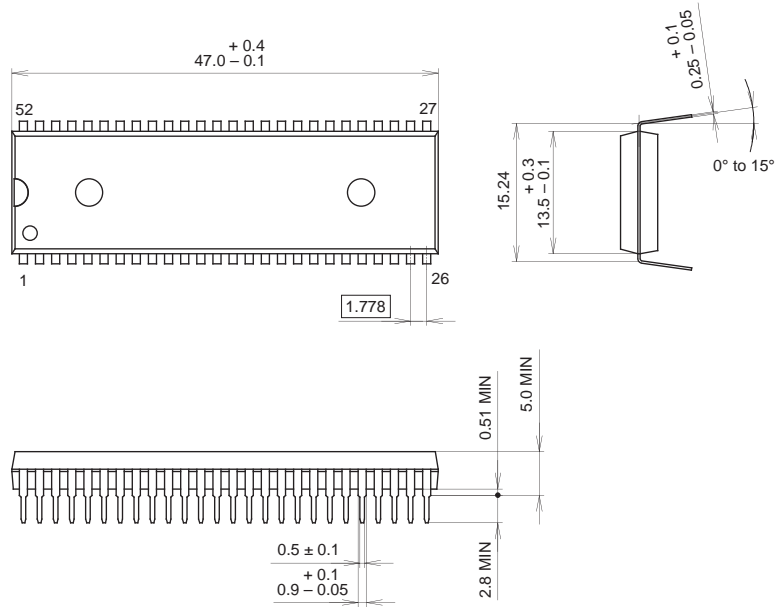
PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g



52PIN SDIP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SDIP-52P-01
EIAJ CODE	SDIP052-P-0600
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	5.6g