



LA6242H — Monolithic Linear IC Four-Channel Bridge Driver for CD Player

Overview

The LA6242H is a four-channel motor driver IC for home and car CD players. It provides a pin for switching the channel 1 input.

Functions and Features

- Four bridge-connected (BTL) power amplifier circuits
- I_O max: 1 A
- Built-in level shifter circuits
- Muting circuit (on/off control for all outputs)
- High output voltage (dynamic range): 6.5 V (typical, channel 1 only)
- Built-in input operational amplifier (channel 1 only)
- Channel 1 input operational amplifier switching function
- Built-in regulator that uses an external PNP transistor and is set by the value of an external resistor.

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC_S}	*1	14	V
	VCCP	VCCP1, VCCP2	14	V
Allowable power dissipation	Pdmax	Independent IC	0.8	W
		Mounted on the specified PCB (114.3 × 76.1 × 1.6 mm, glass epoxy)	1.8	W
Maximum input voltage	VINB		13	V
Maximum output current	I_O max	Each output	1	A
MUTE pin voltage	VMUTE		13	V
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

Note *1: All of the power supply pins, V_{CC_S} , VCCP1, and VCCP2, must be connected to the power supply system externally to the IC.

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5 to 13	V

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Electrical Characteristics

(Unless specified otherwise, the conditions are $V_{CC_S} = V_{CCP1} = V_{CCP2} = 8\text{ V}$, $V_{REF} = 2.5\text{ V}$, $MUTE = 5\text{ V}$, $T_a = 25^\circ\text{C}$.)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Overall]						
Quiescent current 1	I_{CC-ON}	All channel outputs on, MUTE pin: high		30	45	mA
Quiescent current 2	I_{CC-OFF}	All channel outputs off, MUTE pin: low		5	10	mA
Muting function on voltage	$V_{MUTE-ON}$	MUTE *1	2			V
Muting function off voltage	$V_{MUTE-OFF}$	MUTE *1			0.5	V
[BTL Amplifier] (Channel 1) (Output Amplifier Block)						
Input amplifier offset voltage	V_{OFF_OP-AMP}	Channel 1, input operational amplifiers A and B	-50		+50	mV
Output voltage	V_{O1}	$R_L = 8\ \Omega$ *2	6.2	6.5		V
I/O gain	V_{G1}	*3	5.4	6	6.6	Multiplier
Slew rate	$SR1$	With the amplifier operating independently, twice the value measured between outputs *4		0.5		V/ μ s
[Input Operational Amplifier]						
Output offset voltage	V_{OFF1}	Input operational amplifiers A and B	-10		+10	mV
OP-AMP_SINK	OP_SINK	Input operational amplifier sink current	2			mA
OP-AMP_SOURCE	OP_SOURCE	Input operational amplifier source current	300	500		μ A
[Input Operational Amplifier Switching]						
Input amplifier switching voltage 1	V_{IN1-SW}	Channel 1, with input operational amplifier B selected *5			0.5	V
Input amplifier switching voltage 2	V_{IN1-SW}	Channel 1, with input operational amplifier A selected *5	2			V
[BTL Amplifier] (Channels 2 to 4) (Output Amplifier Block)						
Output offset voltage	V_{OFF2}	Between the + and - outputs for each channel	-50		+50	mV
Output voltage	V_{O2}	$R_L = 8\ \Omega$, between the + and - outputs for each channel *2	5	5.4		V
I/O gain	V_{G2}		5.4	6	6.6	Multiplier
Slew rate	$SR2$	Amplifier independently, twice the value measured between outputs *4		0.5		V/ μ s
[Regulator Voltage]						
VREG output voltage	V_{REG}	*6	1.21	1.26	1.31	V
REG-IN sink current	$REG-IN-SINK$	The base current of the external PNP transistor	5	10		mA
Line regulation	ΔV_{OLN}	$6\text{ V} \leq V_{CC} \leq 12\text{ V}$, $I_O = 200\text{ mA}$		20	150	mV
Load regulation	ΔV_{OLD}	$5\text{ mA} \leq I_O \leq 200\text{ mA}$		50	200	mV

Note *1: When the MUTE pin is high, the outputs will be on, and when low, the outputs will be off. (In the amplifier output off state, the outputs are in the high-impedance state.) This operation applies to all channels.

*2: The voltage across the load terminals when an $8\ \Omega$ load is connected across the outputs. With the input either high or low. With the output in the saturated state.

*3: The channel 1 input operational amplifier has a 0 dB gain, i.e. it is a buffer amplifier.

*4: Design guarantee value

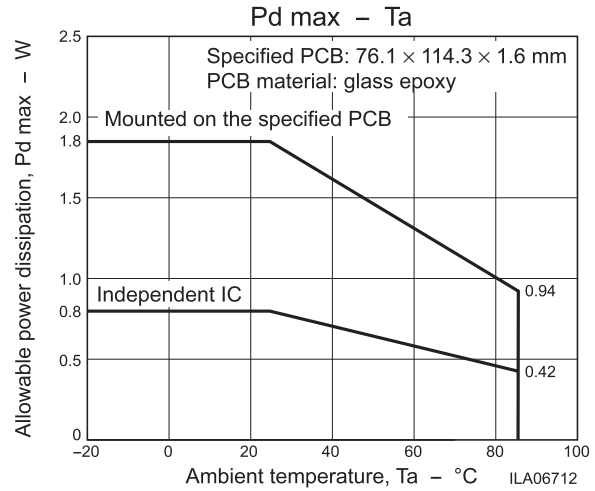
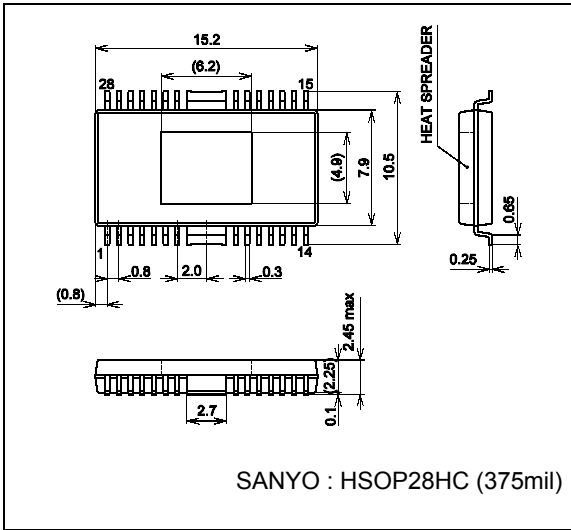
*5: When V_{IN1-SW} is high, operational amplifier A operates, and when low, operational amplifier B operates.

*6: For testing, short the REGOUT to the collector of the external pnp transistor.

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Package Dimensions

unit: mm
3234B



Pin Functions

Pin No.	Symbol	Pin description
1	V _{IN1-A}	Channel 1 input amplifier A inverting input
2	V _{IN1+A}	Channel 1 input amplifier A noninverting input
3	V _{CCP1}	Channels 1 and 2: power stage power supply
4	V _{O1+}	Channel 1 output (+)
5	V _{O1-}	Channel 1 output (-)
6	V _{O2+}	Channel 2 output (+)
7	V _{O2-}	Channel 2 output (-)
8	V _{O3+}	Channel 3 output (+)
9	V _{O3-}	Channel 3 output (-)
10	V _{O4+}	Channel 4 output (+)
11	V _{O4-}	Channel 4 output (-)
12	V _{CCP2}	Channels 3 and 4: power stage power supply
13	V _{IN4}	Channel 4 input
14	V _{IN4G}	Channel 4 input (gain adjustment)
15	V _{IN3}	Channel 3 input
16	V _{IN3G}	Channel 3 input (gain adjustment)
17	V _{IN2}	Channel 2 input
18	V _{IN2G}	Channel 2 input (gain adjustment)
19	REGIN	Base connection of external PNP transistor
20	REGOUT	Regulator error amplifier input (+)
21	V _{CC-S}	Signal system power supply
22	VREFIN	Reference voltage input
23	MUTE	Output on/off control
24	V _{IN1-SW}	Channel 1 input operational amplifier switching
25	S_GND	Signal system ground
26	V _{IN1+B}	Channel 1 amplifier B noninverting input
27	V _{IN1-B}	Channel 1 amplifier B inverting input
28	V _{IN1}	Channel 1 input and input operational amplifier output

- Note:
- The center frame (FR) is used as the power system ground (P-GND). Along with the signal system ground (S-GND), this level must be the lowest potential in the system.
 - The V_{CC-S} (signal system power supply), V_{CCP1}, and V_{CCP2} (output stage power supplies) must be shorted together externally.

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Pin Functions

Pin No.	Pin name	Symbol	Pin description	Equivalent circuit
1 2 26 27 28	Input (channel 1)	V_{IN1-A} V_{IN1+A} V_{IN1+B} V_{IN1-B} V_{IN1}	Inputs The total gain is set by setting the gain of the input amplifier.	
4 5	Output (channel 1)	V_{O1+} V_{O1-}	Channel 1 output	
6 7 8 9 10 11	Output (channels 2 to 4)	V_{O2+} V_{O2-} V_{O3+} V_{O3-} V_{O4+} V_{O4-}	Channel 2 to 4 outputs	
23	MUTE	MUTE	Controls the on/off states of the corresponding channel output. MUTE = high: Output on MUTE = low: Output off *: When the MUTE pin is open, the outputs will be off. (The same as when the MUTE pin is low.)	
24	Channel 1 input amplifier switching	V_{IN1-SW}	Channel 1 input operational amplifier switching function. Either amplifier A or amplifier B is selected according to the voltage applied to the V_{IN1-SW} pin. High: V_{IN_A} Low: V_{IN_B}	

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Pin No.	Pin name	Symbol	Pin description	Equivalent circuit
17 18 15 16 13 14	Input (channels 2 to 4)	V_{IN2} V_{IN2G} V_{IN3} V_{IN3G} V_{IN4} V_{IN4G}	Inputs	
22	VREF	VREFIN	Reference voltage	
19 20	REG	REGIN REGOUT	Regulator block	

MUTE, V_{IN}1-SW

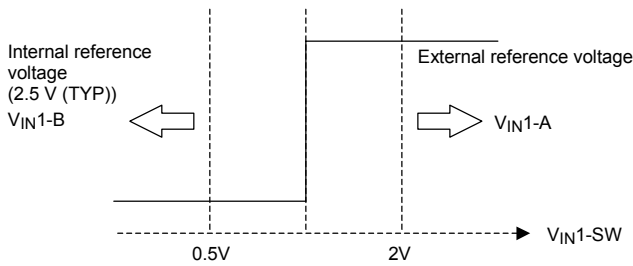
- Relationship between the MUTE pin and the outputs

MUTE	Outputs			
	CH1	CH2	CH3	CH4
H	on			
L	off			

Note *1: When the outputs are off, they are in the high-impedance state.
 *2: The muting function applies to all channels.

- V_{IN}1-SW and the channel 1 input operational amplifier

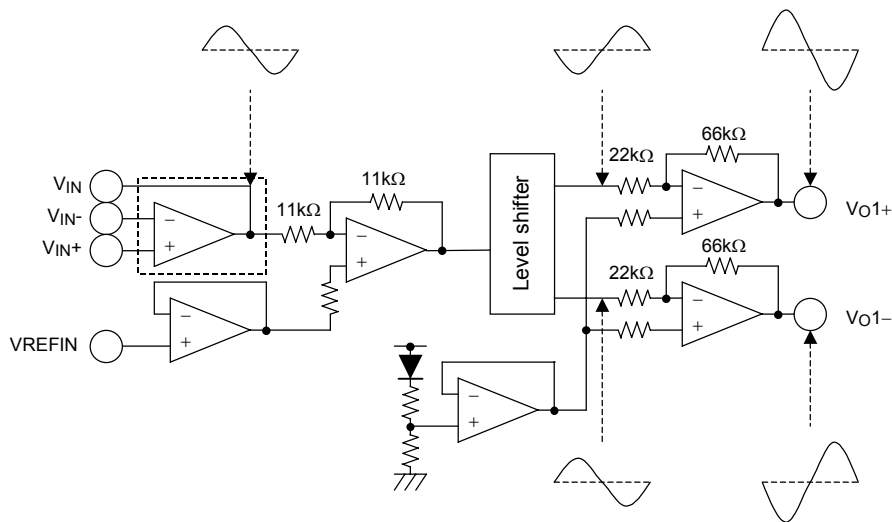
V _{IN} 1_SW	Channel 1 input operational amplifier
H	AMP_A
L	AMP_B



- Muting

MUTE	Output amplifiers
L	off
H	on

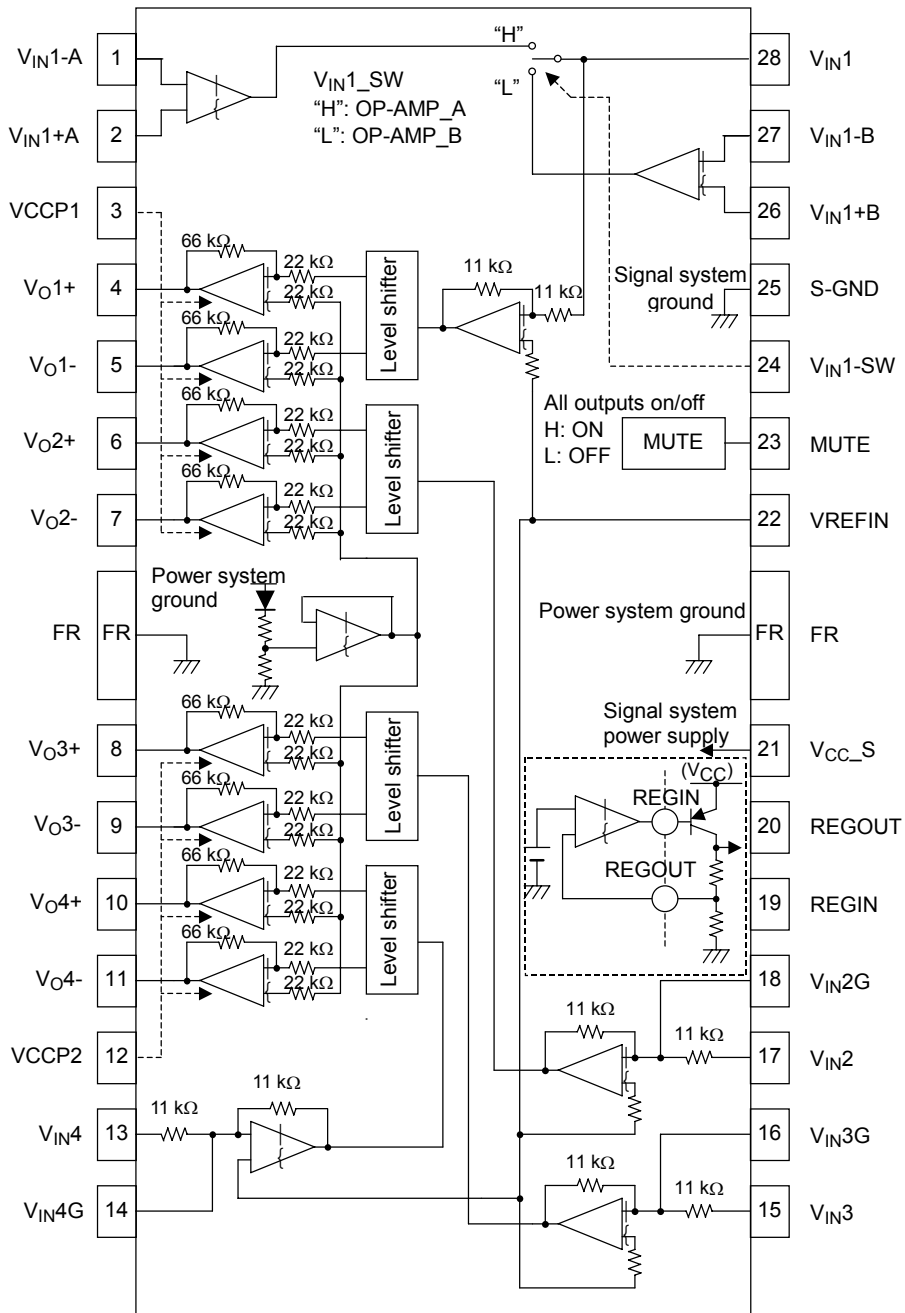
Overview of the input/output relationship



Note *: Only channel 1 has an added input operational amplifier.

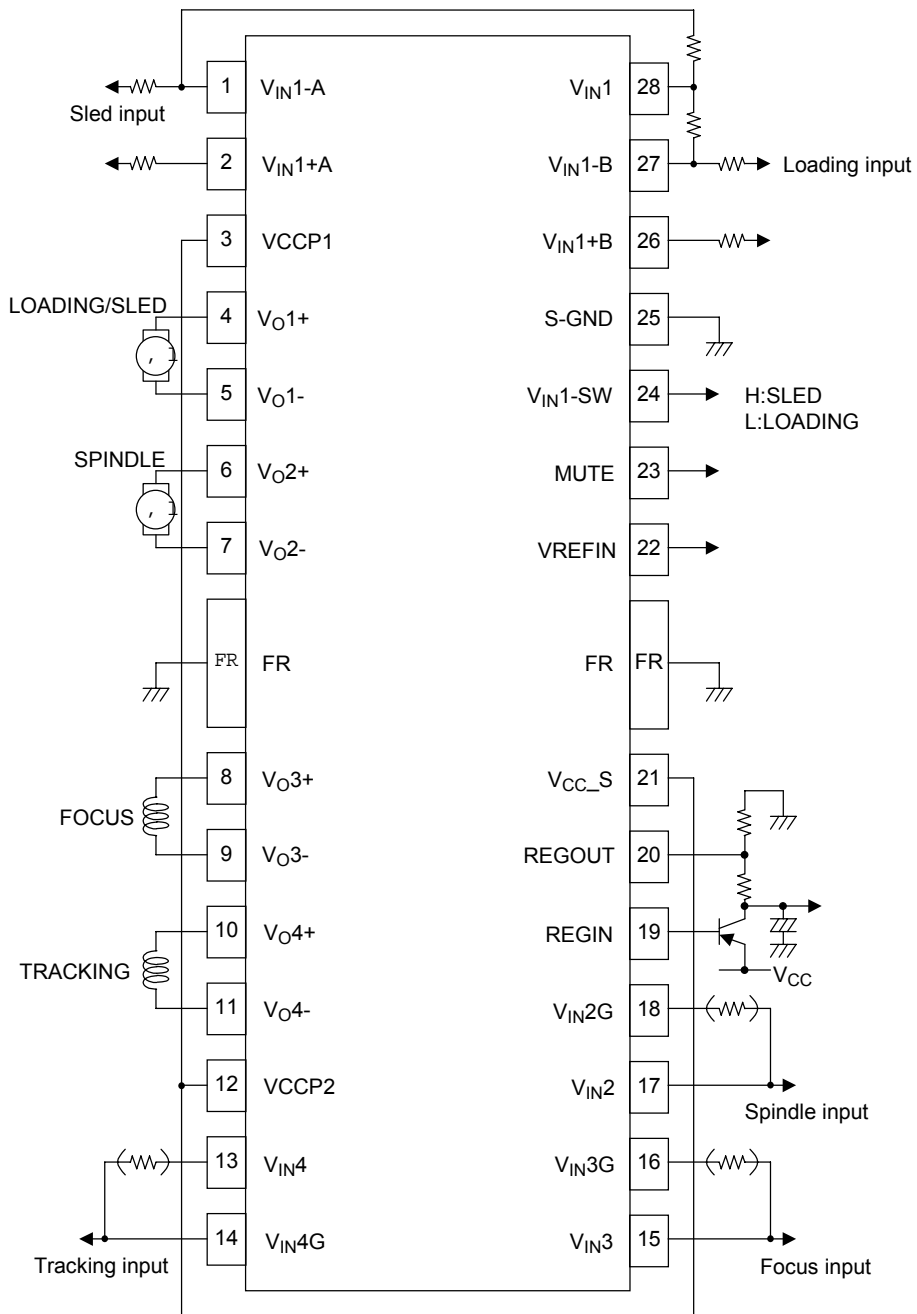
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Block Diagram



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Sample Application Circuit



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