LH1562

240-output LCD Segment/Common Driver IC

DESCRIPTION

The LH1562 is a 240-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The LH1562 is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

FEATURES

- Number of LCD drive outputs : 240
- Supply voltage for LCD drive : +15.0 to +42.0 V
- Supply voltage for the logic system : +2.5 to +5.5 V
- Low power consumption
- Low output impedance
- Package : 269-pin TCP (Tape Carrier Package)

(Segment mode)

- Shift clock frequency
  - 20 MHz (MAX.) : V_{DD} = +5.0±0.5 V
  - 15 MHz (MAX.) : V_{DD} = +3.0 to +4.5 V
  - 12 MHz (MAX.) : V_{DD} = +2.5 to +3.0 V
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 240 bits of input data
- Line latch circuits are reset when $\overline{DISPOFF}$ active

(Common mode)

- Shift clock frequency : 4 MHz (MAX.)
- Built-in 240-bit bi-directional shift register (divisible into 120 bits x 2)
- Available in a single mode (240-bit shift register) or in a dual mode (120-bit shift register x 2)

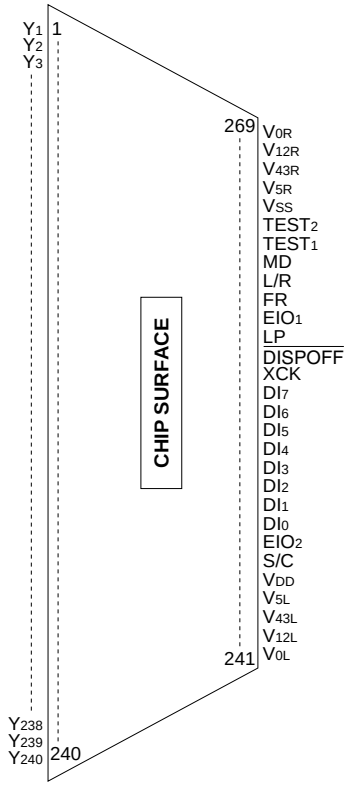
① $Y_1 \rightarrow Y_{240}$ Single mode
② $Y_{240} \rightarrow Y_1$ Single mode
③ $Y_1 \rightarrow Y_{120}$, $Y_{121} \rightarrow Y_{240}$ Dual mode
④ $Y_{240} \rightarrow Y_{121}$, $Y_{120} \rightarrow Y_1$ Dual mode

The above 4 shift directions are pin-selectable

- Shift register circuits are reset when $\overline{DISPOFF}$ active

PIN CONNECTIONS

269-PIN TCP TOP VIEW

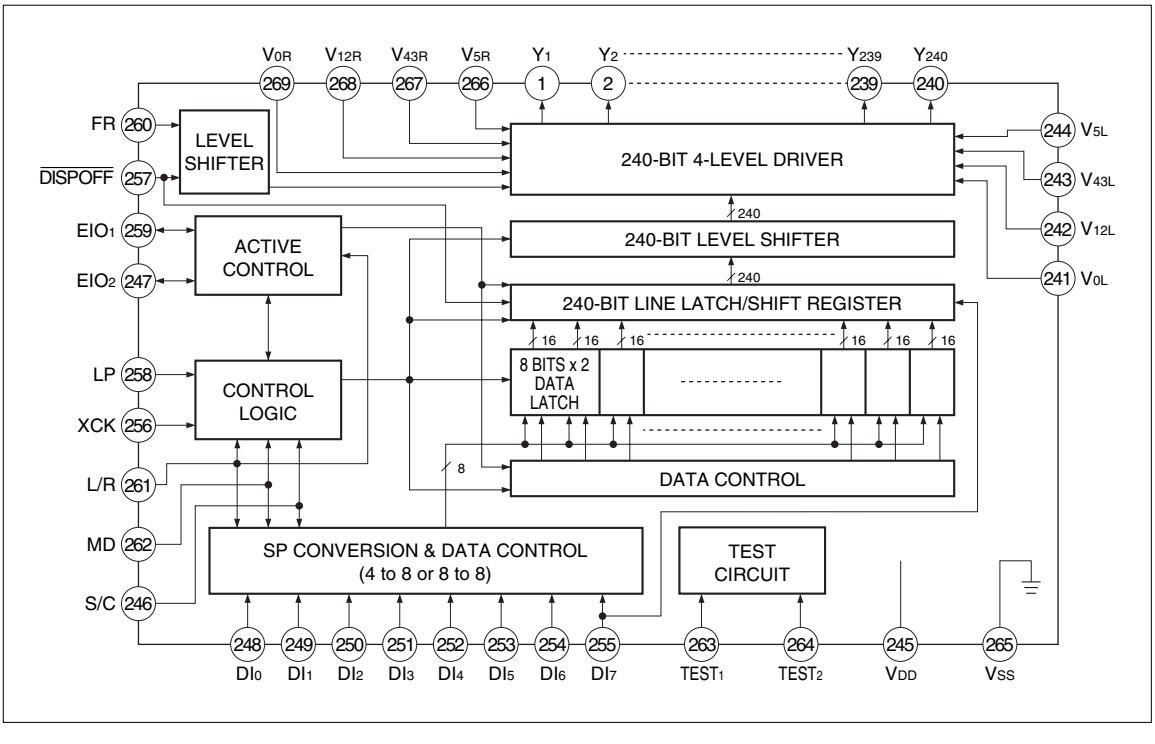


NOTE :
Doesn't prescribe TCP outline.

PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 240	Y_1-Y_{240}	O	LCD drive output
241, 269	V_{0L}, V_{0R}	–	Power supply for LCD drive
242, 268	V_{12L}, V_{12R}	–	Power supply for LCD drive
243, 267	V_{43L}, V_{43R}	–	Power supply for LCD drive
244, 266	V_{5L}, V_{5R}	–	Power supply for LCD drive
245	V_{DD}	–	Power supply for logic system (+2.5 to +5.5 V)
246	S/C	I	Segment mode/common mode selection
247, 259	EIO_2, EIO_1	I/O	Input/output for chip selection at segment mode/ Shift data input/output for shift register at common mode
248 to 254	DI_0-DI_6	I	Display data input at segment mode
255	DI_7	I	Display data input at segment mode/Dual mode data input at common mode
256	XCK	I	Clock input for taking display data at segment mode
257	$\overline{DISPOFF}$	I	Control input for output of non-select level
258	LP	I	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode
260	FR	I	AC-converting signal input for LCD drive waveform
261	L/R	I	Input for selecting the reading direction of display data at segment mode/ Input for selecting the shift direction of shift register at common mode
262	MD	I	Mode selection input
263, 264	$TEST_1$, $TEST_2$	I	Test mode selection input
265	V_{SS}	–	Ground (0 V)

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Active Control	In case of segment mode, controls the selection or non-selection of the chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.
SP Conversion & Data Control	In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel input mode in latch circuit; after that they are put on the internal data bus 8 bits at a time.
Data Latch Control	In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 240 bits of data are read in 30 sets of 8 bits.
Line Latch/ Shift Register	In case of segment mode, all 240 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels (V_0, V_{12}, V_{43}, or V_5) based on the S/C, FR and $\overline{DISPOFF}$ signals.
Control Logic	Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 240 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift.
Test Circuit	The circuit for testing. During normal operation, it isn't activated.

INPUT/OUTPUT CIRCUITS

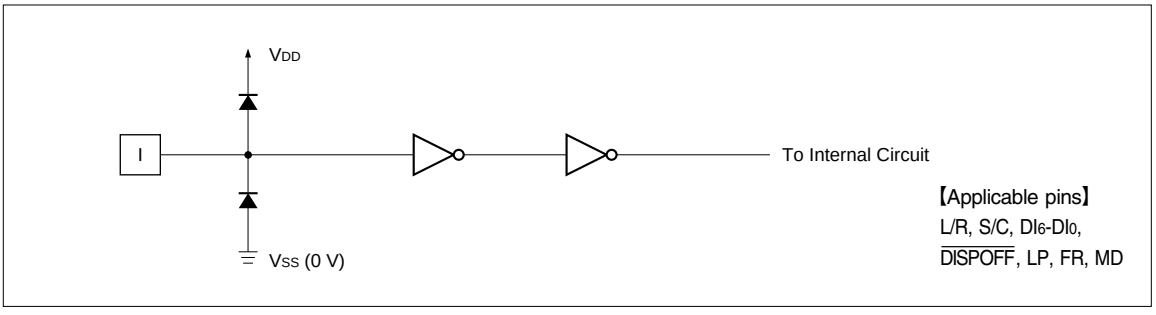


Fig. 1 Input Circuit (1)

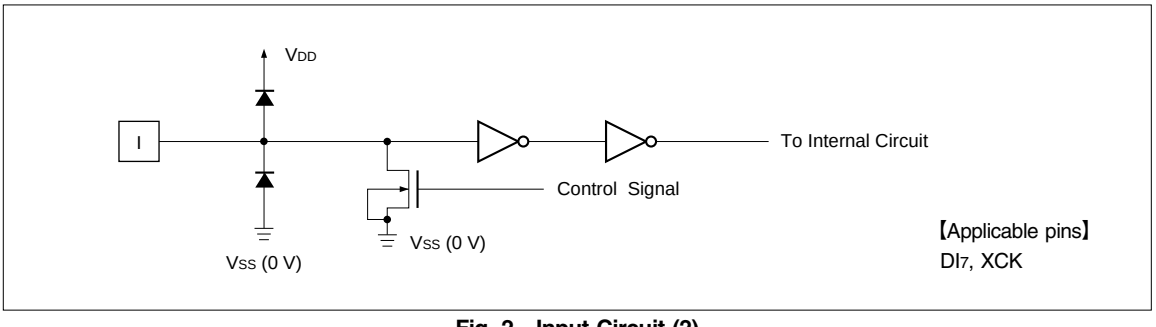


Fig. 2 Input Circuit (2)

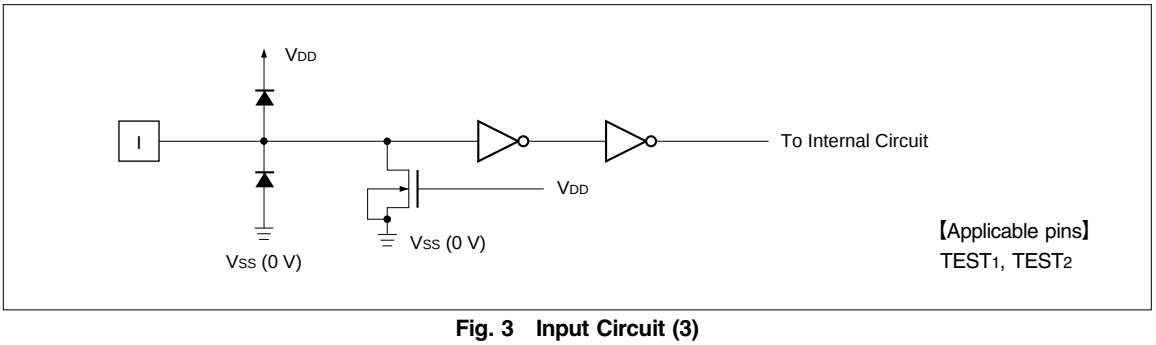


Fig. 3 Input Circuit (3)

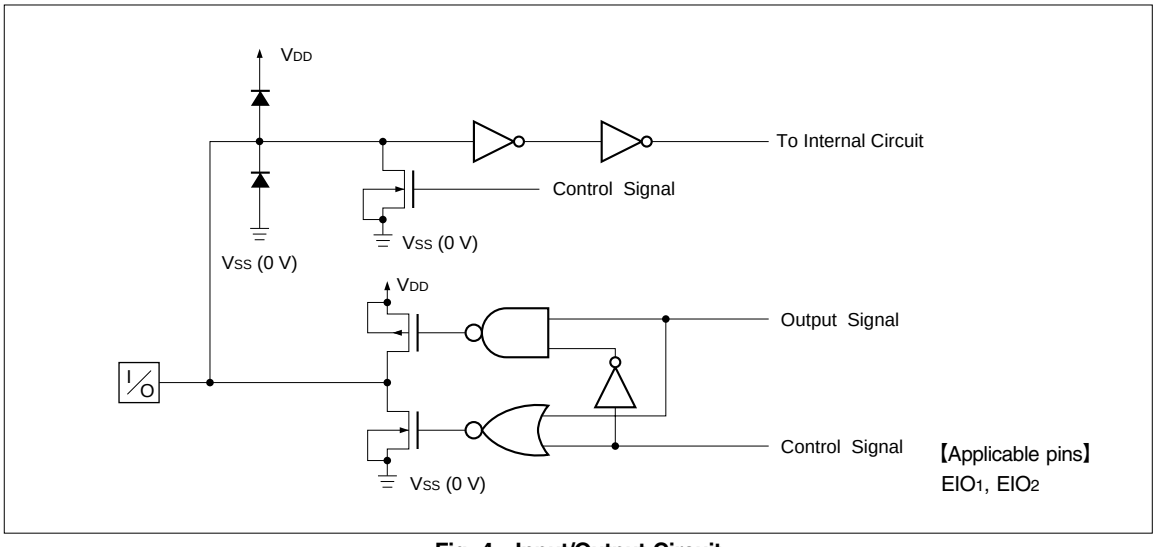


Fig. 4 Input/Output Circuit

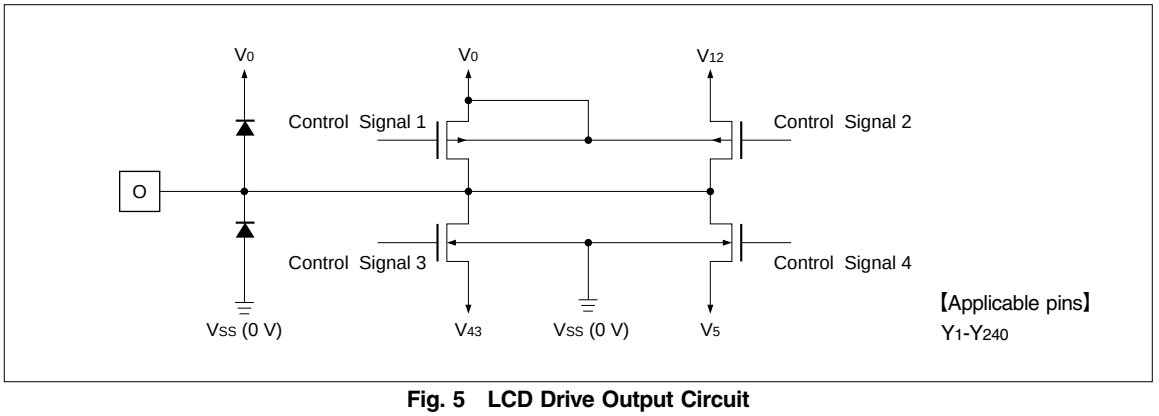


Fig. 5 LCD Drive Output Circuit

FUNCTIONAL DESCRIPTION

Pin Functions

(Segment mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R} V_{5L}, V_{5R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider. • Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$. • V_{iL} and V_{iR} (i = 0, 12, 43, 5) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin.
DI_7-DI_0	Input pins for display data • In 4-bit parallel input mode, input data into the 4 pins, DI_3-DI_0. Connect DI_7-DI_4 to V_{SS} or V_{DD}. • In 8-bit parallel input mode, input data into the 8 pins, DI_7-DI_0. • Refer to **"RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS"** in Functional Operations.
XCK	Clock input pin for taking display data • Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
L/R	Input pin for selecting the reading direction of display data • When set to V_{SS} level "L", data is read sequentially from Y_{240} to Y_1. • When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{240}. • Refer to **"RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS"** in Functional Operations.
$\overline{DISPOFF}$	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (Y_1-Y_{240}) are set to level V_5. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of $\overline{DISPOFF}$. When the $\overline{DISPOFF}$ function is canceled, the driver outputs non-select level (V_{12} or V_{43}), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if $\overline{DISPOFF}$ removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly. • Table of truth values is shown in **"TRUTH TABLE"** in Functional Operations.

SYMBOL	FUNCTION
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.
MD	Mode selection pin • When set to V_{SS} level "L", 8-bit parallel input mode is set. • When set to V_{DD} level "H", 4-bit parallel input mode is set. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
S/C	Segment mode/common mode selection pin • When set to V_{DD} level "H", segment mode is set.
EIO_1, EIO_2	Input/output pins for chip selection • When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input. • When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. • During output, set to "H" while LP · $\overline{XCK}$ is "H" and after 240 bits of data have been read, set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H". • During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 240 bits of data have been read.
$TEST_1$ $TEST_2$	Test mode selection pins • During normal operation, fix to V_{SS} level "L".
Y_1-Y_{240}	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.

(Common mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R} V_{5L}, V_{5R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider. • Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$. • V_{iL} and V_{iR} (i = 0, 12, 43, 5) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin.
EIO_1	Shift data input/output pin for bi-directional shift register • Output pin when L/R is at V_{SS} level "L", input pin when L/R is at V_{DD} level "H". • When L/R = H, EIO_1 is used as input pin, it will be pulled down. • When L/R = L, EIO_1 is used as output pin, it won't be pulled down. • Refer to **"RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS"** in Functional Operations.
EIO_2	Shift data input/output pin for bi-directional shift register • Input pin when L/R is at V_{SS} level "L", output pin when L/R is at V_{DD} level "H". • When L/R = L, EIO_2 is used as input pin, it will be pulled down. • When L/R = H, EIO_2 is used as output pin, it won't be pulled down. • Refer to **"RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS"** in Functional Operations.
LP	Shift clock pulse input pin for bi-directional shift register • Data is shifted at the falling edge of the clock pulse.
L/R	Input pin for selecting the shift direction of bi-directional shift register • Data is shifted from Y_{240} to Y_1 when set to V_{SS} level "L", and data is shifted from Y_1 to Y_{240} when set to V_{DD} level "H". • Refer to **"RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS"** in Functional Operations.
$\overline{DISPOFF}$	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (Y_1-Y_{240}) are set to level V_5. • When set to "L", the contents of the shift register are reset to not reading data. When the $\overline{DISPOFF}$ function is canceled, the driver outputs non-select level (V_{12} or V_{43}), and the shift data is read at the next falling edge of the LP. At that time, if $\overline{DISPOFF}$ removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. • Table of truth values is shown in **"TRUTH TABLE"** in Functional Operations.

SYMBOL	FUNCTION
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.
MD	Mode selection pin • When set to V_{SS} level "L", single mode operation is selected; when set to V_{DD} level "H", dual mode operation is selected. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
DI_7	Dual mode data input pin • According to the data shift direction of the data shift register, data can be input starting from the 121st bit. When the chip is used in dual mode, DI_7 will be pulled down. When the chip is used in single mode, DI_7 won't be pulled down. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
S/C	Segment mode/common mode selection pin • When set to V_{SS} level "L", common mode is set.
DI_6-DI_0	Not used • Connect DI_6-DI_0 to V_{SS} or V_{DD}, avoiding floating.
XCK	Not used • XCK is pulled down in common mode, so connect to V_{SS} or open.
$TEST_1$ $TEST_2$	Test mode selection pins • During normal operation, fix to V_{SS} level "L".
Y_1-Y_{240}	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.

Functional Operations

TRUTH TABLE

(Segment Mode)

FR	LATCH DATA	$\overline{DISPOFF}$	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y_1-Y_{240})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_5

(Common Mode)

FR	LATCH DATA	$\overline{DISPOFF}$	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y_1-Y_{240})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
X	X	L	V_5

NOTES :

- $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.
  There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.
  Supply regular voltage which is assigned by specification for each power pin.

RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(Segment Mode)

(a) 4-bit Parallel Input Mode

MD	L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					60 CLOCK	59 CLOCK	58 CLOCK	···	3 CLOCK	2 CLOCK	1 CLOCK
H	L	Output	Input	DI_0	Y_1	Y_5	Y_9	···	Y_{229}	Y_{233}	Y_{237}
				DI_1	Y_2	Y_6	Y_{10}	···	Y_{230}	Y_{234}	Y_{238}
				DI_2	Y_3	Y_7	Y_{11}	···	Y_{231}	Y_{235}	Y_{239}
				DI_3	Y_4	Y_8	Y_{12}	···	Y_{232}	Y_{236}	Y_{240}
H	H	Input	Output	DI_0	Y_{240}	Y_{236}	Y_{232}	···	Y_{12}	Y_8	Y_4
				DI_1	Y_{239}	Y_{235}	Y_{231}	···	Y_{11}	Y_7	Y_3
				DI_2	Y_{238}	Y_{234}	Y_{230}	···	Y_{10}	Y_6	Y_2
				DI_3	Y_{237}	Y_{233}	Y_{229}	···	Y_9	Y_5	Y_1

(b) 8-bit Parallel Input Mode

MD	L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					30 CLOCK	29 CLOCK	28 CLOCK	···	3 CLOCK	2 CLOCK	1 CLOCK
L	L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	···	Y_{217}	Y_{225}	Y_{233}
				DI_1	Y_2	Y_{10}	Y_{18}	···	Y_{218}	Y_{226}	Y_{234}
				DI_2	Y_3	Y_{11}	Y_{19}	···	Y_{219}	Y_{227}	Y_{235}
				DI_3	Y_4	Y_{12}	Y_{20}	···	Y_{220}	Y_{228}	Y_{236}
				DI_4	Y_5	Y_{13}	Y_{21}	···	Y_{221}	Y_{229}	Y_{237}
				DI_5	Y_6	Y_{14}	Y_{22}	···	Y_{222}	Y_{230}	Y_{238}
				DI_6	Y_7	Y_{15}	Y_{23}	···	Y_{223}	Y_{231}	Y_{239}
				DI_7	Y_8	Y_{16}	Y_{24}	···	Y_{224}	Y_{232}	Y_{240}
L	H	Input	Output	DI_0	Y_{240}	Y_{232}	Y_{224}	···	Y_{24}	Y_{16}	Y_8
				DI_1	Y_{239}	Y_{231}	Y_{223}	···	Y_{23}	Y_{15}	Y_7
				DI_2	Y_{238}	Y_{230}	Y_{222}	···	Y_{22}	Y_{14}	Y_6
				DI_3	Y_{237}	Y_{229}	Y_{221}	···	Y_{21}	Y_{13}	Y_5
				DI_4	Y_{236}	Y_{228}	Y_{220}	···	Y_{20}	Y_{12}	Y_4
				DI_5	Y_{235}	Y_{227}	Y_{219}	···	Y_{19}	Y_{11}	Y_3
				DI_6	Y_{234}	Y_{226}	Y_{218}	···	Y_{18}	Y_{10}	Y_2
				DI_7	Y_{233}	Y_{225}	Y_{217}	···	Y_{17}	Y_9	Y_1

(Common Mode)

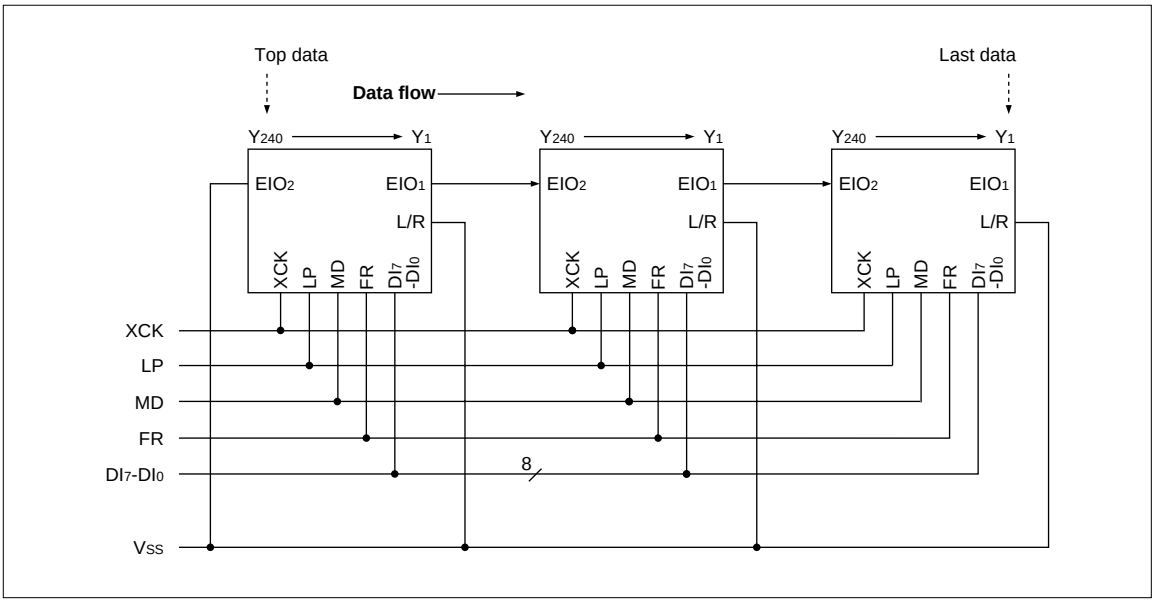
MD	L/R	DATA TRANSFER DIRECTION	EIO_1	EIO_2	DI_7
L (Single)	L	$Y_{240} \rightarrow Y_1$	Output	Input	X
	H	$Y_1 \rightarrow Y_{240}$	Input	Output	X
H (Dual)	L	$Y_{240} \rightarrow Y_{121}$ $Y_{120} \rightarrow Y_1$	Output	Input	Input
	H	$Y_1 \rightarrow Y_{120}$ $Y_{121} \rightarrow Y_{240}$	Input	Output	Input

NOTES :

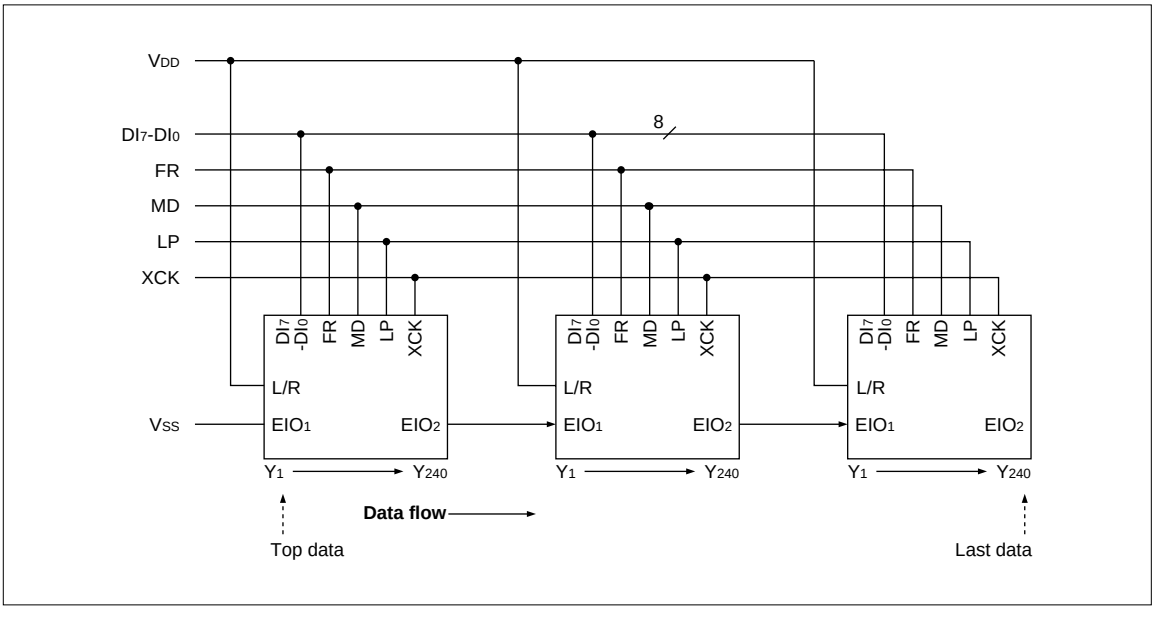
- L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

CONNECTION EXAMPLES OF PLURAL SEGMENT DRIVERS

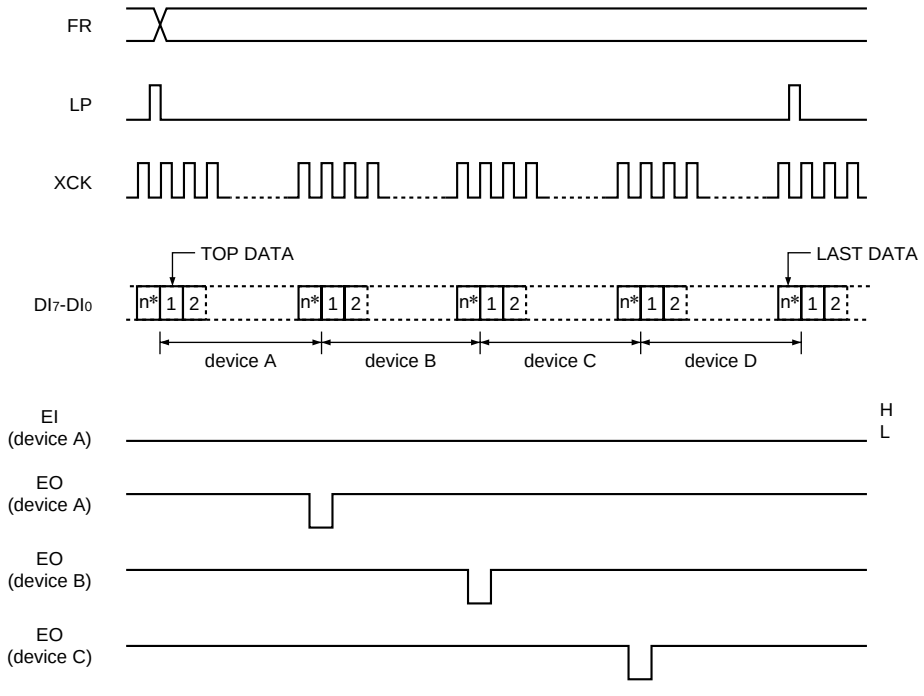
(a) When L/R = "L"



(b) When L/R = "H"



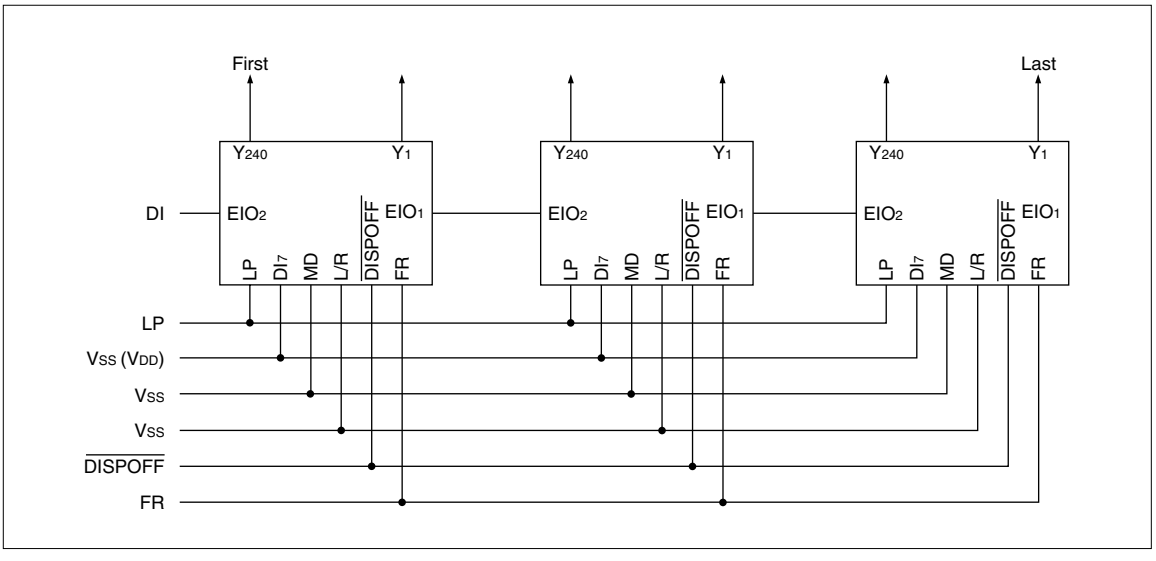
TIMING CHART OF 4-DEVICE CASCADE CONNECTION OF SEGMENT DRIVERS



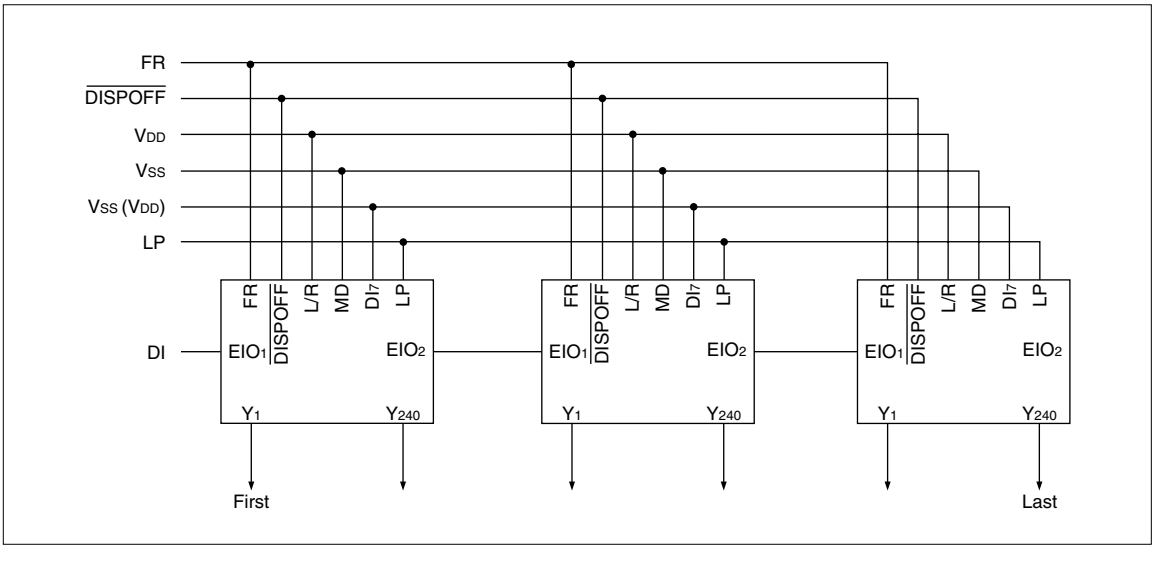
∗ n = 60 in 4-bit parallel input mode.
n = 30 in 8-bit parallel input mode.

CONNECTION EXAMPLES FOR PLURAL COMMON DRIVERS

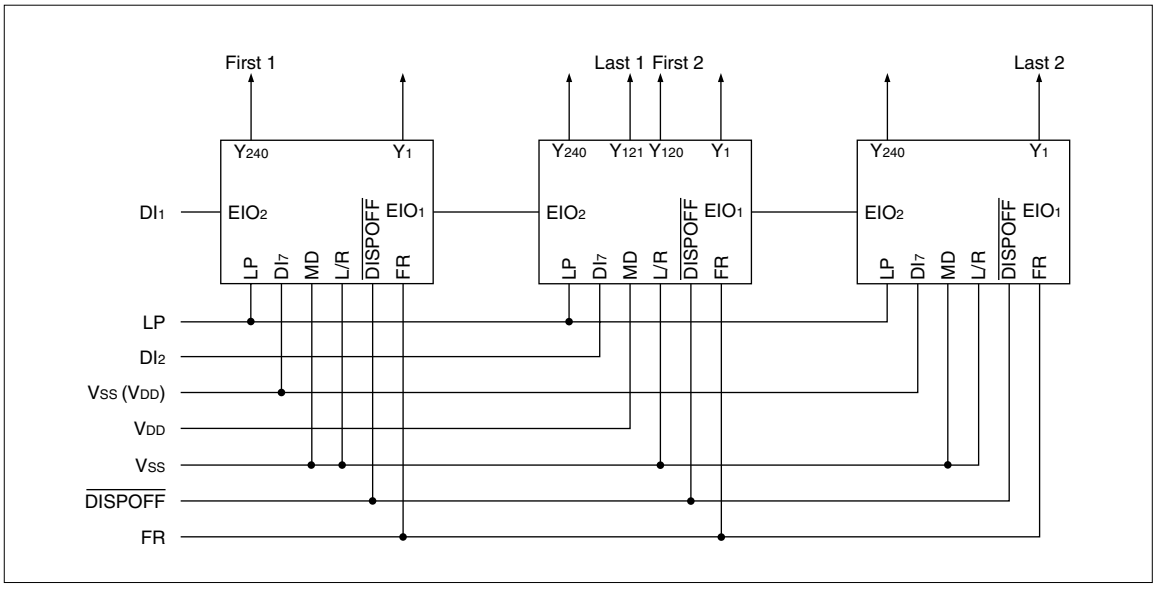
(a) Single Mode (L/R = "L")



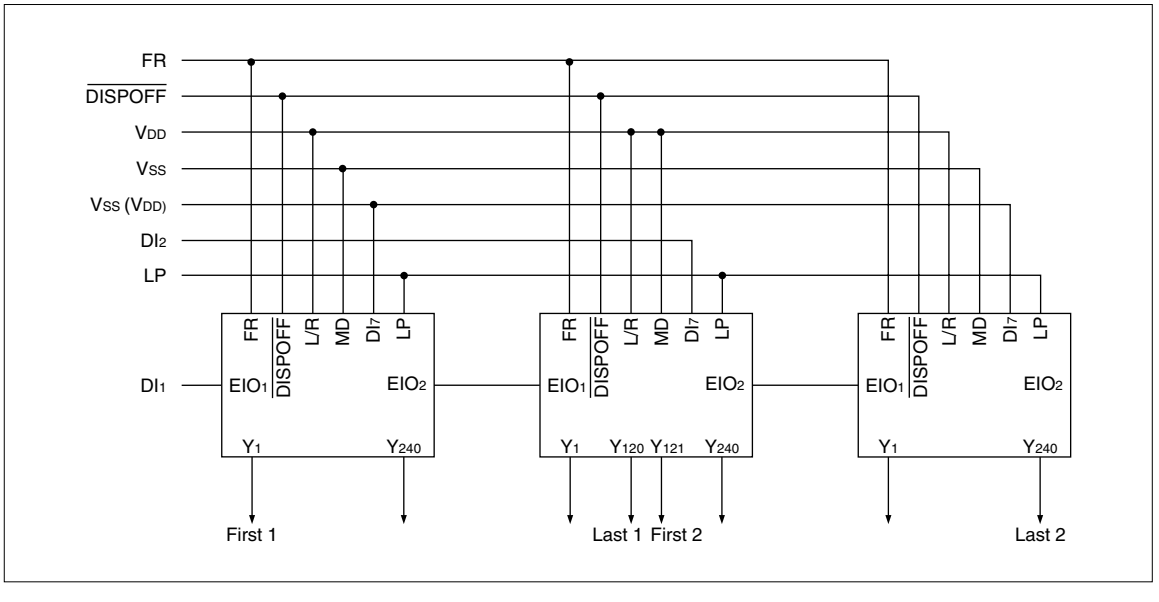
(b) Single Mode (L/R = "H")



(c) Dual Mode (L/R = "L")



(d) Dual Mode (L/R = "H")



PRECAUTIONS

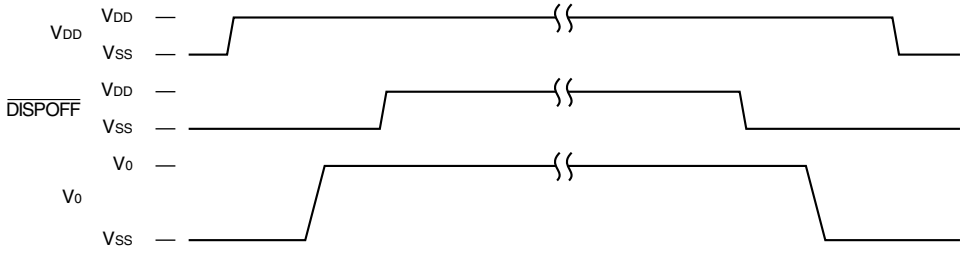
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on $\overline{DISPOFF}$ function. After that, cancel the $\overline{DISPOFF}$ function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_5 on $\overline{DISPOFF}$ function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	−0.3 to +7.0	V	1, 2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	−0.3 to +45.0	V	
	V_{12}	V_{12L}, V_{12R}	−0.3 to V_0 + 0.3	V	
	V_{43}	V_{43L}, V_{43R}	−0.3 to V_0 + 0.3	V	
	V_5	V_{5L}, V_{5R}	−0.3 to V_0 + 0.3	V	
Input voltage	V_I	DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$, $TEST_1$, $TEST_2$	−0.3 to V_{DD} + 0.3	V	
Storage temperature	T_{STG}		−45 to +125	˚C	

NOTES :

1. T_A = +25 ˚C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	+15.0		+42.0	V	
Operating temperature	T_{OPR}		−20		+85	˚C	

NOTES :

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Segment Mode) (V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +15.0 to +42.0 V, T_{OPR} = −20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$			0.2V_{DD}	V	
Input "High" voltage	V_{IH}			0.8V_{DD}			V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = −0.4 mA		V_{DD} − 0.4			V	
Input leakage current	I_{LIL}	V_I = V_{SS}	DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$			−10.0	µA	
	I_{LIH}	V_I = V_{DD}				+10.0	µA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ = 0.5 V, V_0 = 40 V	Y_1-Y_{240}		1.0	1.5	kΩ	
		$\lvert\Delta V_{ON}\rvert$ = 0.5 V, V_0 = 30 V			1.5	2.0		
		$\lvert\Delta V_{ON}\rvert$ = 0.5 V, V_0 = 20 V			2.0	2.5		
Standby current	I_{STB}		V_{SS}			75.0	µA	1
Supply current (1) (Non-selection)	I_{DD1}		V_{DD}			2.0	mA	2
Supply current (2) (Selection)	I_{DD2}		V_{DD}			12.0	mA	3
Supply current (3)	I_0		V_{0L}, V_{0R}			1.5	mA	4

NOTES :

1. V_{DD} = +5.0 V, V_0 = +42.0 V, V_I = V_{SS}.
2. V_{DD} = +5.0 V, V_0 = +42.0 V, f_{XCK} = 20 MHz, no-load, EI = V_{DD}.
   The input data is turned over by data taking clock (4-bit parallel input mode).
3. V_{DD} = +5.0 V, V_0 = +42.0 V, f_{XCK} = 20 MHz, no-load, EI = V_{SS}.
   The input data is turned over by data taking clock (4-bit parallel input mode).
4. V_{DD} = +5.0 V, V_0 = +42.0 V, f_{XCK} = 20 MHz, f_{LP} = 41.6 kHz, f_{FR} = 80 Hz, no-load.
   The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +15.0 to +42.0 V, T_{OPR} = −20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$			0.2V_{DD}	V	
Input "High" voltage	V_{IH}			0.8V_{DD}			V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = −0.4 mA		V_{DD} − 0.4			V	
Input leakage current	I_{LIL}	V_I = V_{SS}	DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$			−10.0	µA	
	I_{LIH}	V_I = V_{DD}	DI_6-DI_0, LP, L/R, FR, MD, S/C, $\overline{DISPOFF}$			+10.0	µA	
Input pull-down current	I_{PD}	V_I = V_{DD}	DI_7, XCK, EIO_1, EIO_2			100.0	µA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ = 0.5 V, V_0 = 40 V	Y_1-Y_{240}		1.0	1.5	kΩ	
		$\lvert\Delta V_{ON}\rvert$ = 0.5 V, V_0 = 30 V			1.5	2.0		
		$\lvert\Delta V_{ON}\rvert$ = 0.5 V, V_0 = 20 V			2.0	2.5		
Standby current	I_{STB}		V_{SS}			75.0	µA	1
Supply current (1)	I_{DD}		V_{DD}			120.0	µA	2
Supply current (2)	I_0		V_{0L}, V_{0R}			240.0	µA	2

NOTES :

1. V_{DD} = +5.0 V, V_0 = +42.0 V, V_I = V_{SS}
2. V_{DD} = +5.0 V, V_0 = +42.0 V, f_{LP} = 41.6 kHz, f_{FR} = 80 Hz, 1/480 duty operation, no-load.

AC Characteristics

(Segment Mode 1) (V_{SS} = V_5 = 0 V, V_{DD} = +5.0±0.5 V, V_0 = +15.0 to +42.0 V, T_{OPR} = –20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R, $t_F \leq$ 10 ns	50			ns	1
Shift clock "H" pulse width	t_{WCKH}		15			ns	
Shift clock "L" pulse width	t_{WCKL}		15			ns	
Data setup time	t_{DS}		10			ns	
Data hold time	t_{DH}		12			ns	
Latch pulse "H" pulse width	t_{WLPH}		15			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		30			ns	
Latch pulse rise to shift clock rise time	t_{LS}		25			ns	
Latch pulse fall to shift clock fall time	t_{LH}		25			ns	
Enable setup time	t_S		10			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns	
$\overline{\text{DISPOFF}}$ "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	C_L = 15 pF			30	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	C_L = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	C_L = 15 pF			1.2	µs	

NOTES :

1. Takes the cascade connection into consideration.
2. (t_{WCK} – t_{WCKH} – t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2) (V_{SS} = V_5 = 0 V, V_{DD} = +3.0 to +4.5 V, V_0 = +15.0 to +42.0 V, T_{OPR} = –20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R, $t_F \leq$ 10 ns	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns	
$\overline{\text{DISPOFF}}$ "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	C_L = 15 pF			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	C_L = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	C_L = 15 pF			1.2	µs	

NOTES :

1. Takes the cascade connection into consideration.
2. (t_{WCK} – t_{WCKH} – t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 3) (V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +3.0 V, V_0 = +15.0 to +42.0 V, T_{OPR} = −20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R, $t_F \leq$ 10 ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		65			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns	
$\overline{\text{DISPOFF}}$ "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	C_L = 15 pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	C_L = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	C_L = 15 pF			1.2	µs	

NOTES :

1. Takes the cascade connection into consideration.
2. (t_{WCK} − t_{WCKH} − t_{WCKL})/2 is maximum in the case of high speed operation.

Timing Chart of Segment Mode

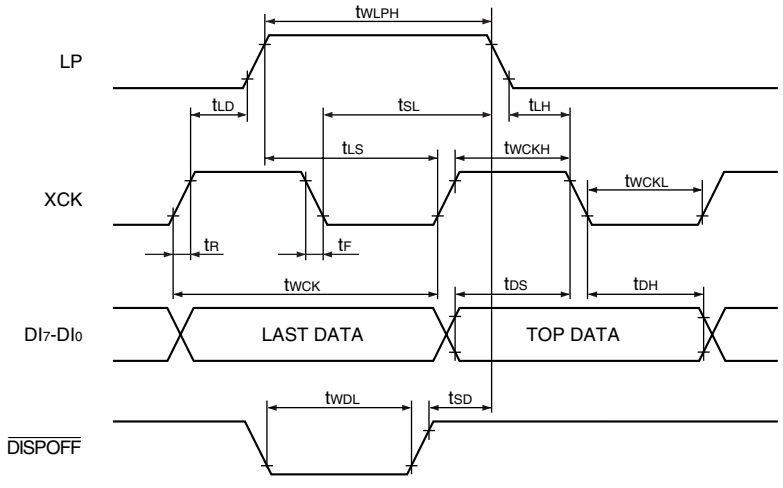
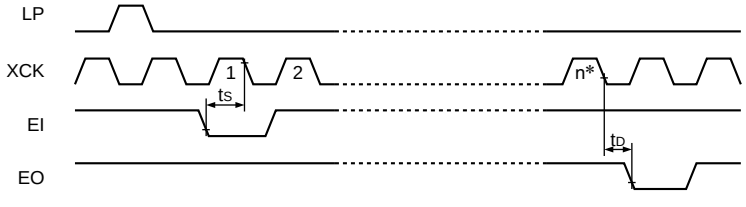


Fig. 6 Timing Characteristics (1)



* n = 60 in 4-bit parallel input mode.
n = 30 in 8-bit parallel input mode.

Fig. 7 Timing Characteristics (2)

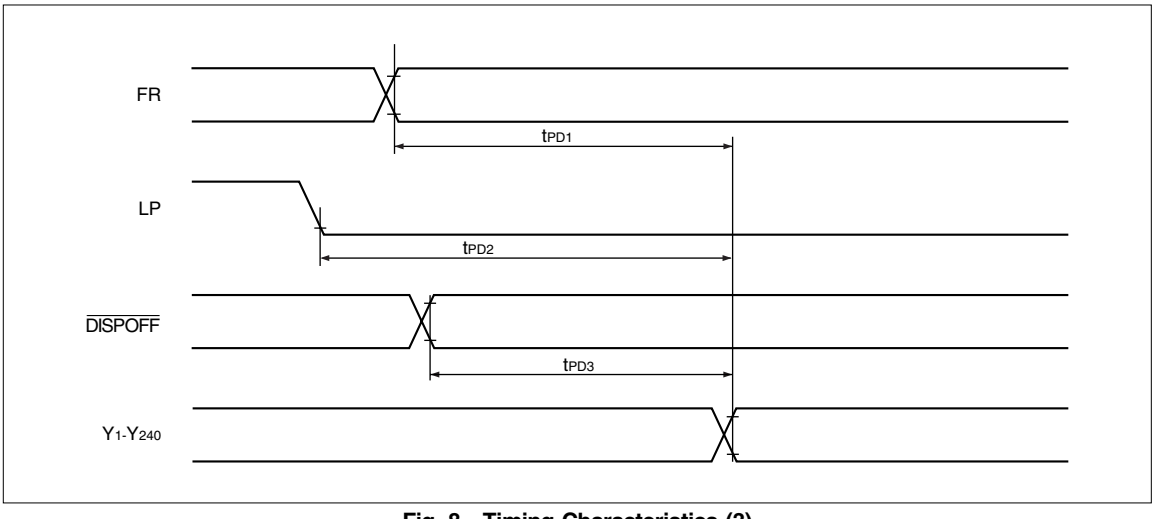
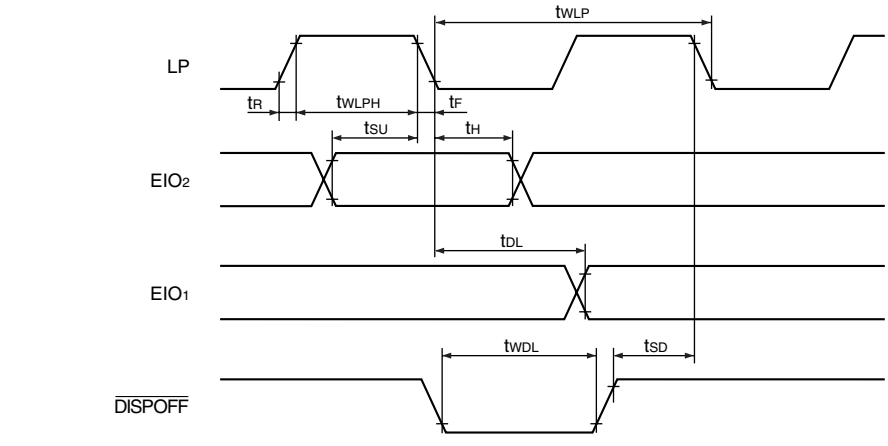


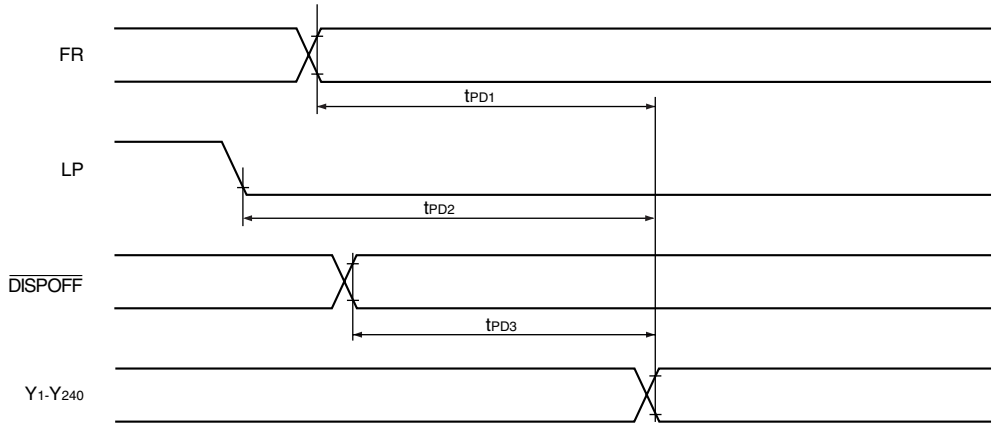
Fig. 8 Timing Characteristics (3)

(Common Mode) (V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +15.0 to +42.0 V, T_{OPR} = −20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	t_R, t_F ≤ 20 ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD} = +5.0±0.5 V	15			ns
		V_{DD} = +2.5 to +4.5 V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
$\overline{DISPOFF}$ removal time	t_{SD}		100			ns
$\overline{DISPOFF}$ "L" pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_{DL}	C_L = 15 pF			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	C_L = 15 pF			1.2	µs
Output delay time (3)	t_{PD3}	C_L = 15 pF			1.2	µs

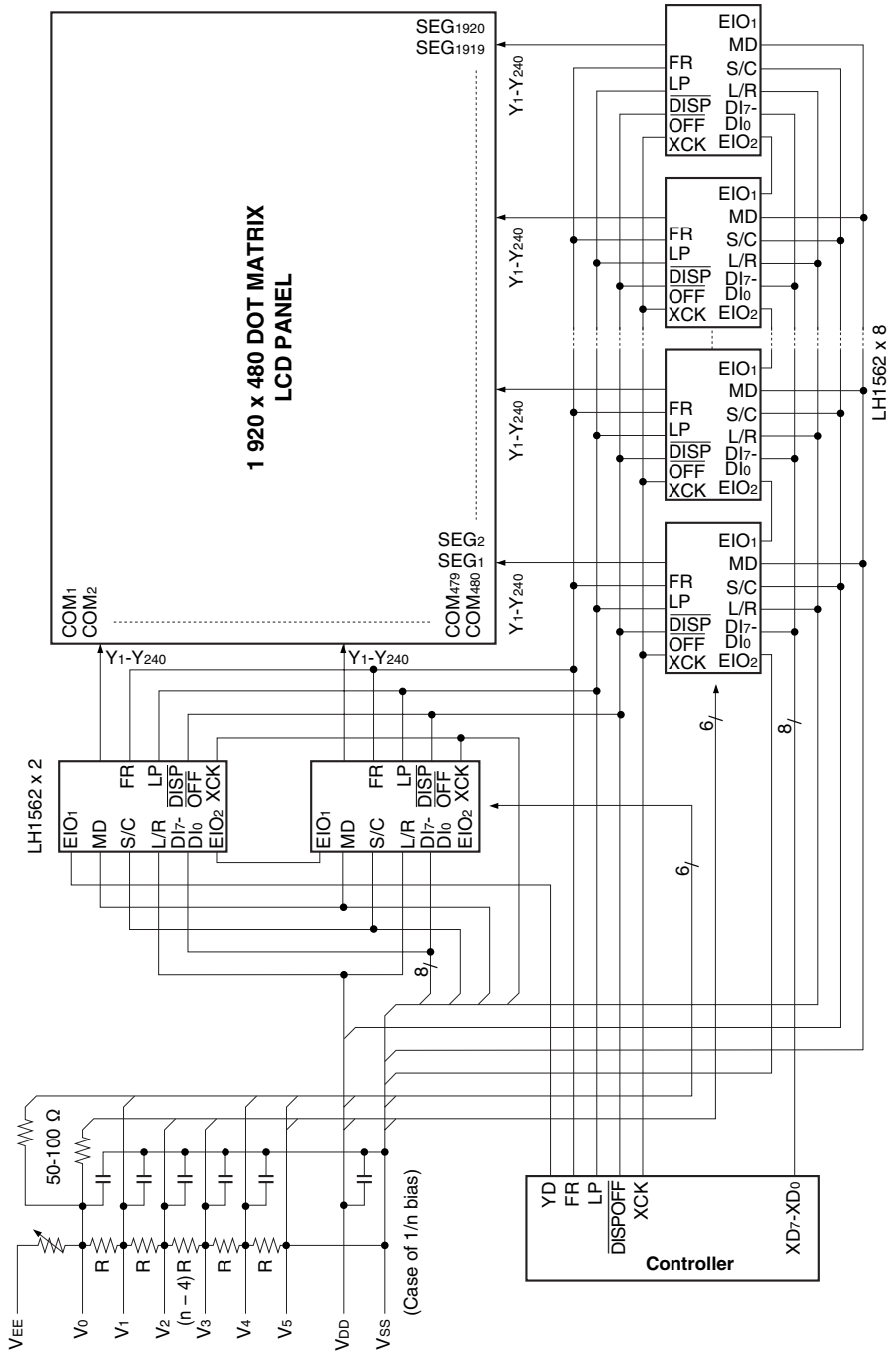
Timing Chart of Common Mode





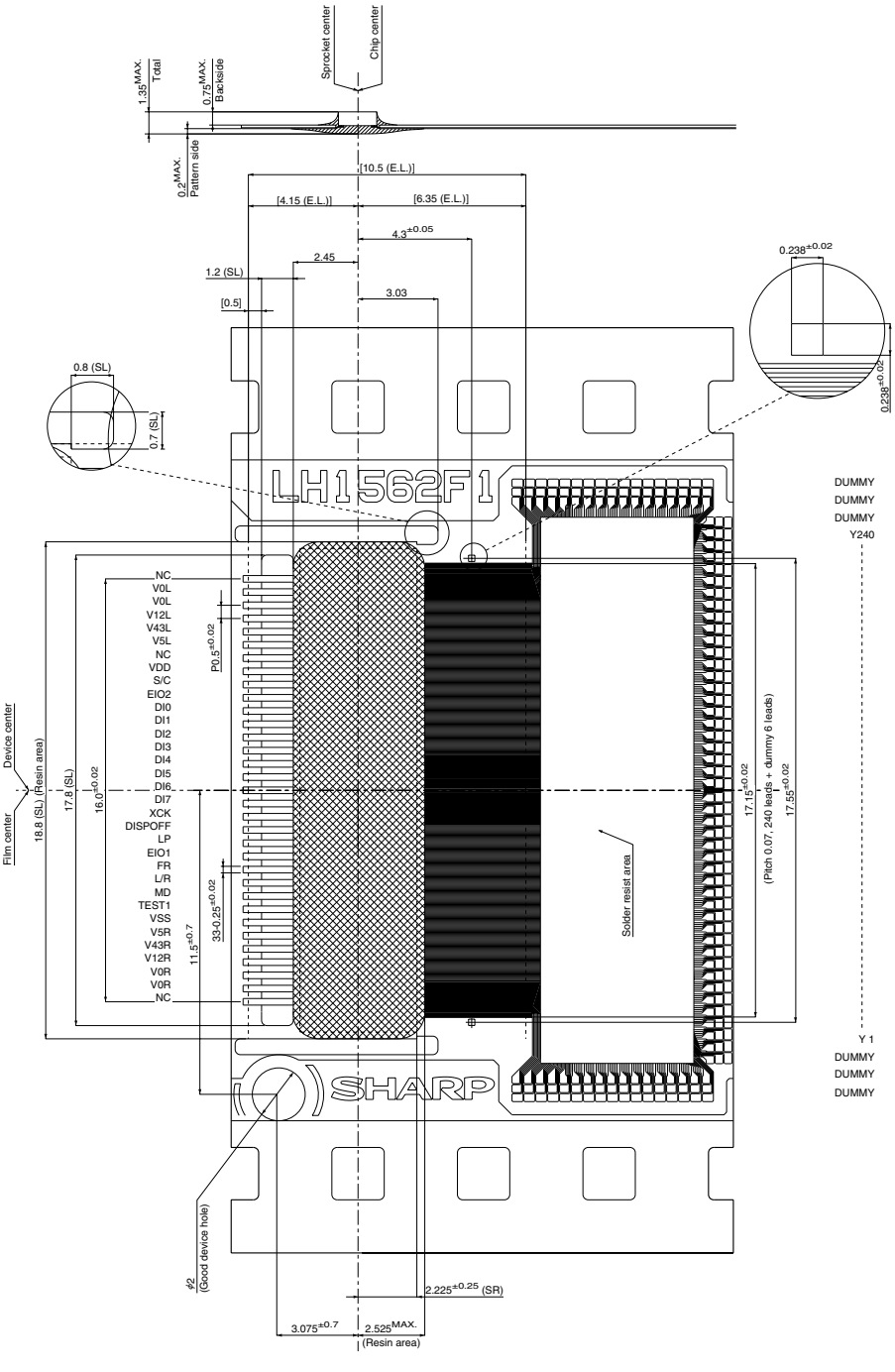
[L/R = "L"]

SYSTEM CONFIGURATION EXAMPLE



PACKAGES

(Unit : mm)



● Tape Material

Substrate	UPILEX S75
Adhesive	#7100
Cu foil [thickness]	SLP 18 µm
Solder resist	Epoxy resin

● Tape Specification

Tape width	35 mm
Tape type	Wide
Perforation pitch	3 pitches

LH1562F1

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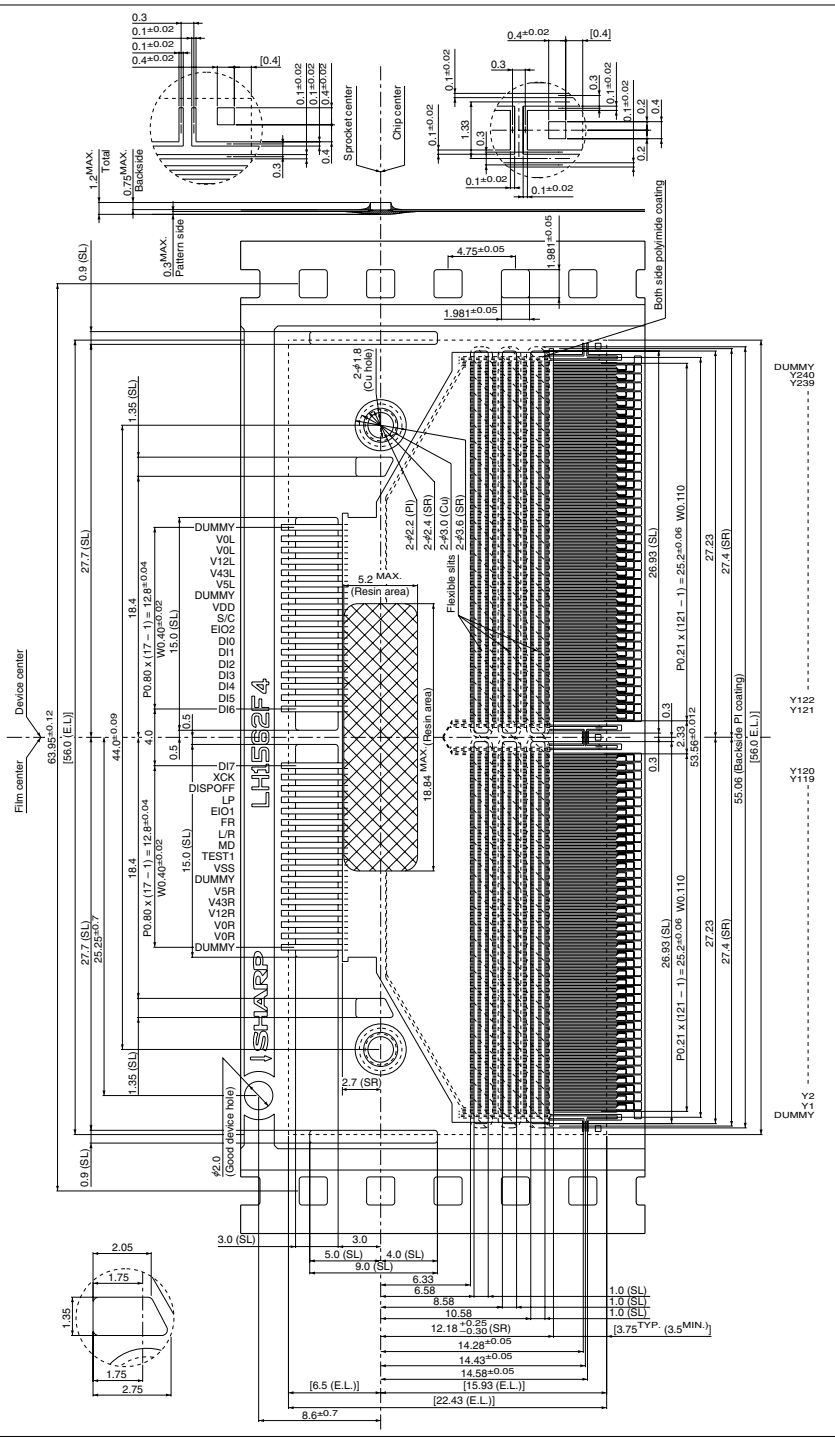
LH1562F4



● Tape Material

Substrate	UPILEX S75
Adhesive	#7100
Cu foil [thickness]	USLP 18 µm
Solder resist	Polyimide SSF

● Tape Specification

Tape width	70 mm
Tape type	Wide
Perforation pitch	6 pitches