Product Brief

MC9328MX21P/D
Rev. 0, 9/2003

MC9328MX21
i.MX21 Application Processor

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Contents

Motorola's i.MX family of microprocessors has demonstrated leadership in the portable handheld market Building on the success of the MX (Media Extensions) series, the i.MX21 (MC9328MX21) provides a leap in performance with an ARM926EJ-S™ microprocessor core that provides native security and accelerated Java support in addition to highly integrated system functions. i.MX products specifically address the needs of the smartphone and portable product markets with their intelligent integrated peripherals, advanced processor core, and power management capabilities.

The i.MX21 features the advanced and power-efficient ARM926EJ-S core operating at speeds up to 400 MHz and is part of a growing family of *Smart Speed* products that offer high peformance processing optimized for lowest power consumption. On-chip modules such as a video accelerator module, LCD controller, USB On-The-Go, CMOS sensor interface, and two sychronous serial interfaces with AC97 host controller offer designers a rich suite of peripherals that can enhance any product seeking to provide a rich multimedia experience. In addition, the i.MX21 provides hardware enabled security features including high assurance boot mode, unique processor IDs, secret key support, secure RAM, and a security monitor. These features enable secure e-commerce, digital rights management (DRM), information encryption, and secure software downloads.

For cost sensitive applications, the NAND Flash controller allows the use of low-cost NAND Flash devices to be used as primary or secondary non-volatile storage. The on-chip error correction code (ECC) and parity checking circuitry of the NAND Flash controller frees the CPU for other tasks. WLAN, Bluetooth and expansion options are provided through PCMCIA/CF, USB, and MMC/SD host controllers.

The i.MX21 is packaged in a 289-pin MAPBGA.

1 Key Features

A summary of the main features of i.MX21:

- High level of on-chip integration
- Very low-power system design without compromised performance
- Optimized for multimedia applications
- Optimized for secure content delivery and M-commerce transactions
- Internal Security systems to prevent unauthorized access
- Dedicated bus master interface to external chips including graphics accelerators

ARM POWERED®

- Supports a wide variety of 16- and 32-bit memory types
- Includes a Smart LCD and standard LCD controller for optimum configuration flexiability
- Provides support for industry standard peripherals such as USBOTG, MMC/SD, PCMCIA/CF and Fast Infrared (Fast IR)
- Integrated camera interface

2 i.MX21 Block Diagram

Figure 1 is a simplified functional block diagram of i.MX21.

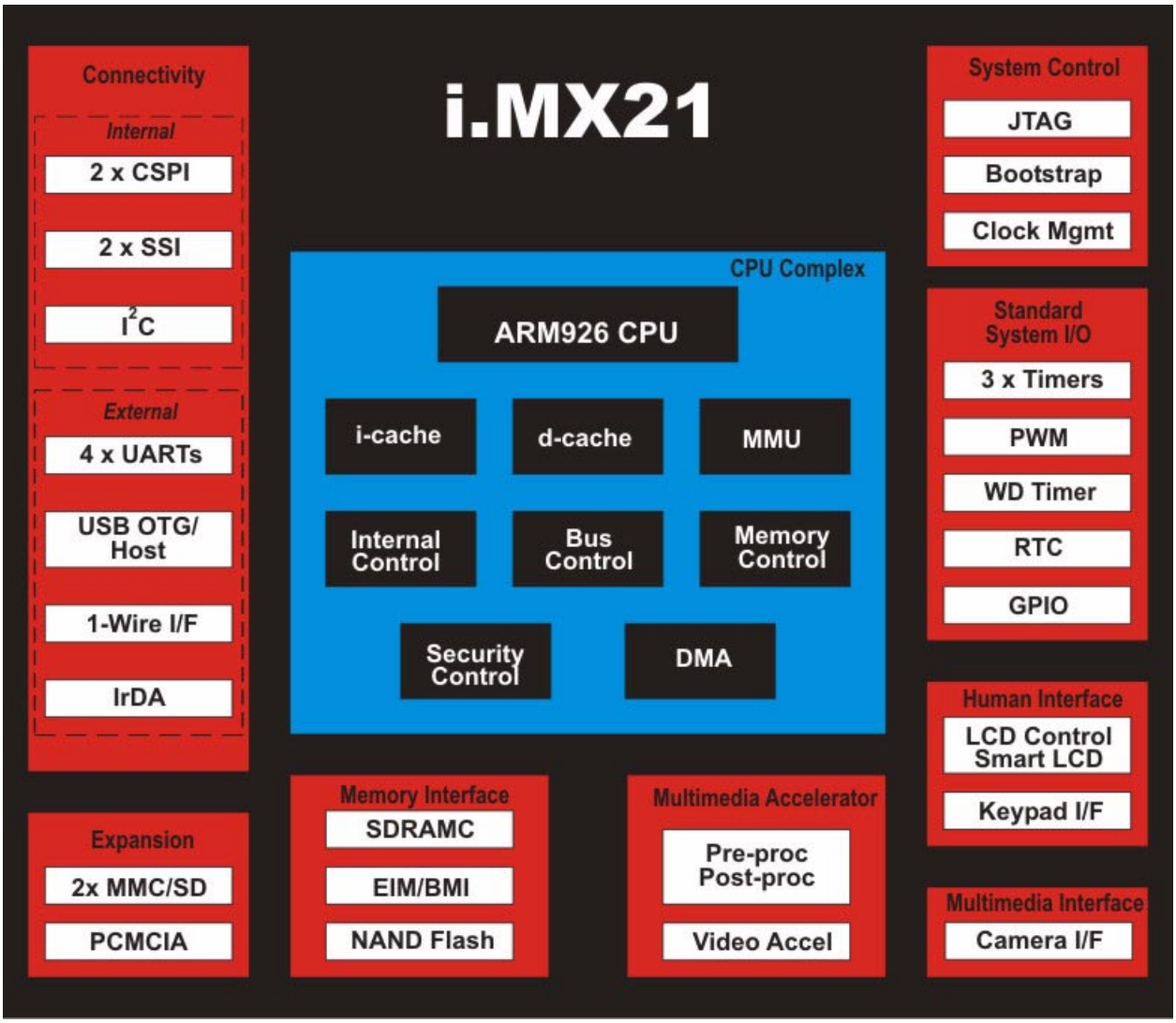

Figure 1. i.MX21 Functional Block Diagram

3 i.MX21 Features

The i.MX21 boasts a robust array of features that can support a wide variety of applications. Below is a brief description of i.MX21 features.

3.1 ARM926EJ-S™ Core Complex

The ARM926EJ-S Core Complex consists of the ARM926EJ-S processor, a 6 × 4 Multi-Layer AHB crossbar switch, and a "primary AHB" complex.

- ARM926EJ-S core: 266 MHz, with speeds up to 400 MHz
  - 16K instruction cache and 16K data cache
  - High-performance ARM® 32-bit RISC engine
  - Thumb® 16-bit compressed instruction set for a leading level of code density
  - Efficient execution of Java byte codes
  - EmbeddedICE™ JTAG software debug
  - 100-percent user code binary compatibility with ARM7TDMI™
  - Advanced Microcontroller Bus Architecture (AMBA™) system-on-chip multi-master bus interface
  - Support for mixed loads of real-time and user applications via cache locking facilities
  - Virtual Memory Management Unit (VMMU)
- AHB to IP bus interfaces (AIPIs)
  - Provide a communication interface between the high-speed AHB to a lower-speed IP bus for slave peripherals
- The Multi-Layer 6 × 4 AHB Crossbar Switch
  - The crossbar switch allows for concurrent transactions to proceed from any input port (bus master) to any output port (bus slave). That is, it is possible for all four output ports to be active at the same time as a result of four independent input or output requests.
- ARM Interrupt Controller (AITC)
  - The AITC is connected to the primary AHB as a slave device and provides support for up to 64 interrupt sources. It generates normal and fast interrupts to the processor core. The AITC supports a hardware assisted vectoring mode for automatic vectoring to reduce interrupt latency.
- Security sub-system
  - Authentication mechanism ensures an authorized and un-modified program/data load, making the Flash ROM (OS) into tamper-evident memory. Using anti-cloning to protect against unauthorized downloads as well as viruses.
  - Availablity of embedded non-readable secret key, unique silicon ID and key management hardware unit (Key Encryption Module and Secure RAM), provides the i.MX21 with a Strong Key Management solution for OS security.
  - The combination of above can achieve a system of high-level of trust and data integrity to support a wide-range of mobile real-time financial and content transactions over the internet and VPNs.
  - The Security Controller, Secure RAM, Security Monitor, and a High Assurance Boot (HAB) process work together to ensure a High Grade and High Trust system suitable for M-Commerce.

applications, network based authentication, authorization and access control, digital signing and digital rights management.

- CPU and System speed:
  - ARM926EJ-S core: typical operation at 266 MHz up to 400 MHz
  - System Clock: up to 133 MHz
  - External memory interface: same clock source as system, up to 133 MHz at 1.8V supply
  - System clock is derived from the CPU clock through an integer divider

3.2 enhanced Multimedia Accelerator (eMMA)

i.MX21 comes with an enhanced Multimedia Accelerator (eMMA) comprising an ISO/IEC 14496-2 compliant MPEG-4 Encoder and Decoder and independent Pre-processing and Post-processing stages which provide exceptional image and video quality. The eMMA represents a major breakthrough to solve the problem of high MIPS requirement for video encode and decode operations in mobile and wireless applications. Tight integration and memory pipelining coupled with AHB master mode operation ensures minimal system loading. To further offload the CPU, live video stream data enters the eMMA module directly through an internal private data interface. The eMMA architecture is shown in Figure 2.

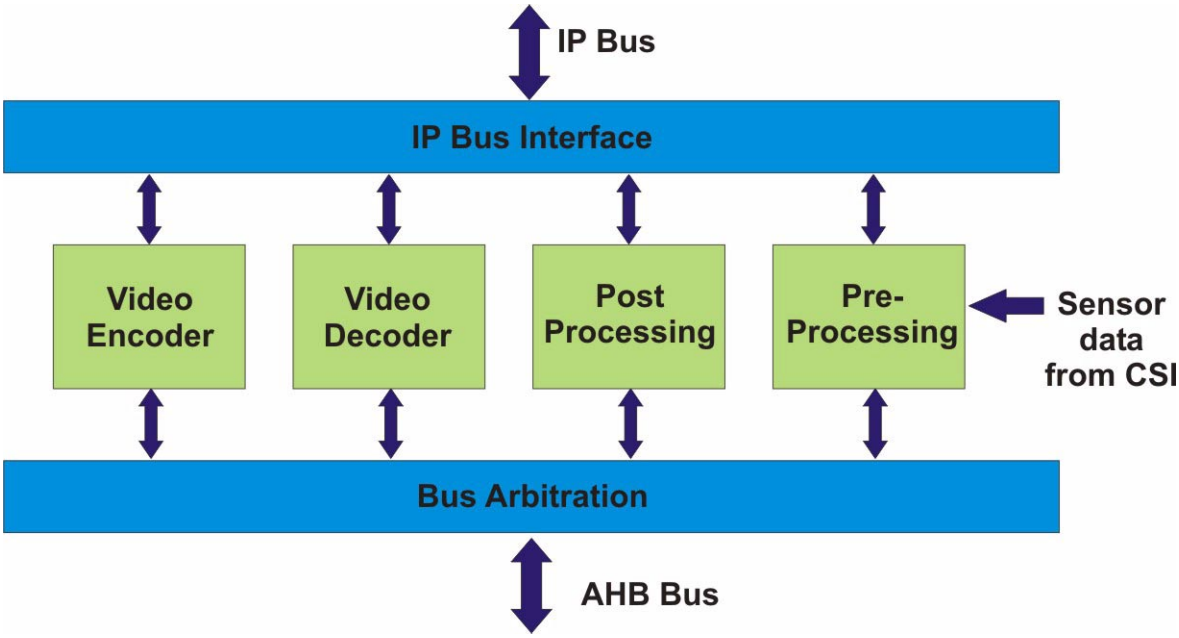

Figure 2. eMMA Architecture

3.2.1 Video Encoder

- Supports MPEG4 and H.263 (Short Video Header) formats
- Fully conforms to ISO/IEC 14496-2 Visual Simple Profiles Levels 0 to 3
- Supports real-time encoding images of sizes from 32 × 32 up to CIF or QVGA at 30 fps
- Input data format is YUV 4:2:0 (Planar)
- Supports camera stabilization

3.2.2 Video Decoder

- Supports MPEG4 and H.263 (Short Video Header) formats
- Fully conforms to ISO/IEC 14496-2 Visual Simple Profile Levels 0 to 3
- Supports real-time decoding of image sizes up to CIF or QVGA at 30 fps
- Output data format is YUV 4:2:0 (Planar)

3.2.3 PostProcessor (PP)

The PostProcessor, shown in Figure 3, performs deblock, dering, image resize and color space conversion (CSC) functions on the input image data. These functions provide flexibility to meet various RGB formats and YUV formats for display. Besides working in tandem with the Decoder sub-block in the eMMA, the Postprocessor can also be used by software decoders (other than MPEG4) to touch up the final output before display. The sub-blocks that perform deblock, dering, resize and CSC operations can be selectively bypassed through software configuration. Figure 3 shows the flow for video postprocessing.

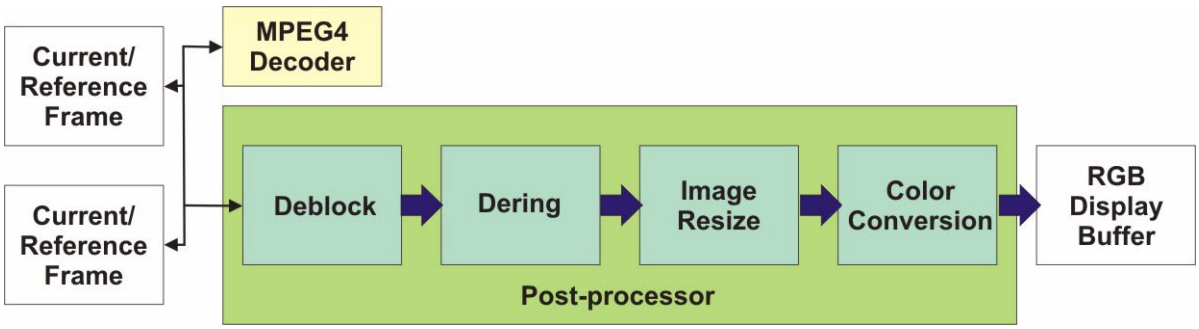

Figure 3. PostProcessor

Postprocessor features:

- Input data:
  - From system memory
- Input format:
  - YUV 4:2:0 (Planar)
- Output format:
  - YUV422
  - RGB444
  - RGB565
  - RGB666
  - RGB888 (unpacked)
- Input Size: Maximum size of 2044 × 2044
- Image Resize:
  - Upscaling ratios ranging from 1:1 to 1:4 in fractional steps
  - Downscaling ratios ranging from 1:1 to 2:1 in fractional steps and a fixed 4:1
  - Ratios provide scaling between QCIF, CIF, QVGA (320 × 240), and QVGA (240 × 320)

3.2.4 Image Pre-Processor (PrP)

The image pre-processor block performs color space conversion and image resizing for a viewfinder display. In addition, it performs data formatting for the video encoder and for still images which can be fed to a hardware or software based video encoder or image compressor. It also provides data formatting for video encoder and still image for input to either a hardware or software based video encoder or image compressor. The Pre-processor has two media inputs and output paths and can accept input from system memory or from a dedicated data bus connected to CMOS Sensor Interface (CSI) module. The Pre-processor can provide frame rate control of the live video stream from the CSI module to adjust for different processing load conditions. The Pre-processor's two output channels output RGB data for display of local camera view and image data for compression by the hardware encoder or a software encoder (still image or video encode).

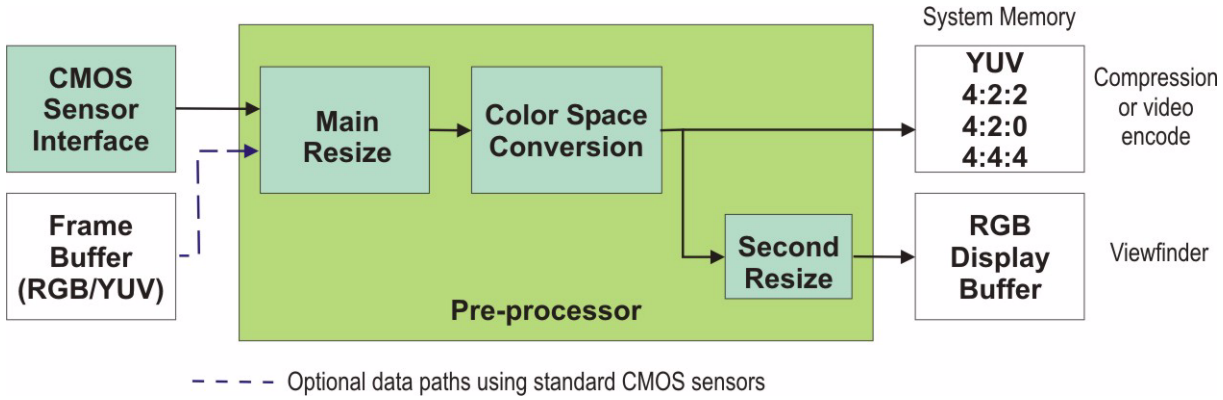

Figure 4. Pre-Processor Data Flow

Pre-processor features:

- Data input:
  - System memory
  - Private DMA between CMOS Sensor Interface module and pre-processor
- Data input formats:
  - Arbitrarily unpacked RGB input
  - YUV 4:2:2 (Interleaved)
  - YUV 4:2:0 (Planar)
- Input image size: 2044 × 2044
- Image scaling:
  - Main resize ratio: 8:1–1:1 in integral steps, Horizontal 9:8/vertical 6:5 and Horizontal 9:8/ Vertical 1:1
  - Secondary resize ratio for viewfinder: 8:1–1:1 in integral steps
- Output data format:
  - RGB565
  - YUV 4:2:2 (Interleaved)
  - YUV 4:2:0 (Planar)
- RGB data and one YUV data format can be generated concurrently

3.3 Security System

Optimized for secure mobile communications and transactions, the i.MX21 addresses consumers' concerns about M-commerce, carriers' concerns with cloning, configuration protection and theft of services, and content providers' concerns regarding digital rights management. The i.MX21 includes a security framework comprising of both hardware and software elements that enable the fundamental cryptographic blocks required for a wide range of security services and applications. Specific security system elements enabled in the i.MX21 include a high assurance boot, a security controller, hash accelerator, and memory management.

The high assurance boot comprises three elements including Public Key Infrastructure, a hash function and a component that enables the digital signature calculation. The high assurance boot permits the flashed code to be verified for integrity before being loaded by the mobile device.

The SHA-1 hash accelerator is employed to provide a hash or message digest for large memory spaces. In addition it supports the digital signature process required for authentication and non-repudiation.

The security control module includes a secure RAM module and security monitor. The secure RAM module has a number of elements, primarily a 168-bit secret key and triple DES encryption, used to prepare sensitive data (passwords, credit card numbers) for storage in on-chip RAM or off-chip non-volatile memory. On-chip data is stored in RAM that can be cleared to prevent unauthorized access and off-chip data is stored in encrypted form using a secure encryption key. In addition, it provides temporary on-chip storage of decrypted results for real time use.

The security monitor comprises system monitor functions and security support tasks used to ensure secure modes are established and maintained in the processor. The security monitor detects any transactions from a secure to unsecure state. It also initiates the clearing of the secure RAM when any such transactions are detected.

With these fundamental security system building blocks a number of security services and applications are enabled. These cryptographic building blocks employed in the i.MX21 lay the foundation that supports the complete gambit of security services and applications ranging from low value transactions, the protection of intellectual property (DRM), and secure high value transactions required by enterprises worldwide.

Motorola has taken advantage of its long history of providing secure solutions to government agencies and customers to create a security system in hardware and software that provides the peace of mind necessary for our expanding wireless world.

3.4 Display and Video Modules

There are two separate LCD controllers in i.MX21, called the LCDC and SLCDC to support both standard and smart LCD panels. A standard LCD panel has no built-in memory and requires an external controller to send display data at a fixed rate. Such panels typically support high refresh rates suitable for graphics, games and video applications. The LCD controller in i.MX21 is an AHB master and can transfer display data from system memory (SDRAM).

Smart panels have built-in memory and a display controller. An advantage of the built-in memory and controller, is that the refresh function is done by the local LCD controller and only data that is changing has to be updated thus offering a reduced transfer rate and lower power operation.

Both LCD controllers in i.MX21 provide glueless connection to external gray-scale or color LCD panels.

The video input port in i.MX21 supports a direct interface to commonly available CMOS sensors. Together with other system resources (DMA and hardware Pre-processor), viewfinder functions can be achieved with extremely low CPU MIPS and low system power consumption.

3.4.1 LCD Controller (LCDC)

The LCDC features include the following:

- Software programmable screen size (up to 800 × 600) to support single (non-split) monochrome, color STN panels, and color TFT panels
- Support color depth for CSTN panels: 4- or 8-bit mapping from 256 × 18 table, 12-bit true color
- Support color depth for TFT panels: 4- or 8-bit mapping from 256 × 18 table, 16-bit/18-bit/24-bit true color
- Up to 16 gray levels out of 16 palettes
- Capable of directly driving popular LCD displays from manufacturers including Sharp, Hitachi, and Toshiba
- Support for data bus width of 16-bit or 18-bit TFT panels
- Support for data bus width of 8-bit, 4-bit, 2-bit, and 1-bit monochrome LCD panels
- Direct interface to Sharp® 320 × 240 and 240 × 320 HR-TFT panels and other generic panels
- Support for logical operation between color hardware cursor and background
- LCD contrast control using 8-bit PWM
- Support for self-refresh LCD modules
- Hardware panning (soft horizontal scrolling)
- Windowing support for one graphic or text overlay

3.4.2 Smart LCD Controller (SLCDC)

The SLCDC transparently and efficiently transfers image data from system memory to the LCD controller on the smart display. The SLCDC module contains a DMA controller that transfers image and control data from system memory to the SLCDC FIFO where it is formatted and sent out to the LCD controller on the smart LCD display.

The SLCDC can be configured to write image data to the LCD controller via a 4-line serial, 3-line serial, an 8- or 16-bit parallel interface. The SLCDC has two FIFOs into which command and display data are loaded via DMA. The display data is tagged with commands that are used by the SLCDC to communicate display information and data to the Smart LCD panel.

The command tagged data format of the SLCDC provides flexibility and ease of connection to existing and new smart LCD panels.

3.4.3 CMOS Sensor Interface (CSI)

The CSI features include the following:

- Configurable interface supports wide variety of popular CMOS sensors that output data in YUV, RGB, or Bayer format
- Supports CCIR656 format
- Statistic data generation for Auto Exposure and Auto White Balance control which is required for Bayer data
- DMA support for image data transfer
- Private data bus to eMMA Pre-processor module for video and image preprocessing

3.5 Bus Master Interface (BMI)

The i.MX21 includes a bus master interface to reduce the overhead to external multi-media coprocessors such as those from ATI Technology, Inc. This improvement elevates overall systems performance for video and graphics intensive application such as 3D gaming.

- Supports 8- or 16-bit data bus mode
- Supports external bus master read or write to CPU using memory access timing
- Supports CPU write to external bus slave using memory access timing
- Supports ATI graphic chip burst read/write accesses timing
- High communication speed
- Supports DMA

3.6 Wireless Connectivity

3.6.1 Fast Infra-Red Interface (Fast IR)

The Infrared Interface in i.MX21 implements both the Medium Infra-Red (MedIR) and Fast Infra-Red (Fast IR) protocols. In MedIR mode, the Fast IR interface supports wireless communications at 0.576 Mbps and 1.152 Mbps and uses a framed transmission protocol which follows the High-Level Data Link Controller (HDLC) protocol. In Fast IR mode, the module operates at 4 Mbps with 4 Pulse Position Modulation (4PPM) defined by *Serial Infrared Physical Layer Link Specification v1.4(IrPHY)*.

In addition to the MIR and Fast IR modes, the i.MX21 supports SIR protocol on all 4 of the UART modules. Only UART1 may be used together with the Fast IR interface as these two modules share their pins for transparent speed and protocol stepping from SlowIR to MedIR or SlowIR to Fast IR modes.

Figure 5 shows the Fast IR pins that are shared with the UART module. The pin selection is controlled via GPIO configuration.

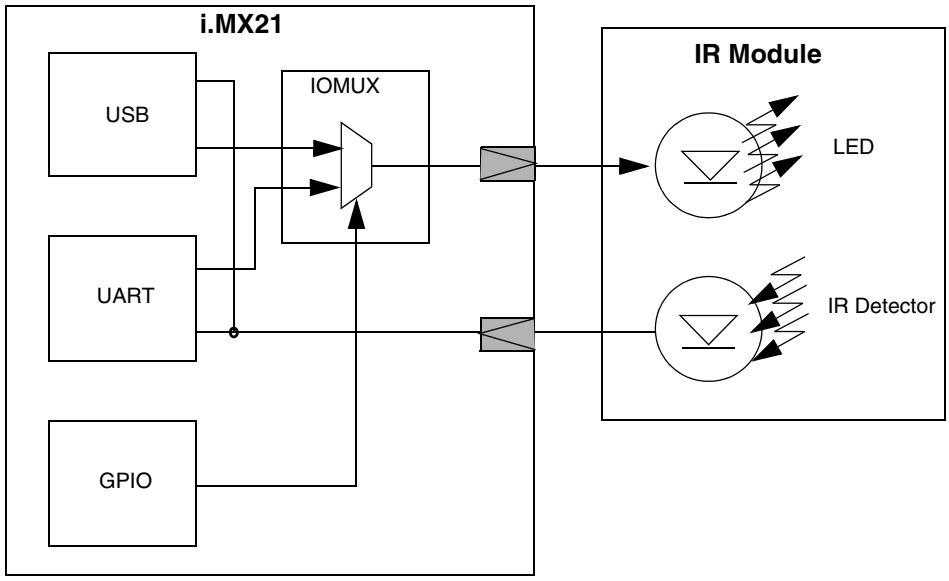

Figure 5. Fast Infra-Red Interface

3.7 Wired Connectivity

There are multiple peripheral modules in i.MX21 providing both external and on-board connection capability. All peripherals that have FIFOs also support DMA transfers to and from the FIFOs. This minimizes CPU intervention and reduces interrupt overhead to the system. The exception to this is the Pulse Width Modulator which has FIFOs but does not support DMA.

3.7.1 USB On-The-Go (USBOTG) Controller

The USB controller in i.MX21 implements the USB On-The-Go (OTG) specification. The USBOTG module is complaint to the *USB 2.0 Specification*, and operates at full and low speeds as specified in the USB 2.0 specification. The OTG port is capable of connecting to a USB host or client device and uses the Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) to switch between Host and Function roles. One of the dual host ports can be used for connection to a smartphone USB client device and the other host port is available for connection to other client devices. The connection to the smartphone forms an interprocessor link as an alternate to a UART-based link.

Built-in switching logic implements a bypass mode in which the internal host port is bypassed to allow an external USB host and the smartphone USB client to be directly connected. This feature enables the external USB host to directly control the smartphone modem for debug or for production programming. Figure 6 shows the USBOTG block diagram.

The USBOTG module operates as a bus master taking ownership of the bus for DMA transfers allowing the USBOTG to continue operation even while the CPU is in a low-power mode.

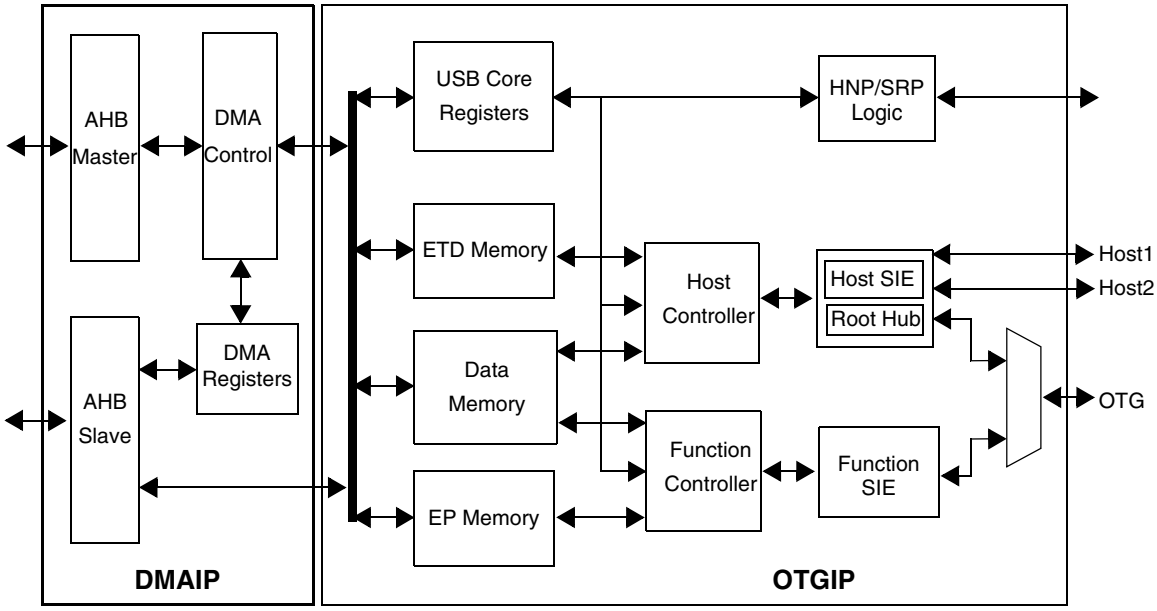

Figure 6. USB On-The-Go Controller

The USB On-the-Go module has the following features:

- Compliant with the USB 2.0 specification for operation at full speed (12 Mbps) and low speed (1.5 Mbps)
- Fully compliant with the USB On-The-Go specification
- Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) implemented in hardware and can also be controlled by software
- Transaction scheduling and transfer level protocol implemented in hardware including

bandwidth management, data toggle and retry

— AMBA AHB 2.0 Bus Master DMA Controller:
  – 32 DMA Channels for Host Controller EndPoint Transfer Descriptors
  – 32 DMA Channels for Function Controller EndPoint Descriptors
— USB function supports 32 physical endpoints:
  – 16 IN endpoints and 16 OUT endpoints
  – Programmable for type (control, interrupt, bulk, isochronous), packet size, and buffering
— Double buffering support for all four types of host and function controller transactions
— Separate descriptor and data memory space
— Direct device to device transfers in one frame
— Power savings mode for Host Controller and suspend mode for Function Controller
— All USB host ports support external transceiver bypass mode

3.7.2 Four Universal Asynchronous Receiver/Transmitters (UART1, UART2, UART3, and UART4)

— Supports serial data transmit/receive operation: 7 or 8 data bits, 1 or 2 stop bits, programmable parity (even, odd, or none)
— Programmable baud rates up to 1.875 MHz
— Automatic baud rate detection
— 32-bytes FIFO for transmit and 32 half-words FIFO for receive data
— IrDA Serial Infra-Red (Slow IR) mode support

3.7.3 Two Configurable Serial Peripheral Interfaces (CSPI1 and CSPI2) for High Speed Data Transfer

— Master/slave configurable
— Three chip-selects each for master mode operation
— Up to 16-bit programmable data transfer
— 8 × 32-bit FIFO for both transmit and receive data

3.7.4 Inter-IC (I^2C) Bus Module

— Multiple-master operation
— Software-programmable for 1 of 64 different serial clock frequencies
— Interrupt-driven, byte-by-byte data transfer
— Arbitration-lost interrupt with automatic mode switching from master to slave
— Calling address identification interrupt
— Start and stop signal generation and detection
— Repeated START signal generation
— Acknowledge bit generation and detection
— Bus-busy detection

3.7.5 Two Synchronous Serial Interfaces (SSI) with Inter-IC Sound (I^2S) and AC97 Host Controller Module (AC97)

— Supports generic SSI interface for timeslot based communication with synchronous voice codecs

— SSI signals are routed through the digital audio mux (AUDMUX) module. This module routes the signals from the two SSI modules to any of four external ports in a flexible arrangment. Additionally, the digital audio mux can route signals from these external devices directly to each other without intervention of the SSI modules.

— Supports Philips standard Inter-IC Sound (I^2S) bus for external digital audio chip interface at 44.1 kHz and 48 kHz

— AC97 Host Controller mode with support for two audio channels supporting fixed and variable rate transfers

3.7.6 Digital Audio Mux

— Supports 1 host and 3 peripheral interfaces

— Flexible audio, voice, and data routing without host processor intervention

— Built-in support for network mode connection of host and peripheral interfaces

— Separate and simultaneous audio paths from hosts to peripherals

— External 4-wire connection to synchronous devices, audio, and voice codecs

3.7.7 One-Wire Controller

— Supports One-wire interface to a 1 kbit Add-Only Memory (DS2502)

— Implements One-wire protocol defined by Dallas Semiconductors

3.7.8 Keypad Interface

— Supports up to 8×8 external key pad matrix

— Open drain design

— Glitch suppression circuit prevents erroneous key detection

— Multiple keys detection

— Standby key press detection

3.8 Memory Expansion and I/O Card Support

3.8.1 Two Multimedia Card and Secure Digital (MMC/SD) Host Controller Modules

- Fully compatible with the Multi-Media Card (MMC) *MMC System Specification,* version 2.2
- Fully compatible with the Secure Digital (SD) *SD Specification, version 1.0*, and *SD I/O specification, version 1.0* with 1 or 4 channel(s)
- 20–80 Mbps maximum data rate with up to 10 cards, one of which can be SD
- Supports hot swappable operation
- Dedicated power pin

3.9 Memory Interface

3.9.1 External Interface Module (EIM)

— Six Chip-selects (CS0-5) for external devices, each with 16 Mbyte of address space

— CS0 supports boot from ROM, NAND, or NOR Flash of up to 64 Mbyte of address space

— CS1 covers a range of 64 Mbytes, while CS2–CS5 cover a range of up to 16 Mbytes

— Programmable protection, port size, and wait states for each chip-select

— Internal and external boot ROM selection

— Selectable bus watchdog counter

— Burst support for external AMD™ or Intel® flash with 32-bit data path

— External Data Transfer Acknowledge (DTACK) support for slower devices connected on CS5

3.9.2 SDRAM Controller (SDRAMC)

— Support for four banks of single data rate 64 Mbit, 128 Mbit, and 256 Mbit SDRAM
  – Two independent chip-selects with up to 64 Mbyte per chip-select
  – Up to four banks active simultaneously for each chip-select
  – JEDEC standard pinout and operation

— PC133-compliant interface
  – 133 MHz system clock achievable with "-8" option PC133-compliant memories
  – Single and fixed-length (4-word) burst access
  – Access time of 8-1-1-1-1-1-1-1 at 133 MHz

— Software configurable for differing system requirements
  – 16-bit or 32-bit bus width
  – Configurable row cycle delay (tRC), row precharge delay (tRP), row-to-column delay (tRCD), and column-to-data delay (CAS latency)

— Built-in auto-refresh timer and state machine

— Hardware supported self-refresh entry and exit: capability to maintain valid data during system reset and low-power modes

— Auto-powerdown (clock suspend) timer

3.9.3 NAND Flash Controller (NFC)

— Contains hardware bootloader for automatic boot up from NAND Flash devices

— Supports all 8-bit/16-bit NAND Flash devices regardless of density and organization

— Supports 512-bit and 2 kbyte page sizes

— Internal 2 kbyte of buffer ram used as boot ram during cold startup and as read/write page buffers to relieve CPU intervention

— Automatic ECC detection and selectable correction

— Data protection for RAM buffer and NAND Flash pages

3.9.4 PCMCIA/CF Interface

— PCMCIA/CF host controller interface fully compliant with the *PCMCIA standard release 2.1* (PC Card -16) and *Compact Flash Specification V1.4*

— Supports one PCMCIA or CF socket

— Supports hot-insertion, card detection and removal

— Mapping to common memory space, attribute memory space, and I/O space

— Supports 7 programmable memory and I/O windows

— Generates a single interrupt to the CPU

— Programmable card access timing to interface with slower devices

— Supports TrueIDE mode

— Provides special control signals for external buffering to separate high and low speed paths

3.10 Standard System Resources

3.10.1 Clock Generation Module (CGM) and Power Control Module

— 2 digital phase-locked loops (DPLLs): MCU and system PLL and serial peripheral PLL

— MCU and system PLL generates system and CPU clocks from a 26 MHz or 32 kHz crystal

— Serial peripheral PLL generates 48 MHz clock for the USBOTG and generates clocks for other serial peripherals from a 26 MHz or 32 kHz crystal

— Support for three power modes for different power consumption needs: run, doze, and stop

— Used for clock control and gating for on-chip peripherals

3.10.2 Three General-Purpose 32-Bit Counters/Timers

— Automatic interrupt generation

— Programmable timer I/O pins

— Input capture capability with programmable trigger edge

— Output compare with programmable mode

3.10.3 Watchdog Timer

— Programmable time out of 0.5 s to 64 s

— Resolution of 0.5 s

3.10.4 Real-Time Clock/Sampling Timer (RTC)

— 32.768 kHz and 32 kHz input operation

— Full clock features: seconds, minutes, hours, days

— Capable of counting up to 512 days

— Minute countdown timer with interrupt

— Programmable daily alarm with interrupt

— Sampling timer with interrupt

— Once-per-second, once-per-minute, once-per-hour, and once-per-day interrupts

— Interrupt generation for digitizer sampling or keyboard debouncing

3.10.5 Pulse-Width Modulator (PWM) Module

— 4 × 16-bit FIFO to minimize interrupt overhead

— 16-bit resolution

— Sound and melody generation

3.10.6 Direct Memory Access Controller (DMAC)

— 16 channels that support linear memory, 2D memory, and FIFO for both source and destination

— Supports 8-bit, 16-bit, or 32-bit FIFO port size and memory port size data transfer

— DMA burst length is configurable up to maximum of 16 words, 32 half-words, or 64 bytes for each channel

— Bus utilization control for a channel that is not triggered by a DMA request

— Interrupts provided to interrupt handler on bulk data transfer complete or transfer error

— DMA burst time-out error to terminate DMA cycle when the burst cannot be completed in a programmed timing period

— Dedicated external DMA request and grant signal

— Supports increment, decrement, and no increment for source and destination addressing

— Supports DMA chaining

3.10.7 General-Purpose I/O (GPIO) Ports

— Supports level or edge trigger interrupt, system wake-up capable

— Most I/O signals are multiplexed with dedicated functions for pin efficiency

3.11 Debug Capability

- UART Bootstrap mode function:
  - — Allows user to initialize system and download program or data to system memory through UART1
  - — Accepts execution command to run program stored in system memory
  - — Supports memory/register read/write operation of selectable data size of byte, half-word, or word
  - — Provides a 16-byte instruction buffer for ARM instruction storage and execution
- USB bootstrap mode function:
  - — Supports bootstrapping through USB OTG port
- JTAG port to support generic ARM debug tools

3.12 Power Management

- Support for three power modes of operation: run, doze, and stop
- Aggressive clock gating within modules to minimize CMOS switching power
- Active well-biasing technique to reduce standby mode current consumption

3.13 Operating Voltage

— I/O voltage: 1.7 V to 2.0 V or 2.7 V to 3.3 V

— Internal logic voltage: 1.45 V to 1.65 V

3.14 Packaging Information

— Type: 0.65 mm pitch MAPBGA

— Dimensions: 14mm × 14mm

— Pins: 289

NOTES

HOW TO REACH US:

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