

MCM321024

Advance Information
1M x 32 Bit
Fast Static RAM Module

The MCM321024 is an 32M bit static random access memory module organized as 1,048,576 words of 32 bits. The module is a 72-lead single in-line memory module (SIMM) consisting of eight MCM6249 fast static RAMs packaged in 32-lead SOJ packages and mounted on a printed circuit board along with sixteen decoupling capacitors.

The MCM6249 is a high performance CMOS fast static RAM organized as 1,048,576 words of 4 bits. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM321024 is equipped with output enable (\bar{G}) and four separate byte enable (E1 – E4) inputs, allowing for greater system flexibility. The \bar{G} input, when high, will force the outputs to high impedance. Ex high will do the same for byte x.

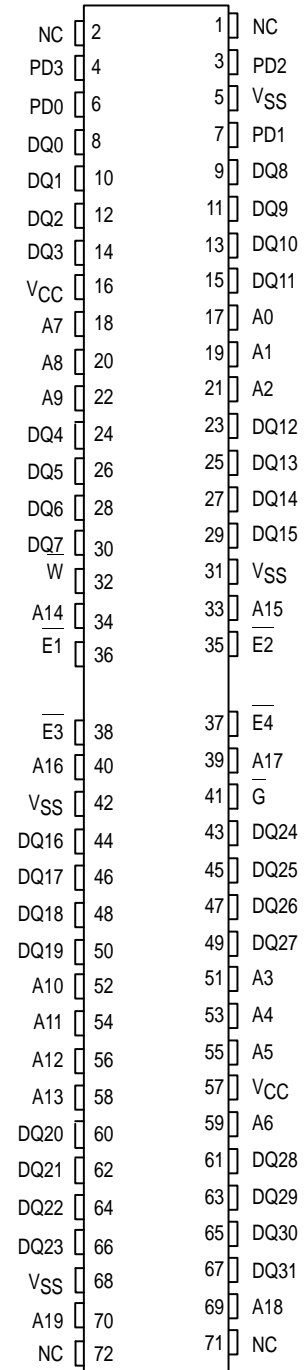
PD0 – PD3 are reserved for density identification. PD0 and PD2 are connected to ground. These pins can be used to identify the density of the memory module.

- Single 5 V \pm 10% Power Supply
- Fast Access Time: 20/25 ns
- Three-State Outputs
- Fully TTL Compatible
- JEDEC Standard Pinout
- Power Requirement: 1520/1400 mA Maximum, Active AC
- High Board Density SIMM Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte (Eight Bits)
- High Quality Six-Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State-of-the-Art Fast Static RAMs

PIN NAMES	
A0 – A19	Address Inputs
\bar{W}	Write Enable
\bar{G}	Output Enable
E1 – E4	Byte Enables
DQ0 – DQ31	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground
PD0 – PD3	Package Density
NC	No Connect

For proper operation of the device, VSS must be connected to ground.

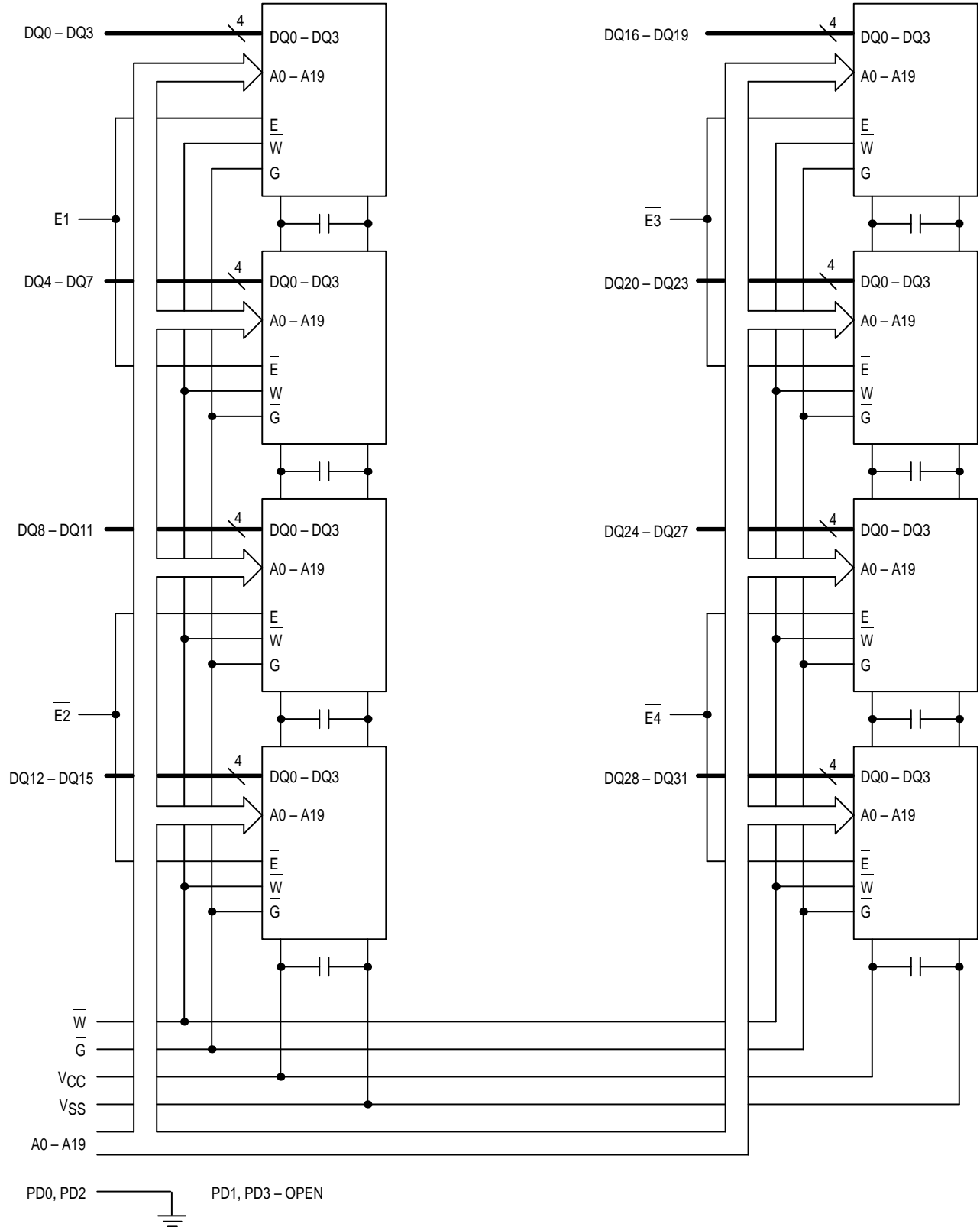
PIN ASSIGNMENT
TOP VIEW
72 LEAD SIMM — CASE TBD



This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
11/15/96

**FUNCTIONAL BLOCK DIAGRAM
1M x 32 MEMORY MODULE**



TRUTH TABLE

Ex	G	W	Mode	V _{CC} Current	Output	Cycle
H	X	X	Not Selected	I _{SB1} or I _{SB2}	High-Z	—
L	H	H	Read	I _{CCA}	High-Z	—
L	L	H	Read	I _{CCA}	D _{out}	Read Cycle
L	X	L	Write	I _{CCA}	D _{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	- 0.5 to 7.0	V
Voltage Relative to V _{SS}	V _{in} , V _{out}	- 0.5 to V _{CC} + 0.5	V
Output Current (per I/O)	I _{out}	± 30	mA
Power Dissipation	P _D	8.0	W
Temperature Under Bias	T _{bias}	- 10 to + 85	°C
Operating Temperature	T _A	0 to + 70	°C
Storage Temperature	T _{stg}	- 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V _{CC}	4.5	5.0	5.5	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} +0.3*	V
Input Low Voltage	V _{IL}	- 0.5**	—	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)

** V_{IL} (min) = - 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V _{in} = 0 to V _{CC})	I _{lkg(I)}	—	—	± 8	μA
Output Leakage Current (G, Ex = V _{IH} , V _{out} = 0 to V _{CC})	I _{lkg(O)}	—	—	± 8	μA
AC Active Supply Current (G, Ex = V _{IL} , I _{out} = 0 mA, MCM321024-20: t _{AVAV} = 20 ns Cycle time ≥ t _{AVAV} min)	I _{CCA}	—	1440 1320	1520 1400	mA
AC Standby Current (Ex = V _{IH} , Cycle time ≥ t _{AVAV} min)	I _{SB1}	—	400	480	mA
CMOS Standby Current (Ex ≥ V _{CC} - 0.2 V, All Inputs ≥ V _{CC} - 0.2 V or ≤ 0.2 V)	I _{SB2}	—	80	120	mA
Output Low Voltage (I _{OL} = + 8.0 mA)	V _{OL}	—	—	0.4	V
Output High Voltage (I _{OH} = - 4.0 mA)	V _{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All pins except DQ0 - DQ31, W, G, and E1 - E4 E1 - E4 W, G)	C _{in}	32 10 40	48 14 64	pF
Input/Output Capacitance (DQ0 - DQ31)	C _{out}	8	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 10\%$, $T_A = 0\text{ to } +70^\circ\text{C}$, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V
 Output Timing Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V

Output Load See Figure 1a Unless Otherwise Noted
 Input Rise/Fall Time 3 ns

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM321024-20		MCM321024-25		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	ns	
Output Enable Access Time	t_{GLQV}	—	7	—	9	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	ns	4,5,6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	0	9	0	10	ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	0	9	0	10	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	ns	

NOTES:

1. \bar{W} is high for read cycle.
2. E1 – E4 are represented by \bar{E} in these timing specifications, any combination of Exs may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1b.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($E = V_{IL}$, $G = V_{IL}$). See Read Cycle 1.

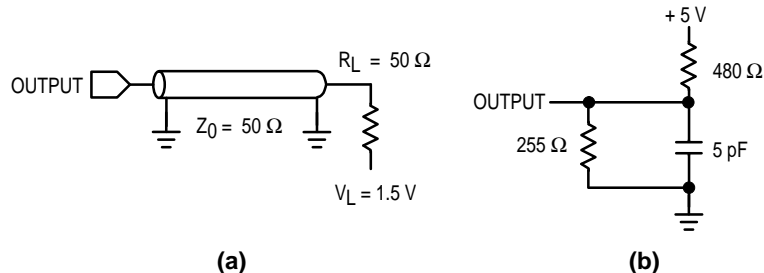
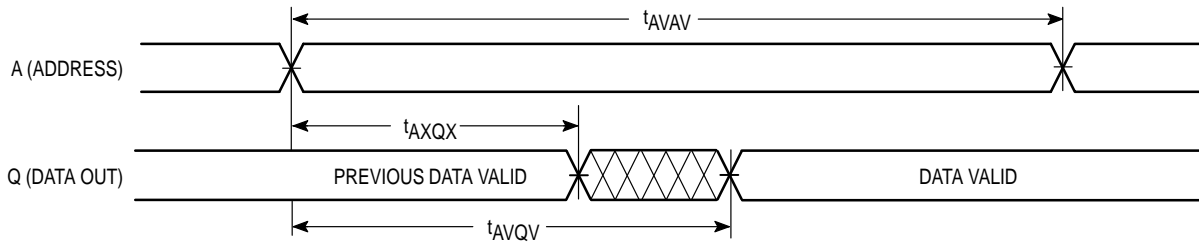


Figure 1. Test Loads

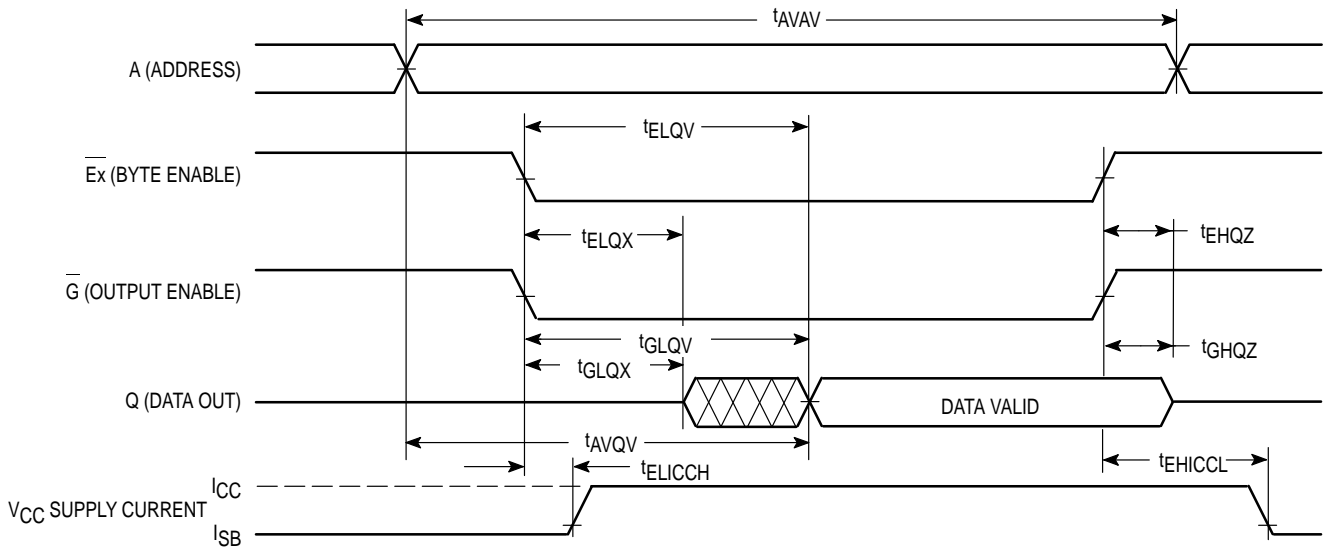
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with \bar{E} going low.

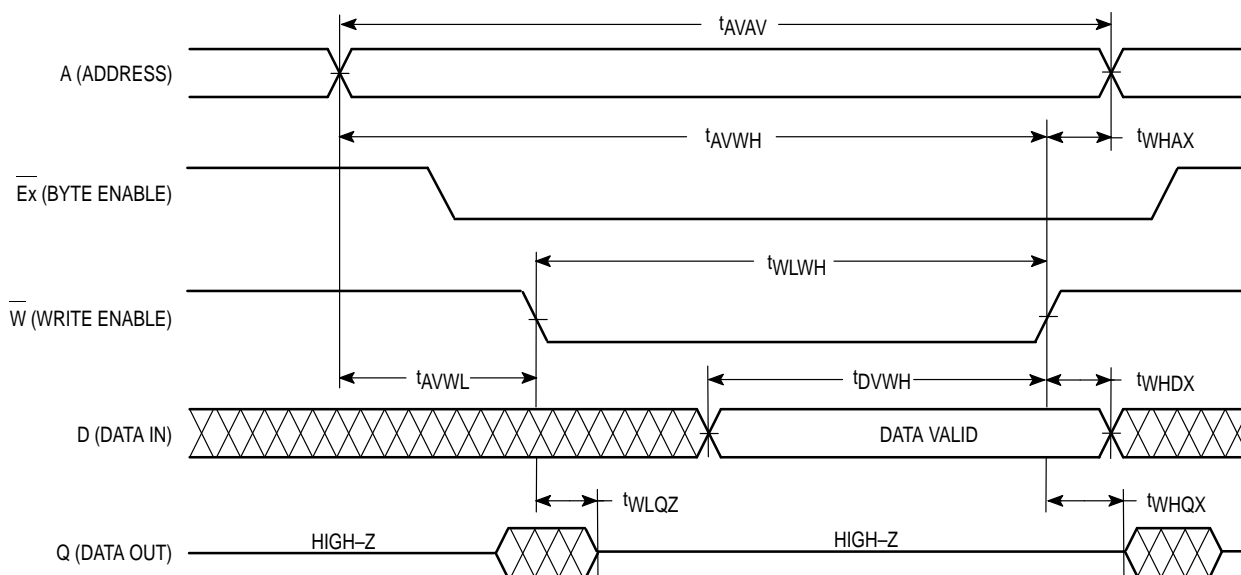
WRITE CYCLE 1 (\overline{W} Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM321024-20		MCM321024-25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	ns	
Write Pulse Width	t_{WLWH} , t_{WLEH}	15	—	17	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	0	9	0	10	ns	4,5,6
Write High to Output Active	t_{WHQX}	5	—	5	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. E1 – E4 are represented by E in these timing specifications, any combination of Exs may be asserted. \overline{G} is a don't care when \overline{W} is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1



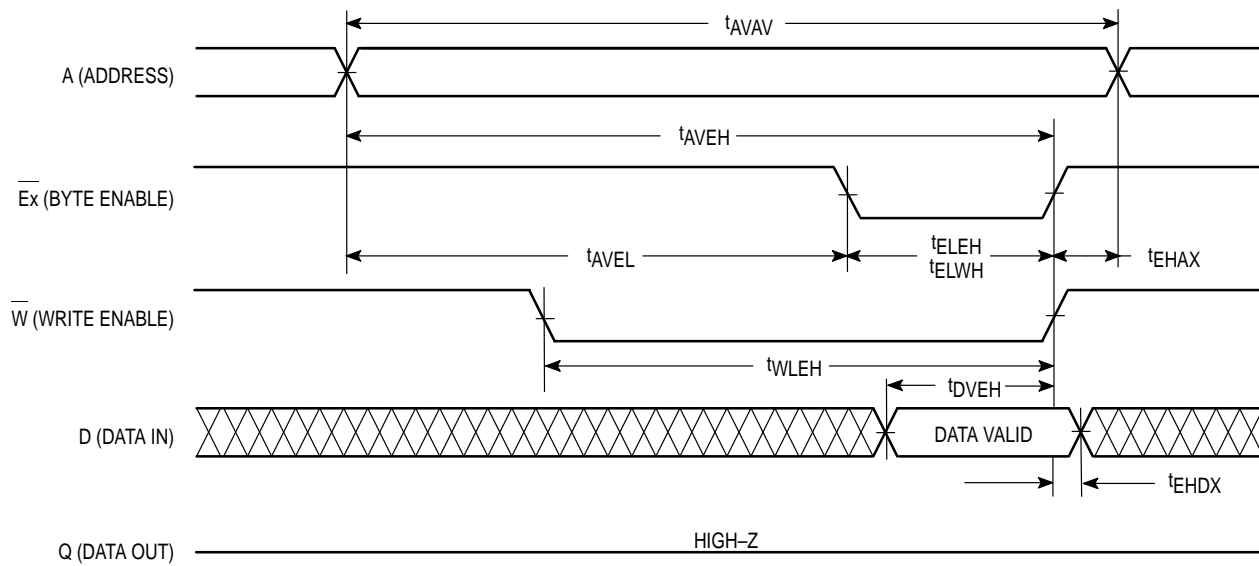
WRITE CYCLE 2 (\bar{E} Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM321024-20		MCM321024-25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	ns	
Enable to End of Write	t_{ELEH}	15	—	17	—	ns	4,5
Enable to End of Write	t_{ELWH}	15	—	17	—	ns	
Write Pulse Width	t_{WLEH}	15	—	17	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

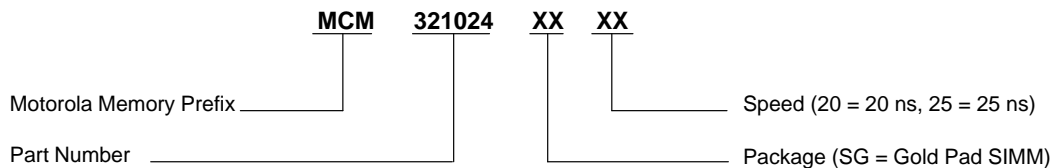
NOTES:

1. A write occurs during the overlap of \bar{E} low and \bar{W} low.
2. E1 – E4 are represented by E in these timing specifications, any combination of Exs may be asserted. \bar{G} is a don't care when \bar{W} is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If \bar{E} goes low coincident with or after \bar{W} goes low, the output will remain in a high impedance condition.
5. If E goes high coincident with or before \bar{W} goes high, the output will remain in a high impedance condition.


WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM321024SG20 MCM321024SG25

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