Micro Linear

ML6680

Token Ring Copper-to-Fiber Converter

GENERAL DESCRIPTION

The ML6680 is a single-chip conversion between Token Ring ISO/IEC8802-5 copper-based media and Token Ring ISO/IEC8802-5 fiber-based media. The ML6680 fiber-optic interface contains a data quantizer, circuitry for fiber optic key signal generation and recognition, pin-selectable signal switching, and current driven transmitter outputs.

The ML6680 copper interface consists of a twisted pair line equalizer, receive squelch circuit, pin selectable phantom wire fault detection and signal switching, and a transmit driver. This section supports the ISO/IEC8802-5 standard requirements. The ML6680 provides an optional PECL compatible interface.

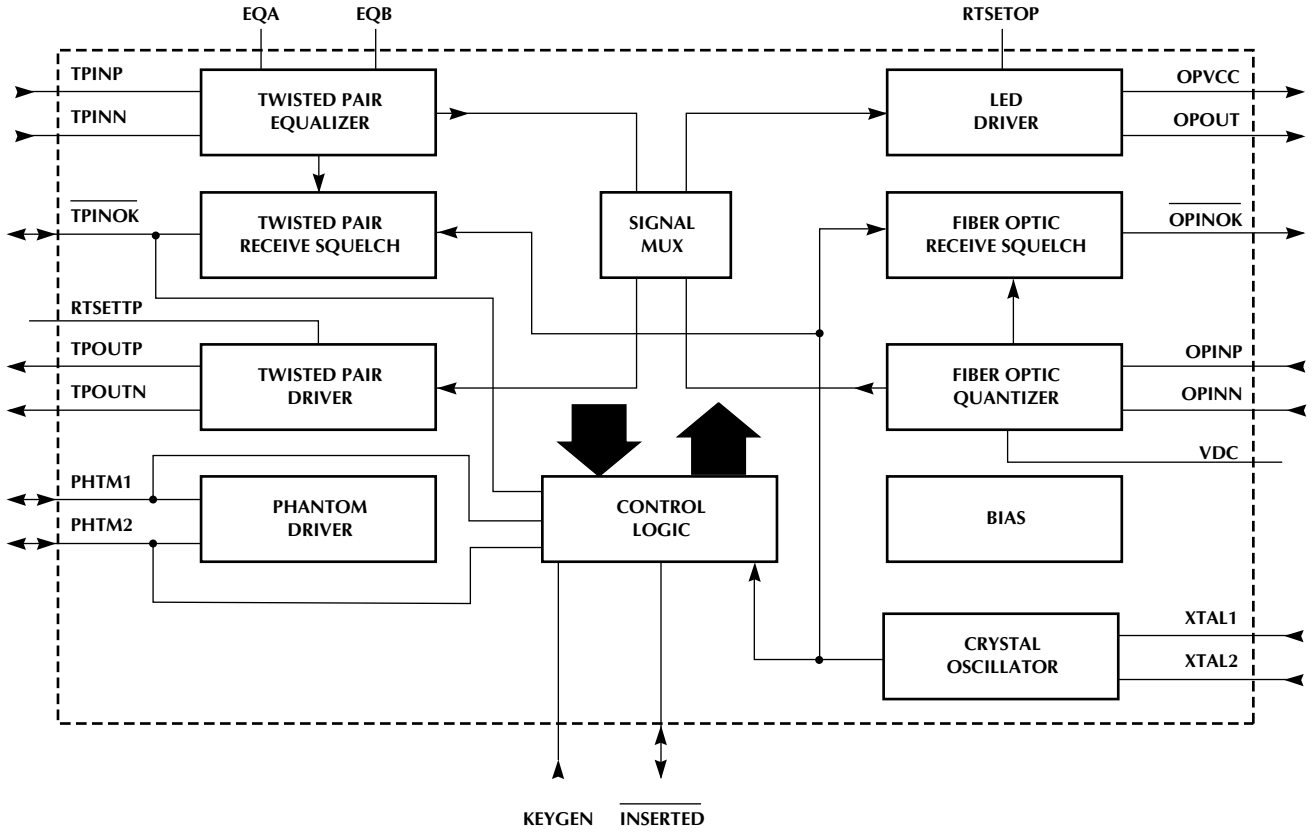
The ML6680 may be configured to one of four modes:

1. Standard Media Converter
2. Concentrator Media Converter
3. Lobe or Ring Out Port Media Converter
4. Ring In Port Media Converter

FEATURES

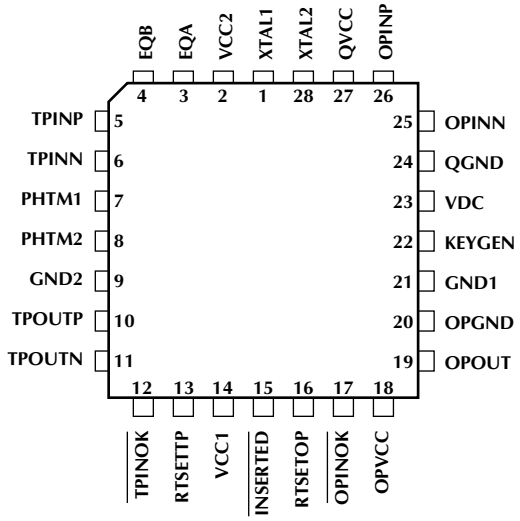
- Single-chip copper-to-fiber converter for Token Ring
- 16Mbps and 4Mbps data rates with the same external components
- Four modes of operation covering a wide variety of applications
- Full duplex operation
- Highly stable data quantizer with 55dB input dynamic range
- Current driven fiber optic LED driver for accurate launch power
- Current driven output for low RFI noise and low jitter
- Capable of driving 100Ω UTP or 150Ω STP
- Pin selectable phantom wire fault detection and signal switching

BLOCK DIAGRAM



PIN CONFIGURATION

ML6680
28-Pin PLCC (Q28)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1, 28	XTAL1, XTAL2	Crystal inputs. A 32.768kHz watch crystal connected between these pins provides timing for the fiber optic insertion key signal. An external clock can be used to drive XTAL1 while grounding XTAL2. The frequency of the external clock should be between 32.7kHz and 34.5kHz.
2	V_{CC2}	Positive 5V power supply.
3, 4	EQA, EQB	Equalizer network pins. An external combination of two resistors and a capacitor connected at EQA and EQB sets up the on-chip twisted pair receive equalizer.
5, 6	TPINP/N	Receive twisted pair inputs. This differential input pair receives differential Manchester signals from the coupling transformer (or PECL compatible levels).
7, 8	PHTM1/2	Phantom drive/sense inputs/outputs. In configuration 1, these pins are TTL inputs from two external opto isolators. They are low when phantom power is present and high when phantom power is removed. These pins provide the phantom drive current and are used to check for a wire fault on the phantom circuits when it is required in configuration 2. In configuration 3, these pins are don't cares. In configuration 4, these pins are low for normal operation, or any or both of them is high to force the ML6680 into the "Bypass State."
9	GND2	Ground.
10, 11	TPOUTP/N	Transmit twisted pair outputs. This differential current output pair drives differential Manchester signals into the network coupling transformer and transmit filter. Output edge rates are controlled to allow use of a simpler filter than would otherwise be required. These outputs can be PECL compatible with an external resistor network.
12	$\overline{\text{TPINOK}}$	Valid twisted pair input signal indicator. It is an active low, open collector LED driver. This output goes low when the signal at TPINP/N meets frequency and amplitude squelch requirements. This input is tied to ground for configurations 3 and 4 to enable signal path switching.
13	RTSETTP	Twisted pair transmit level set resistor input. A precision resistor between RTSETTP and VCC sets the amplitude of the TPOUTP/N output.
14	VCC1	Positive 5V power supply.
15	$\overline{\text{INSERTED}}$	Insertion indicator. It is an active low, open collector LED driver. In configurations 1, 3 and 4 this output goes low when the ML6680 is in the "Insert State." In configuration 2 this output goes low when the ML6680 is in the "Insert State" and no wire fault is detected. This input is tied to ground to disable the frequency squelch, and to reduce the time constant of the amplitude squelch of the optical input.
16	RTSETOP	A precision resistor between RTSETOP and VCC sets the amplitude of the OPOUT output.
17	$\overline{\text{OPINOK}}$	Valid fiber optic input signal indicator. It is an active low, open collector LED driver. This output goes low when the signal at OPINP/N meets frequency and amplitude squelch limit for received signals at TPINP/N.
18	OPVCC	Positive 5V power supply for fiber optic LED driver.
19	OPOUT	Fiber optic LED driver output. The fiber optic LED connects between this pin and OPVCC.
20	OPGND	Ground for the fiber optic LED driver.
21	GND1	Ground.
22	KEYGEN	Key generation select CMOS input. This input is low for configurations 2 and 3 of the general description, and is high for configurations 1 and 4.
23	VDC	Offset correction time constant capacitor input. An external capacitor between this pin and QGND determines the time constant of the internal offset correction circuit for the fiber optic quantizer.
24	QGND	Quantizer's ground.
26, 25	OPINP/N	Receive fiber inputs. This pair of inputs receive differential Manchester signals from the fiber optic receiver/preamp and present them to the on-chip fiber optic quantizer. These inputs should be capacitively coupled to the input source. The input resistance is approximately 1.3kΩ.
27	QVCC	Quantizer's positive 5V power supply.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Power Supply Voltage Range, V_{CC} ..... –0.3 to 6V
Input Voltage Range ..... –0.3 to V_{CC}
Output Current
  TPOUTP, TPOUTN 50mA
  OPOUT 70mA
  PHTM1, PHTM2 ..... 10mA
Input Current
  RTSETTP, RTSETOP, $\overline{\text{TPINOK}}$,
  $\overline{\text{OPINOK}}$, $\overline{\text{INSERTED}}$ 20mA
Storage Temperature ..... –65°C to 150°C
Lead Temperature (soldering, 10 sec.) ..... 260°
Thermal Resistance ..... 68°C/W

OPERATING CONDITIONS

Power Supply Voltage, V_{CC} ..... 5V ± 5%
All V_{CC} supply pins must be within 0.1V of each other.
All GND pins must be within 0.1V of each other.
Ambient Temperature, T_A ..... 0°C to 70°C
Junction Temperature, T_J ..... 0°C to 125°C
LED on Current 4mA
RTSETOP ..... 115Ω ± 1%
RTSETTP ..... 255Ω ± 1%

ELECTRICAL CHARACTERISTICS

Over full range of operating conditions unless otherwise specified (Note 1).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY CURRENT						
I_{CC1}	V_{CC} Supply Current	No transmitting, phantom power off	30	36	50	mA
I_{CC2}	V_{CC} Supply Current	RTSETTP = 255, RTSETOP = 115, transmitting, phantom power on (Note 2)	120		160	mA
CMOS INPUTS PHTM1, PHTM2 (when KEYGEN = High or $\overline{\text{TPINOK}}$ is grounded) **AND KEYGEN**						
V_{ILC}	Input Low Voltage				0.1 x V_{CC}	V
V_{IHC}	Input High Voltage		0.9 x V_{CC}			V
TTL INPUT: XTAL1						
V_{ILT}	Input Low Voltage				0.8	V
V_{IHT}	Input High Voltage		2			V
I_{ILT}	Input Low Current	V(XTAL1) = 0V	–100			µA
I_{IHT}	Input High Current	V(XTAL1) = 2.7V			100	µA
R_{IX1}	Input Resistance		400		560	kΩ
CONTROL INPUTS: INSERTED, TPINOK						
V_{ILS}	Input Low Voltage				0.1	V
I_{ILS}	Input Low Current	V_{IN} = 0V	–50			µA
STATUS LED OUTPUTS: INSERTED, TPINOK, OPINOK						
I_{OLS}	Output Low Current	Pin connected to V_{CC}	14	19	24	mA
I_{OHS}	Output Off Current			3	10	µA

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PHANTOM DRIVE OUTPUTS: PHTM1, PHTM2						
R_{NF}	No Fault Phantom Load Resistance		2.9		5.5	kΩ
R_{SC}	Short Circuit Phantom Load Resistance				50	Ω
R_{OC}	Open Circuit Phantom Load Resistance		50			kΩ
V_{OHP}	Phantom Output High Voltage	I_{OHP} > –1mA	4.1			V
		I_{OHP} > –2mA	3.5			V
I_{SC}	Phantom Short Circuit Current	V(PHTM1) or V(PHTM2) = 0V		–1.8	–1.2	mA
I_{OFFP}	Phantom Off Current	V(PHTM1) or V(PHTM2) = 0V	–100		100	µA
TWISTED PAIR RECEIVER: TPINP, TPINN						
V_{OSRTP}	Differential Offset Voltage		–35		35	mV
V_{DSTP}	Differential Squelch Threshold		200		300	mV_{P-P}
V_{PSTP}	Differential Post-Squelch Threshold		100		150	mV_{P-P}
V_{CMTP}	Open-Circuit Common Mode Bias Voltage			2.4		V
R_{IDRTP}	Differential Input Resistance		8	9.6	12.5	kΩ
TWISTED PAIR TRANSMITTER: TPOUTP, TPOUTN						
I_{TTP}	Peak Output Current	RTSETTP = 255Ω, Pins Connected to V_{CC}	27		29.5	mA
I_{OFFTP}	Off State Output Current				1.5	mA
I_{DCI}	Differential Current Im Balance		–300		300	µA
OPTICAL RECEIVER: OPINP, OPINN						
V_{CMOP}	Open Circuit Common Mode Bias Voltage			1.6		V
V_{IROP}	Input Signal Range		V_{DSOP}		1600	mV_{P-P}
V_{OSROP}	Differential Offset Voltage			3		mV
EN	Input Referred Voltage Noise	50MHz BW		25		μV_{RMS}
R_{IDROP}	Differential Input Resistance		1.8	2.6	3.3	kΩ
V_{DSOP}	Differential Squelch Threshold		5		6	mV_{P-P}
V_{PSOP}	Differential Post Squelch Threshold		4		5	mV_{P-P}
H	Hysteresis			20		%
OPTICAL TRANSMITTER: OPOUT						
I_{TOP}	Peak Output Current	RTSETOP = 115Ω	47	52	57	mA
I_{OFFOP}	Off State Output Current				1	mA

AC CHARACTERISTICS

Over full range of operating conditions unless otherwise specified. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK REFERENCE: XTAL1						
f_{XO}	Reference Clock Frequency		32.7		34.5	kHz
D_{XO}	Reference Clock Duty Cycle		30		70	%
TWISTED PAIR RECEIVER: TPINP, TPINN						
t_{THTP}	Input Pulse Width Threshold		550		1000	ns
t_{USQTP}	Time to Unsquelch (Off to On)		2		5	µs
t_{REJTP}	Time to Reject (On to Off)		550		1000	ns
OPTICAL RECEIVER: OPINP, OPINN						
t_{THOP}	Input Pulse Width Threshold	V($\overline{\text{INSERTED}}$) > 0.7V	550		1000	ns
t_{USQOP}	Time to Unsquelch (Off to On)	V($\overline{\text{INSERTED}}$) > 0.7V	3		9	µs
		V($\overline{\text{INSERTED}}$) = 0V	0.8		1.2	µs
t_{REJOP}	Time to Reject (On to Off)	V($\overline{\text{INSERTED}}$) > 0.7V	3		9	µs
		V($\overline{\text{INSERTED}}$) = 0V	0.8		1.2	µs
PROPAGATION DELAYS STEADY STATE						
t_{TPOP}	TPINP-TPINN to OPOUT				20	ns
t_{OPTP}	OPINP-OPINN to TPOUTP-TPOUTN				30	ns
t_{TPTP}	TPINP-TPINN to TPOUTP-TPOUTN				30	ns
t_{OPOP}	OPINP-OPINN to OPOUT				20	ns
INSERTION AND BYPASS KEY GENERATION (Fig. 1)						
T_K1	Key Element #1 (avg. $P_O < P_{O\_Off}$)		808		858	µs
T_K2	Key Element #2 (avg. $P_O > P_{O\_Off}$)		1616		1717	µs
T_K3	Key Element #3 (avg. $P_O < P_{O\_Off}$)		1616			µs
T_BYP	Bypass Element (avg. $P_O > P_{O\_Off}$)		4.85	26.5		ms
T_KINIT1	Time that phantom power should be applied in config 1 before generating the insertion key.	V(KEYGEN) = V_{CC}, V($\overline{\text{TPINOK}}$) > 0.7V		26.5		ms
T_KINIT4	Time that the optical input should be valid in config 4 before generating the insertion key.	V(KEYGEN) = V_{CC}, V($\overline{\text{TPINOK}}$) = 0V V(PHTM1) = 0V, V(PHTM2) = 0V		26.5		ms
T_KOFF	Time that the optical input should be invalid before generating the bypass key.	V(KEYGEN) = VCC, V($\overline{\text{TPINOK}}$) = 0V V(PHTM1) = 0V, V(PHTM2) = 0V		26.5		ms

AC CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INSERTION KEY ECHO AND BYPASS KEY RECOGNITION (Fig. 1)						
T_ECHO	Time since starting insertion key generation until receiving the insertion key echo.				100	ms
T_E1Key	Key Echo From T_K1		766		900	µs
T_E2Key	Key Echo From T_K2		1533		1800	µs
T_E3Key	Key Echo From T_K3		1533			µs
T_BYPDET	Time of optical input not valid before recognizing a bypass key		4		4.5	ms

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 2: Current into all V_{CC} pins, external bias resistors, and external transmit loads. Does not include status LED's current.

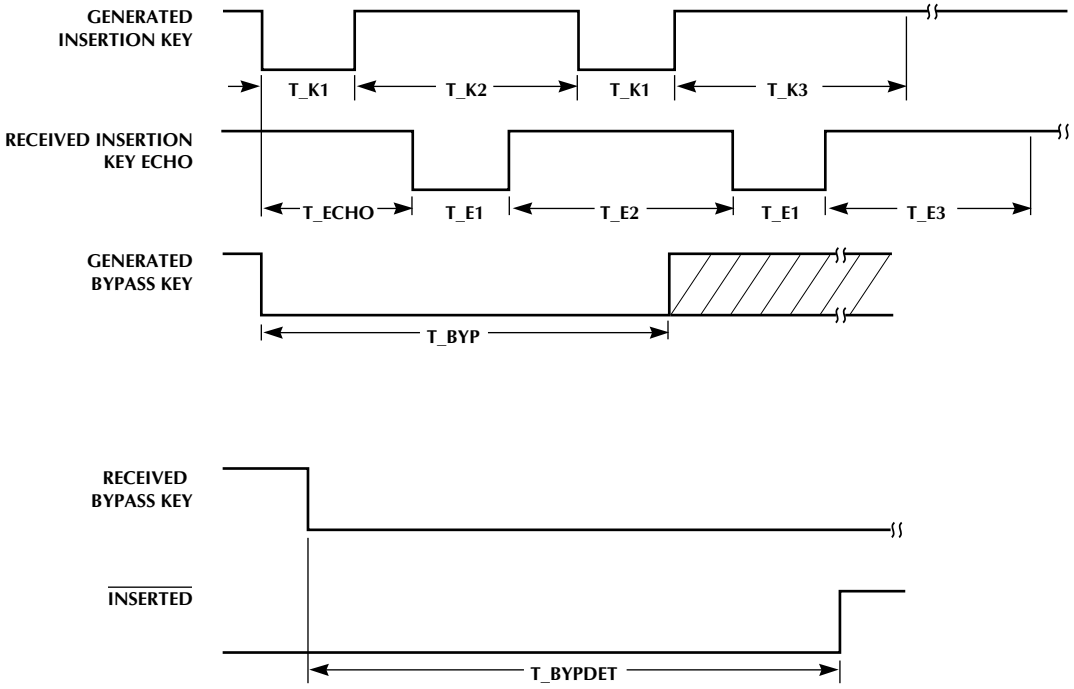


Figure 1

FUNCTIONAL DESCRIPTION

Fiber Optic LED Driver

The output stage of the transmitter is a current mode switch which develops the output light by sinking current from OPVCC through the LED into the OPOUT pin. Once the current requirement for the LED is determined, the RTSETOP resistor is selected. The following equation is used to select the correct RTSETOP resistor:

$$RTSETOP = (52mA/I_{OUT}) \times 115\Omega$$

No current is provided during the off cycles of the Insertion, Bypass, or Echo Keys, or when the input signal that should be routed to the Fiber Optic LED Driver does not meet the corresponding input squelch requirements.

Fiber Optic Quantizer

The OPINP, OPINN input signal is fed into a limiting amplifier with a gain of about 100 and input resistance of 1.3kΩ. Maximum sensitivity is achieved through the use of a DC restoration feedback loop and AC coupling the input. When AC coupled, the input DC bias voltage is set by an on-chip network at about 1.7V. These coupling capacitors, in conjunction with the input impedance of the amplifier, establish a high pass filter with 3dB corner frequency, f_L, at

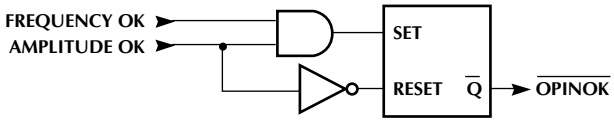
$$f_L = 1/(2 \times \pi \times 1300 \times C)$$

Since the amplifier has a differential input, two capacitors of equal value are required. If the signal driving the input is single ended, one of the coupling capacitors can be tied to V_{CC}. The internal amplifier has a lowpass filter built-in to band limit the input signal which in turn will improve the signal to noise ratio. Although the input is AC coupled, the offset voltage, V_{OS}, within the amplifier will be present at the amplifier's output. In order to reduce this error a DC feedback loop nulls the offset voltage, forcing V_{OS} to be zero. The comparator is a high-speed differential zero crossing detector that slices and accurately digitizes the receive signal. The output of the comparator is fed in parallel into both the fiber optic squelch circuit and the signal MUX. The capacitor between pin VDC and QGND should be set to 500pF.

Fiber Optic Squelch

The ML6680 monitors the frequency and amplitude of the input from a fiberoptic receiver. The optical squelch circuit rejects signals whose frequencies are lower than 1MHz or whose amplitudes are lower than –32dBm.

If both requirements are met, the LED output $\overline{OPINOK}$ goes low, and the amplitude threshold is lowered 20%.



Copper Pair Driver

The output stage of the twisted pair transmitter is a current mode switch which develops the output voltage by driving current through the terminating resistor and the output filter. The harmonic content is controlled to simplify the filter design. The transmitter employs a center tap 2:1 transformer where the center tap is tied to V_{CC}. While one pin of the transmit pair is pulled low, the other pin floats. The output pins to the twisted pair wires, TPOUTP and TPOUTN, can drive shielded or unshielded twisted pair cable through the appropriate isolation transformer. The output current is set by the value of RTSETTP. No transitions are generated at TPOUTP and TPOUTN when the input signal that should be routed to the Copper Pair Driver does not meet the corresponding input squelch requirements. PECL compatible output are obtained with an external network of 3 resistors. In this case the current of the output stage can be reduced by adjusting the value of RTSETTP.

Twisted Pair Line Equalizer

The receive equalizer compensates for twisted pair cable dispersion, which otherwise would give rise to inter-symbol interference (ISI). The amount of equalization varies with the average amplitude of the received signal. The received signal amplitude gives a rough value for the length of the attached cable. The filter/equalizer characteristic is the inverse of the cable's dispersion characteristic. Both UTP and STP cables approximate a low-pass filter, so the filter/equalizer approximates an inverse square root equalizer. Two external resistors and one external capacitors are required between pins EQA and EQB. The output of the equalizer is fed into the signal MUX. On a PECL application these pins should be connected between each other.

Twisted Pair Squelch Circuit

The twisted pair line receiver internally sets the common mode bias of the input TPINP and TPINN. Voltage offset comparators are used to set the amplitude squelch threshold, and analog timers are used to set the pulse width squelch threshold. When the input signal meets amplitude and pulse width requirements, the squelch circuit reduces the offset voltage of the comparators, decreasing the amplitude squelch threshold by half. This hysteresis allows the receiver to stay on in the presence of a fading input signal. The twisted pair squelch circuit rejects signals whose frequencies are lower than 1MHz or whose amplitudes are lower than $300mV_{P-P}$. If both requirements are met, the LED output $\overline{TPINOK}$ goes low.

Clock Oscillator

The ML6680 provides an on-chip clock oscillator by connecting a 32.768kHz watch crystal between pins XTAL1 and XTAL2. The part can also be driven by an external clock applied at XTAL1 and tying XTAL2 to ground. The frequency of the external clock should be between 32.7kHz and 34.5kHz.

Status LED Drivers

The ML6680 has three status LED drivers. The LED driver pins are active low. The LED's are tied to their respective pins through a 300Ω resistor to V_{CC}.

Modes of Operation

Four configurations are possible with the ML6680, as follows:

1. Standard Media Converter: Senses ISO/IEC8802-5 phantom power and generates ISO/IEC8802-5 fiberoptic insertion or bypass requests.
2. Concentrator Media Converter: Recognizes the ISO/IEC8802-5 fiberoptic insertion or bypass requests and drives the ISO/IEC8802-5 phantom circuits.
3. Lobe or Ring Out Port Media Converter: Recognizes the ISO/IEC8802-5 fiberoptic insertion or bypass requests.
4. Ring In Port Media Converter: Generates ISO/IEC8802-5 fiberoptic insertion or bypass requests. Modifies the internal signal paths depending on the presence or absence of a fiberoptic link, and on the reception of the ISO/IEC8802-5 "Insertion Key Echo."

CONFIGURATION 1

Standard Media Converter:

This configuration is selected by tying KEYGEN to VCC. There are always two fixed signal paths, one from TPINP and TPINN to OPVCC and OPOUT, and another from OPINP and OPINN to TPOUTP and TPOUTN. The generation of the "Insertion Key" or "Bypass Key" is exclusively controlled by the logic values at PHTM1 and PHTM2. The "Insertion Key" is generated when both PHTM1 and PHTM2 go low, and stay low for at least 26.5ms. If the "Insertion Key Echo" is received within the following 100ms, the part goes to the "Insert State" and the LED output $\overline{\text{INSERTED}}$ goes low. During the generation of the "Insertion Key," and while waiting for the "Insertion Key Echo" the states of PHTM1 and PHTM2 do not have any effect. When the part is in the "Insert State" and either PHTM1 or PHTM2 goes high, the LED output $\overline{\text{INSERTED}}$ goes high, the part leaves the "Insert State," generates the "Bypass Key," and starts waiting for PHTM1 and PHTM2 to go low again.

CONFIGURATION 2

Concentrator Media Converter:

This configuration is selected by tying KEYGEN to ground. There are always two fixed signal paths, one from TPINP and TPINN to OPVCC and OPOUT, and another from OPINP and OPINN to TPOUTP and TPOUTN. The part powers on in the "Bypass State" where it neither applies phantom current nor checks for a phantom wire fault. After recognizing an "Insertion Key" at its fiber optic inputs, it applies phantom power by providing current at PHTM1 and PHTM2, goes to the "Phantom Wire Fault Check State," and starts waiting for a "Bypass Key." At this state, the LED output $\overline{\text{INSERTED}}$ stays low while no phantom wire fault is detected. When the part is in the "Phantom Wire Fault Check State" and a "Bypass Key" is recognized, the part leaves this state, removes the phantom power, and starts waiting for a "Insertion Key" again.

CONFIGURATION 3

Lobe or Ring Out Port Media Converter:

This configuration is selected by tying both KEYGEN and $\overline{\text{TPINOK}}$ to ground. When the ML6680 is in the "Insert State," the signal paths are from TPINP and TPINN to OPVCC and OPOUT, and from OPINP and OPINN to TPOUTP and TPOUTN. Otherwise, the signal paths are from TPINP and TPINN to TPOUTP and TPOUTN, and from OPINP and OPINN to OPVCC and OPOUT. The part powers on in the "Bypass State" and goes to the "Insert State" after recognizing an "Insertion Key" at its fiber optic inputs. It goes back to the "Bypass State" after recognizing a "Bypass Key." While it is at the "Insert State," the LED output $\overline{\text{INSERTED}}$ stays low.

CONFIGURATION 4

Ring In Port Media Converter:

This configuration is selected by tying KEYGEN to VCC and $\overline{\text{TPINOK}}$ to ground. When the part is in the "Insert State," the signal paths are from TPINP and TPINN to OPVCC and OPOUT, and from OPINP and OPINN to TPOUTP and TPOUTN. Otherwise, the input at TPINP and TPINN is routed to TPOUTP and TPOUTN, and also to OPVCC and OPOUT. The "Insertion Key" is generated when activity is detected at OPINP and OPINN for at least 26.5ms and, PHTM1 and PHTM2 stay low. If the "Insertion Key Echo" is received within the following 100ms, the ML6680 goes to the "Insert State" and the LED output $\overline{\text{INSERTED}}$ goes low. During the generation of the "Insertion Key," and while waiting for the "Insertion Key Echo" the logic states of PHTM1 and PHTM2 do not have any effect. When the part is in the "Insert State" and no activity is detected at OPINP and OPINN for at least 26.5ms, or either PHTM1 or PHTM2 goes high, the LED output $\overline{\text{INSERTED}}$ goes high, the part leaves the "Insert State," generates the "Bypass Key," and starts waiting for 26.5ms of optical input activity again.

Low Frequency Signaling Mode

Some old implementations of discrete media converters, use a non-standard protocol with frequencies between 1 and 10kHz. To facilitate the migration to the ML6680, a specific operating mode is provided by grounding the pin $\overline{\text{INSERTED}}$. Pin KEYGEN should also be grounded to prevent the generation of unwanted "Insertion" or "Bypass Keys." In this operating mode, the optical frequency squelch circuitry is disabled and the time constant of the amplitude squelch is significantly reduced.

For each edge of the low frequency optical input, the ML6680 generates a pulse at the led output $\overline{\text{OPINOK}}$. It also generates a pulse at the TPOUTP output for each rising edge and another at the TPOUTN output for each falling edge.

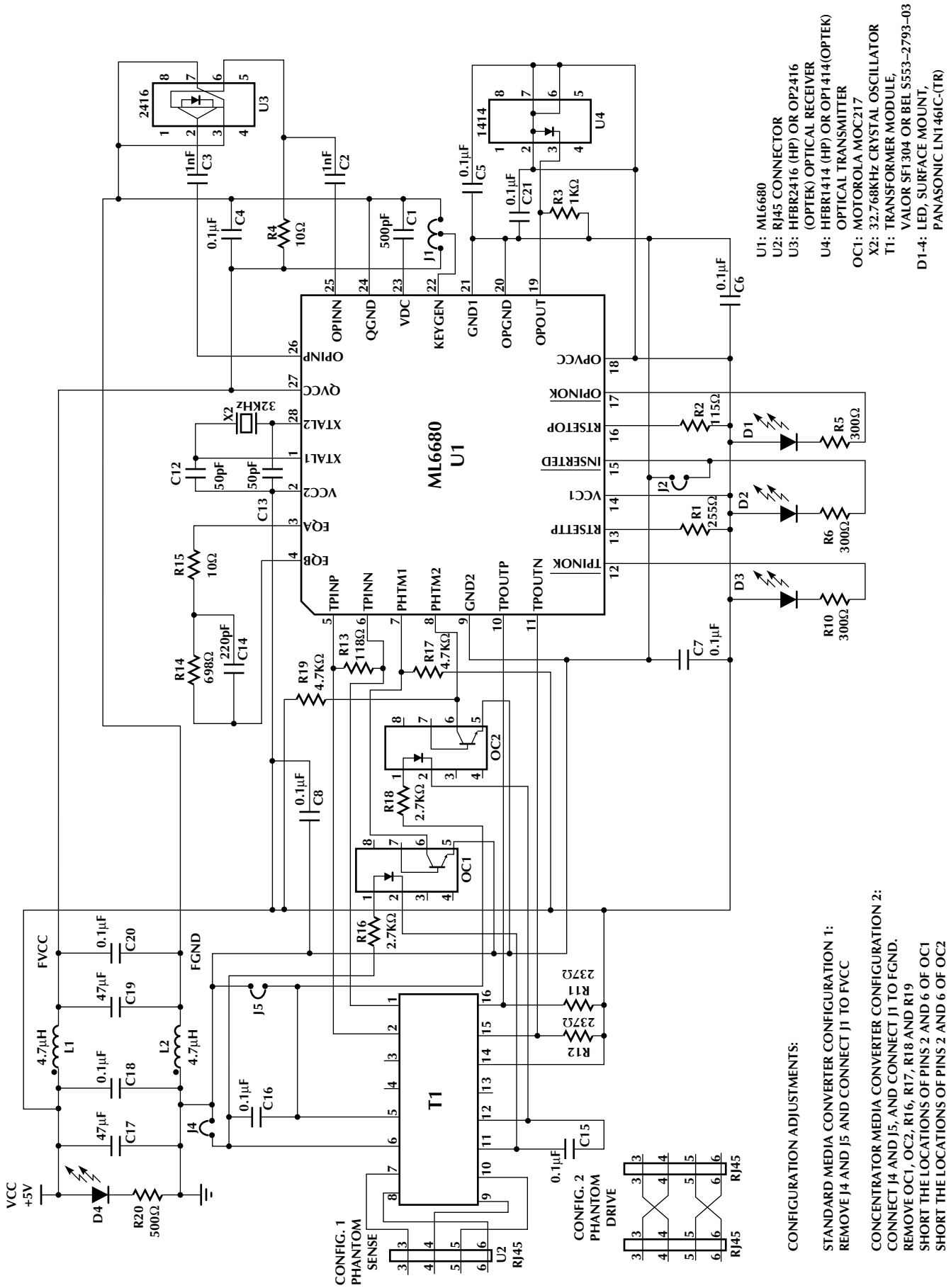


Figure 2. ML6680 Configurations 1 and 2

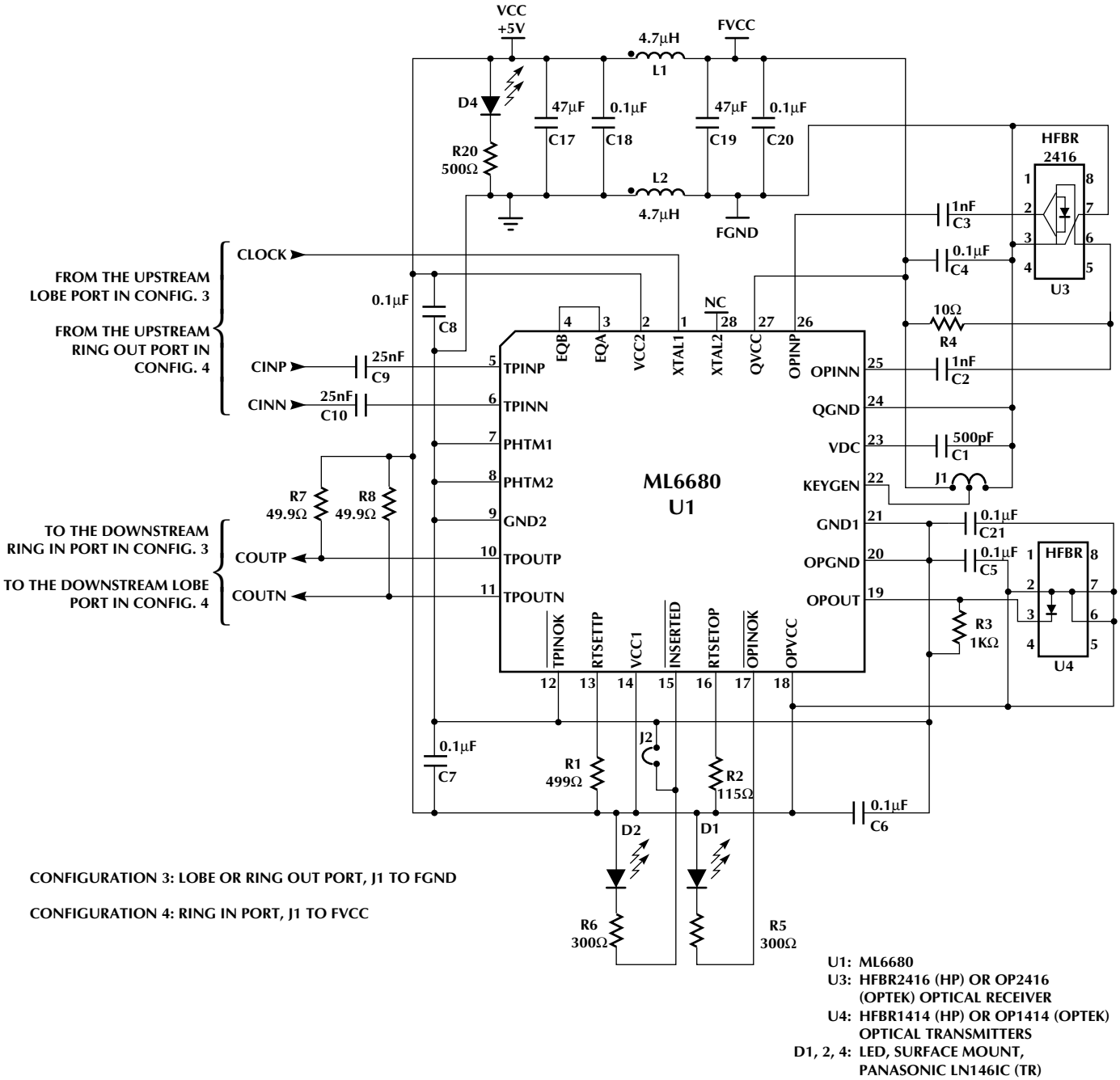
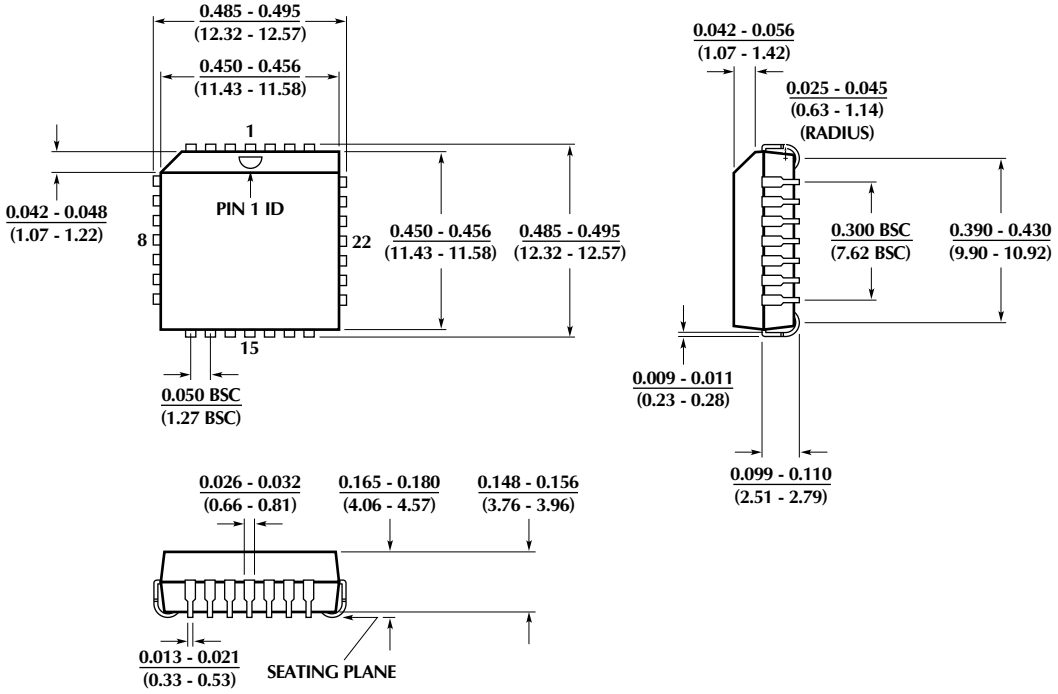


Figure 3. ML6680 Configurations 3 and 4

PHYSICAL DIMENSIONS inches (millimeters)

Package: Q28
28-Pin PLCC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6680CQ	0°C to 70°C	28-PIN PLCC (Q28)

2092 Concourse Drive
San Jose, CA 95131
Tel: 408/433-5200
Fax: 408/432-0295